

December 1, 2014

Product Specifications of the RX113 Group of MCUs

*Upper: Temperature range for the operation: -40 to +85°C Lower: Temperature range for the operation -40 to +105°C

Group name		RX113				
Dort No.*		R5F51138ADxx	R5F51137ADxx	R5F51136ADxx	R5F51135ADxx	
Part No.*		R5F51138AGxx	R5F51137AGxx	R5F51136AGxx	R5F51135AGxx	
Internal memory	Flash ROM	512 KB	384 KB	256 KB	128 KB	
	RAM	64 KB		32 KB		
	E2 data flash	8 KB				
Power supply voltage		1.8 to 3.6 V				
Maximum operating frequency		32 MHz				
Temperature range for the operation		−40 to +85°C or −40 to +105°C				
CPU core		 RX CPU General registers: 32-bit × 16 Multiplier: 32-bit multiplier Divider: Yes Multiply-accumulator: Yes (two types: memory-to-memory operations and register-to-register operations) 				
On-chip peripheral functions		Transfer functions	Data trai	nsfer controller (DTCa)	

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	Timers	 Multi-function timer pulse unit 2: 16 bits × 6 channels (MTU2a) Port output enable 2 (POE2a) Compare match timer (CMT): 16 bits × 2 channels × 2 units Real-time clock (RTCA) Independent watchdog timer (IWDTa): 14 bit × 1 channel 8-bit timer (TMR): (8 bit × 2 channels) × 2 units 	
	Communication functions	 Serial communications interface (SCIe): 100-pin [7 channels], 64-pin [5 channels] Serial communications interface (SCIf): 1 channel I2C bus interface (RIIC): 1 channel Serial peripheral interface (RSPI): 1 channel USB 2.0 Full Speed (USBc): [1 channel, USB 2.0 Full Speed (12 Mbps), Low Speed (1.5 Mbps) H/F/OTG] Serial sound interface (SSI): 1 channel IrDA interface: 1 channel 	
	Touch key functions	 Capacitive Touch Sensing Unit (CTSU) × 12 channels, 36 keys (max. input keys when configuring 12 ch in the 6 ch × 6 ch matrix state using mutual-capacitance.) Self-capacitance and mutual capacitance are supported. 	
	Analog functions	 12-bit A/D converter (S12ADb): 100-pin [17 channels], 64-pin [11 channels] 	

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		 12-bit D/A converter: 2 channels (R12DAA) Comparator: 2 channels (CMPBa) 	
	LCD controller/ driver (LCDC)	 Internal voltage boosting method, capacitor split method, and external resistance division method are switchable. Segment signal output × common signal output: 100-pin: 40 com. × 4 seg., 36 com. × 8 seg., 64-pin: 20 seg. × 4 com., 16 seg. × 8 com 	
	Safety functions	 Clock Frequency Accuracy Measurement Circuit (CAC) Data Operation Circuit (DOC) 14 bits Independent Watchdog Timer (IWDTa) CRC Calculator (CRC) 	
	Clock generation circuit	 Main clock oscillator Sub-clock oscillator Low-speed on-chip oscillator (LOCO) High-speed on-chip oscillator (HOCO) Dedicated on-chip oscillator for the IWDT USB-dedicated PLL frequency synthesizer USB-dedicated PLL frequency synthesizer 	
	Others	 Event Link Controller (ELC) Multi-function Pin Controller (MPC) Power-on Reset Circuit (POR) Voltage Detection Circuit (LVD) 	

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	Temperature Sensor (TEMPSA)		
On-chip debugging function	Yes (with trace function)		
Low power consumption modes	 3 modes Sleep mode Deep sleep mode Software standby mode 		
Packages	 100-pin LFQFP (PLQP0100KB-A) 14 × 14 mm, 0.50 mm pitch 100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65 mm pitch 64-pin LFQFP (PLQP0064KB-A) 10 × 10 mm, 0.50 mm pitch 		

(Remarks)

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