**March 25, 2013**

## R-Car H2 Product Specifications

| Item | Specification | | |
|---|---|---|---|
| Product number | R8A7790x | | |
| Power supply voltage | 3.3/1.8 V (IO), 1.5/1.35 V (DDR3), 1.0 V (Core) | | |
| CPU core | ARM®CortexTM-A15 Quad | ARM®CortexTM-A7 Quad (device option) | SH-4A core (device option) |
| Cache memory | L1 Instruction cache: 32 KB<br>L1 Operand cache: 32 KB<br>L2 Cache: 2 MB | L1 Instruction cache: 32 KB<br>L1 Operand cache: 32 KB<br>L2 cache: 512 KB | Instruction cache: 32 KB<br>Operand cache: 32 KB |
| External memory | DDR3-SDRAM<br>Maximum operating frequency: 800 MHz<br>Data bus width: 32 bits × 2 ch (6.4 GB/s × 2) | | |
| Expansion bus | Flash ROM and SRAM,<br>Data bus width: 8 or 16 bits | | |
| | PCI Express 2.0 (1 lane) | | |
| Graphics | PowerVR Series6 G6400 (3D) | | |
| | Renesas graphics processor (2D) | | |
| Video | Display Out × 3 ch (2 ch: LVDS, 1 ch: RGB888) | | |
| | Video Input × 4 ch | | |
| | Video codec module (H.264/AVC, MPEG-4, VC-1) | | |
| | IP conversion module | | |
| | JPEG accelerator | | |
| | TS Interface × 2 ch | | |
| | Video image processing (color conversion, image expansion, reduction, filter processing) | | |
| | Distortion compensation module (image renderer) × 4 ch | | |

| Item | Specification |
|---|---|
| | High performance Real-time Image recognition processor (IMP-X4) (device option) |
| Audio | Audio DSP |
| | Sampling rate converter × 10 ch |
| | Serial sound interface × 10 ch |
| | MOST DTCP |
| Storage Interface | USB 3.0 Host interface × 1 port (wPHY) |
| | USB 2.0 Host interface × 3 port (wPHY) |
| | SD Host interface × 4 ch (SDXC, UHS-I) |
| | Multimedia card interface × 2 ch |
| | Serial ATA interface × 2 ch |
| In car network and automotive peripherals | Media local bus (MLB) Interface × 1 ch (6pin / 3pin interface selectable) |
| | CAN Interface × 2 ch |
| | IEBus Interface |
| | GPS baseband module (Galileo, GLONASS) (device option) |
| | Ethernet controller AVB (IEEE802.1BA, 802.1AS, 802.1Qav and IEEE1722, GMII/MII, without PHY) |
| Security | Crypto engine (AES, DES, Hash, RSA) |
| | SecureRAM |
| Other peripherals | DMA controller<br>LBSC DMAC: 3 ch / SYS-DMAC: 30 ch / RT-DMAC: 3 ch / Audio-DMAC: 26 ch / Audio (peripheral)-DMAC: 29 ch |
| | 32bit timer × 12 ch |
| | PWM timer × 7 ch |
| | I2C bus interface × 8 ch |
| | Serial communication interface (SCIF) × 10 ch |
| | Quad serial peripheral interface (QSPI) × 1 ch (for boot) |
| | Clock-synchronized serial interface (MSIOF) × 4 ch (SPI/IIS) |
| | Ethernet controller (IEEE802.3u, RMII, without PHY) |

| Item | Specification |
|---|---|
| | Interrupt controller (INTC) |
| | Clock generator (CPG) with built-in PLL |
| | On chip debugger interface |
| Low power mode | Dynamic Power Shutdown (CPU core, 3D, IMP)<br>AVS and DVFS function<br>DDR-SDRAM power supply backup mode |
| Package | 831 pin Flip Chip BGA (27 mm × 27 mm) |
| Development environment | ICE for ARM CPU available from different vendors. |
| Evaluation board | A user system development reference platform offering the following features is also available, enabling the users to carry out efficient system development.<br>(1) Includes car information system-oriented peripheral circuits, providing users with an actual device verification environment.<br>(2) Can be used as a software development tool for application software, etc.<br>(3) Allows easy implementation of custom user functions. |
| Software Platform | Support OS: QNX® Neutrino® RTOS, Windows® Embedded Automotive, Linux<br>Wide variety of H.264, MPEG-4 and VC-1 for video compliant with OpenMAX IL I/F in addition to BSPs compliant with OSs standard API are available to realize complete system concept. |