

RENESAS SEMICONDUCTOR RELIABILITY REPORT

GROUP : RA0L1
DEVICE : R7FA0L1XXX
APPLICATION : Consumer / Industry

Quality Assurance Div.
Renesas Electronics Corporation

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Table. Reliability test results (QFP)

Test Items	Reference	Test Conditions	Results Failure/Size	Comment
High Temperature Operating Life (HTOL)	JESD22-A108	Ta=125 °C, Vccmax, 1000 hrs	0/22	
High Temperature Storage Life (HTSL)	JESD22-A103	Ta=150 °C, 1000 hrs	0/22	
Temperature Humidity bias (THB) (*1)	JESD22-A101	Ta=85 °C, RH=85 %, Vccmax, 1000 hrs	0/22	
Temperature Cycling (TC) (*1)	JESD22-A104	Ta=-65 °C to 150 °C , 300 cycles	0/22	
Latch-Up (LU)	JESD78	Pulse Current Injection, I=+/-150 mA	0/3	
Electrostatic discharge (ESD-HBM)	JS-001	1.5 kΩ, 100 pF, +/-2000 V, 1 time	0/3	Class: 2
Electrostatic discharge (ESD-CDM)	JS-002	+/-500V,1time	0/3	Class: C2a
Solderability (SD)	J-STD-002	245 °C, 5 s, Solder coverage ≥95 %	0/5	
Resistance to Soldering Heat (PC)	JESD22-A113, J-STD-020	MSL3(Moisture Sensitivity Level 3)	0/22	

*1) With preconditioning per JESD22-A113, MSL 3

·It is tested to confirm that all the samples are satisfied with an individual product specification.

Note :

Basically qualification tests were performed using a representative product with the same wafer process and the same package structure .

Table. Reliability test results (QFN)

Test Items	Reference	Test Conditions	Results Failure/Size	Comment
High Temperature Operating Life (HTOL)	JESD22-A108	Ta=125 °C, Vccmax, 1000 hrs	0/22	
High Temperature Storage Life (HTSL)	JESD22-A103	Ta=150 °C, 1000 hrs	0/22	
Temperature Humidity bias (THB) (*1)	JESD22-A101	Ta=85 °C, RH=85 %, Vccmax, 1000 hrs	0/22	
Temperature Cycling (TC) (*1)	JESD22-A104	Ta=-65 °C to 150 °C , 300 cycles	0/22	
Latch-Up (LU)	JESD78	Pulse Current Injection, I=+/-150 mA	0/3	
Electrostatic discharge (ESD-HBM)	JS-001	1.5 kΩ, 100 pF, +/-2000 V, 1 time	0/3	Class: 2
Electrostatic discharge (ESD-CDM)	JS-002	+/-500V,1time	0/3	Class: C2a
Solderability (SD)	J-STD-002	245 °C, 5 s, Solder coverage ≥95 %	0/5	
Resistance to Soldering Heat (PC)	JESD22-A113, J-STD-020	MSL3(Moisture Sensitivity Level 3)	0/22	

*1) With preconditioning per JESD22-A113, MSL 3

·It is tested to confirm that all the samples are satisfied with an individual product specification.

Note :

Basically qualification tests were performed using a representative product with the same wafer process and the same package structure .

Table. Reliability test results (SOP)

Test Items	Reference	Test Conditions	Results Failure/Size	Comment
High Temperature Operating Life (HTOL)	JESD22-A108	Ta=125 °C, Vccmax, 1000 hrs	0/22	
High Temperature Storage Life (HTSL)	JESD22-A103	Ta=150 °C, 1000 hrs	0/22	
Temperature Humidity bias (THB) (*1)	JESD22-A101	Ta=85 °C, RH=85 %, Vccmax, 1000 hrs	0/22	
Temperature Cycling (TC) (*1)	JESD22-A104	Ta=-65 °C to 150 °C , 300 cycles	0/22	
Latch-Up (LU)	JESD78	Pulse Current Injection, I=+/-150 mA	0/3	
Electrostatic discharge (ESD-HBM)	JS-001	1.5 kΩ, 100 pF, +/-2000 V, 1 time	0/3	Class: 2
Electrostatic discharge (ESD-CDM)	JS-002	+/-500V,1time	0/3	Class: C2a
Solderability (SD)	J-STD-002	245 °C, 5 s, Solder coverage ≥95 %	0/5	
Resistance to Soldering Heat (PC)	JESD22-A113, J-STD-020	MSL3(Moisture Sensitivity Level 3)	0/22	

*1) With preconditioning per JESD22-A113, MSL 3

•It is tested to confirm that all the samples are satisfied with an individual product specification.

Note :

Basically qualification tests were performed using a representative product with the same wafer process and the same package structure .

The failure rate of the device in an actual use condition can be estimated by the below procedure.

•Equation for the failure rate estimation (λ)

$$\lambda = \lambda_b \times \pi T \text{ (FIT)}$$

① Unique failure rate (λ_b)

$$\lambda_b = 4.1 \text{ FIT}$$

Unique failure rate at $T_a = 55^\circ\text{C}$ using 60 % confidence level.

② Temperature term (πT)

$$\pi T = \exp\{11600 \times E_a \times (1/(273+55) - 1/(273+T_a))\}$$

E_a : Activation energy (eV)

T_a : Ambient temperature ($^\circ\text{C}$)

πT simplified chart as $E_a = 0.7 \text{ eV}$												
T_a ($^\circ\text{C}$)	40	50	55	60	65	70	75	80	85	90	100	110
πT	0.31	0.68	1	1.45	2.08	2.95	4.15	5.77	7.96	10.88	19.82	34.99

•MTTF (Mean Time To Failure)

$$MTTF = 1/\lambda$$

Reference about Renesas package code

Package type		Package code *1
Lead type plastic package	QFP	PxQP
	SOP	PxSP
Non-lead type plastic package	QFN	PxQN
Grid array type plastic package	BGA	PxBG
	LGA	PxLG
Wafer level chip scale package	WLCSP	SxBG

*1. First four digit

Table. Product list

No	Group	Product part number	Package code	No	Group	Product part number	Package code
1	RA0L1	R7FA0L1053CFJ	PLQP0032G*	51			
2	RA0L1	R7FA0L1054CFJ	PLQP0032G*	52			
3	RA0L1	R7FA0L1073CFJ	PLQP0032G*	53			
4	RA0L1	R7FA0L1074CFJ	PLQP0032G*	54			
5	RA0L1	R7FA0L1053CFL	PLQP0048K*	55			
6	RA0L1	R7FA0L1054CFL	PLQP0048K*	56			
7	RA0L1	R7FA0L1073CFL	PLQP0048K*	57			
8	RA0L1	R7FA0L1074CFL	PLQP0048K*	58			
9	RA0L1	R7FA0L1053CNE	PWQN0048K*	59			
10	RA0L1	R7FA0L1054CNE	PWQN0048K*	60			
11	RA0L1	R7FA0L1073CNE	PWQN0048K*	61			
12	RA0L1	R7FA0L1074CNE	PWQN0048K*	62			
13	RA0L1	R7FA0L1053CNH	PWQN0032K*	63			
14	RA0L1	R7FA0L1054CNH	PWQN0032K*	64			
15	RA0L1	R7FA0L1073CNH	PWQN0032K*	65			
16	RA0L1	R7FA0L1074CNH	PWQN0032K*	66			
17	RA0L1	R7FA0L1053CNK	PWQN0024K*	67			
18	RA0L1	R7FA0L1054CNK	PWQN0024K*	68			
19	RA0L1	R7FA0L1073CNK	PWQN0024K*	69			
20	RA0L1	R7FA0L1074CNK	PWQN0024K*	70			
21	RA0L1	R7FA0L1053CSC	PLSP0020J*	71			
22	RA0L1	R7FA0L1054CSC	PLSP0020J*	72			
23	RA0L1	R7FA0L1073CSC	PLSP0020J*	73			
24	RA0L1	R7FA0L1074CSC	PLSP0020J*	74			
25				75			
26				76			
27				77			
28				78			
29				79			
30				80			
31				81			
32				82			
33				83			
34				84			
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40				90			
41				91			
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43				93			
44				94			
45				95			
46				96			
47				97			
48				98			
49				99			
50				100			