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RENESAS SEMICONDUCTOR RELIABILITY REPORT

New Product release

DEVICE: RA6W1(A-C)

APPLICATION: Consumer/Industry

Quality Assurance Div.
Renesas Electronics Corporation

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Table. Reliability test results QFN package

Test Items	Reference	Test Conditions	Number of Lots	Number of Samples	Results Failure/Size	Comments
High Temperature Operating Life (HTOL)	JESD22-A108, JESD85	Ta=125C, Vccmax, 1000 hrs	3	77	0/231	
High Temperature Storage Life (HTSL)	JESD22-A103	Ta=150C, 1000 hrs	3	25	0/75	
Latch-Up (LU)	JESD78	Pulse Current Injection, I=+/-100 mA	1	3	0/3	QBS with WLCSP result
Human Body Model ESD (ESD-HBM)	JS-001	1.5 kΩ, 100 pF, +/-2000 V, 1 time	1	3	0/3	QBS with WLCSP result
Charged Device Model ESD (ESD-CDM)	JS-002	+/-500V,1time	1	3	0/3	Class: C2
Highly Accelerated Temperature and Humidity Stress (HAST)	JESD22-A110	Ta=110C, RH=85%, Vccmax, 264 hrs	3	25	0/75	*1
Temperature Cycling (TC)	JESD22-A104	Ta=-55C to 125C , 700 cycles	3	25	0/75	*1
Solderability (SD)	J-STD-002	245C, 5 s, Solder coverage ≥95 %	1	15	0/15	
Resistance to Soldering Heat (PC)	JESD22-A113, J-STD-020	MSL3(Moisture Sensitivity Level 3)	3	50	0/150	
Cu Bump Shear	JESD22-B116	Ppk >1.66 or Cpk > 1.33	1	5	0/5	
Physical Dimensions	Package outline drawing	Ppk >1.66 or Cpk > 1.33	1	10	0/10	

*1 With preconditioning per JESD22-A113, MSL 3

·It is tested to confirm that all the samples are satisfied with an individual product specification.

Note :

Basically qualification tests were performed using a representative product with the same wafer process and the same package structure .

Table. Reliability test results WLCSP package

Test Items	Reference	Test Conditions	Number of Lots	Number of Samples	Results Failure/Size	Comments
High Temperature Operating Life (HTOL)	JESD22-A108, JESD85	Ta=125C, Vccmax, 1000 hrs	3	77	0/231	QBS with QFN result
High Temperature Storage Life (HTSL)	JESD22-A103	Ta=150C, 1000 hrs	3	25	0/75	
Latch-Up (LU)	JESD78	Pulse Current Injection, I=+/-100 mA	1	3	0/3	Pass RT and 85°C
Human Body Model ESD (ESD-HBM)	JS-001	1.5 kΩ, 100 pF, +/-2000 V, 1 time	1	3	0/3	
Charged Device Model ESD (ESD-CDM)	JS-002	+/-450V,1time	1	3	0/3	Class: C1
Temperature Cycling (TC)	JESD22-A104	Ta=-55C to 125C , 700 cycles	3	25	0/75	*1
Unbiased Highly Accelerated Stress Test (UHST)	JESD22-A118 & A102	Ta=130C, RH=85%, 96 hrs	3	25	0/75	*1
Solder Ball Shear (SBS)	JESD22-B117	Ppk >1.66 or Cpk > 1.33	1	5	0/5	
Solderability (SD)	J-STD-002	Pre-condition C, Solder coverage ≥95 %	1	20	0/20	
Resistance to Soldering Heat (PC)	JESD22-A113, J-STD-020	MSL1(Moisture Sensitivity Level 1)	3	50	0/150	
Physical Dimensions	Package outline drawing	Ppk >1.66 or Cpk > 1.33	1	30	0/30	

*1 With preconditioning per JESD22-A113, MSL 1

·It is tested to confirm that all the samples are satisfied with an individual product specification.

Note :

Basically qualification tests were performed using a representative product with the same wafer process and the same package structure .

Calculation method of standard failure rate

Operating reliability is decided by inherent reliability of device and environment condition of use (See below)

·Calculation method of standard failure rate (λ)

$$RELIA \lambda = \lambda_b \times \pi T \quad (FIT)$$

(2)Temperature parameter

(1)Basic failure rate

(1)Basic failure rate(λ_b)

λ_b : 51.1

Unique failure rate at $T_a=55^\circ C$ using 60% confidence level.

(2)Temperature parameter (πT)

$$\pi T = \exp \{ 11600 \times E_a \times (1/(273 +55) - 1/(273 +T_a)) \}$$

E_a : Activation energy
 T_a : Ambient temperature

πT simplified chart											
$E_a(eV)$	$T_a (^\circ C)$	40	55	60	65	70	75	80	90	100	110
0.7	πT	0.31	1.00	1.45	2.08	2.95	4.15	5.77	10.88	19.82	34.99

(3)MTTF (Mean Time To Failure)

$$MTTF = 1 / \lambda$$

Calculation standard

Confidence level 60 %

Standard temperature (T_e) 55 °C

Use within recommended conditions