



Report No. APR-25-H0064
Date: Mar. 19, 2025

RENESAS SEMICONDUCTOR RELIABILITY REPORT

APPLICATION: High Quality

SERIES: REXFET-1 ANM3

DEVICE: RBA300N10EHPF-5UA02#GB0

Quality Assurance Div.
Renesas Electronics Corporation

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Q101 Qualification Test Results

[Note : Basically qualification tests were performed using a representative product with the same wafer process and the same package structure .]

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results (Fail of Total)	Comments: (N/A =Not Applicable)
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TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS

PC	A1	JESD22-A113 J-STD-020	SMD only; Moisture Preconditioning for HAST/H3TRB,UHAST/AC,TC,IOL/PTC.	3	308	924	0 of 924	-
HAST	A2	JESD22-A110	Ta=130°C, RH=85%, VDSS=Maximum rating, 96h	-	-	-	-	See H3TRB.
H3TRB	A2 alt	JESD22-A101	Ta=85°C, 85%RH, VDSS=Maximum rating, 1,000h	3	77	231	0 of 231	-
UHAST	A3	JESD22-A118 or A101	Ta=130°C, RH=85%, 96h	3	77	231	0 of 231	-
AC	A3 alt	JESD22-A102	Ta=121°C, 100%RH, 96h	-	-	-	-	See UHAST.
TC	A4	JESD22-A104 Appendix 6	Ta=-55°C to 150°C, 1,000cycles	3	77	231	0 of 231	-
TCHT	A4a	JESD22-A104 Appendix 6	TC Hot Test.	-	-	-	-	See TCDT.
TCDT	A4a alt	JESD22-A104 Appendix 6 J-STD-035	TC Delamination Test.	3	77	231	0 of 231	-
IOL	A5	MIL-STD-750 Method 1037	ΔTc=100°C, 15,000cycles	3	77	231	0 of 231	-
PTC	A5 alt	JESD22-A105	Power Temperature Cycling.	-	-	-	-	See IOL.

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

HTRB	B1	MIL-STD-750-1 M1039	Tch = 175°C, VDSS=Maximum rating, 1,000h	3	77	231	0 of 231	-
ACBV	B1a	MIL-STD-750-1 M1040 Test condition A	AC blocking voltage.	-	-	-	-	N/A Thyristors Only.
SSOP	B1b	MIL-STD-750-1 M1038 condition B (Zeners)	Steady State Operational.	-	-	-	-	N/A Voltage Regulators (Zeners) Only.
HTGB	B2	JESD22-A108	Tch = 175°C, VGSS=+20V, 1,000h	3	77	231	0 of 231	-

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Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results (Fail of Total)	Comments: (N/A =Not Applicable)
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TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

DPA	C1	AEC Q101-004 Section4	Random sample of parts that have successfully completed H3TRB or HAST and TC.	3	4	12	0 of 12	-
PD	C2	JEDEC JESD22-B100	Physical Dimensions.	1	30	30	0 of 30	-
WBP	C3	MIL-STD-750-2 Method 2037	Wire Bond Pull.	1bond	10parts	10bonds	0 of 10bonds	-
WBS	C4	AEC Q101-003 JESD22-B116	Wire Bond Shear Test.	1bond	10parts	10bonds	0 of 10bonds	-
DS	C5	MIL-STD-750-2 Method 2017	Die Shear.	1	5	5	0 of 5	-
TS	C6	MIL-STD-750-2 Method 2036	Terminal Strength.	-	-	-	-	N/A SMD
RTS	C7	JESD22-B107	Resistance to Solvents.	-	-	-	-	N/A laser etched parts
RSH	C8	JESD22-A111 (SMD)	Resistance to Solder Heat.	-	-	-	-	N/A Wave solder deprecated.
TR	C9	JESD24-3, 24-4, 24-6 as appropriate	Thermal Resistance.	1	10	10	0 of 10	-
SD	C10	JEDEC J-STD-002	Solderability: (>95% coverage)	3	10	30	0 of 30	-
WG	C11	AEC Q005	see AEC-Q005	-	-	-	Pass	Performed on product TEG with test method based on JESD201.
CA	C12	MIL-STD-750-2 Method 2006	Constant Acceleration.	-	-	-	-	N/A hermetic packaged devices only
VVF	C13	JESD22-B103	Vibration Variable Frequency.	-	-	-	-	N/A hermetic packaged devices only
MS	C14	JESD22-B104	Mechanical Shock.	-	-	-	-	N/A hermetic packaged devices only
HER	C15	JEDEC JESD22-A109	Hermeticity.	-	-	-	-	N/A hermetic packaged devices only

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

DI	D1	AEC Q101-004 Section3	Dielectric Integrity.	1	5	5	0 of 5	Confirmed by process TEG
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Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results (Fail of Total)	Comments: (N/A =Not Applicable)
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TEST GROUP E – ELECTRICAL VERIFICATION TESTS

EV	E0	JESD22-B101	External Visual.	All	All	All	0 of All	-
TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test.	All	All	All	0 of All	-
PV	E2	Individual AEC user specification	Parametric Verification.	3	25	75	0 of 75	-
ESDH	E3	AEC Q101-001	Electrostatic Discharge, Human Body Model.	1	30	30	0 of 30	HBM:C:100pF,R:1.5KΩ,2000V↑
ESDC	E4	AEC Q101-005	Electrostatic Discharge, Charged Device Model.	1	30	30	0 of 30	CDM:±1000V↑
UIS	E5	AEC Q101-004 Section2	UNCLAMPED INDUCTIVE SWITCHING.	1	5	5	0 of 5	-
SC	E6	AEC Q101-006	Short Circuit Characterization.	-	-	-	-	N/A For smart power parts only.

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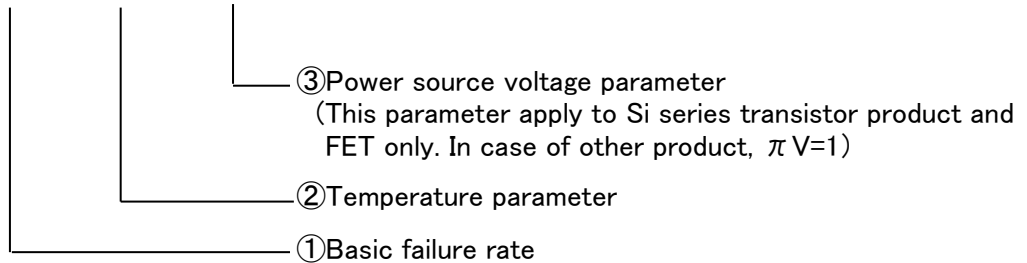
Calculation method of standard failure

·Calculation method of standard failure rate

Operating reliability is decided by inherent reliability of device and environment condition of use (See below).

·Calculation method of standard failure rate (λ)

$$\lambda = \lambda_b \times \pi T \times \pi V \quad (\text{fit})$$



①Basic failure rate(λ_b)

Product Name: RBA300N10EHPF-5UA02 λ_b : 0.59 (Fit)

②Temperature parameter(π_T)

$$\pi T = \exp(11600 \times Ea \times \left(\frac{1}{273 + 55} - \frac{1}{273 + Ta(j)} \right))$$

E_a : Activation energy

T_j(T_{ch}) : junction temperature

		π T simplified chart									
E _a (eV)	T _j (T _{ch})	40	55	60	65	70	75	80	90	100	110
0.8	π T	0.26	1.00	1.53	2.31	3.45	5.08	7.42	15.30	30.37	58.14

③Power source voltage parameter(π_V) (Si series transistor products,FET only)

$$S = \frac{\text{supply voltage (VCE or VDS)}}{\text{absolute maximum voltage (VCEs or VDSS)}}$$

$$S > 0.2 \quad \pi V = \exp(2.86 \times S - 2.29)$$

$$S \leq 0.2 \quad \pi V = 0.18$$

④MTTF (Mean Time To Failure)

MTTF and failure rate have the following relationship in the contingent failure domain

$$MTTF = \frac{1}{\lambda} \times 10^9 \quad (\text{h})$$

$$MTTF * = 1,694,915,254 \quad (\text{h})$$

(* π_T=1, π_V=1)

Calculation standard

·Confidence level 60% ·Standard temperature T_j = 55°C ·Use within recommended conditions