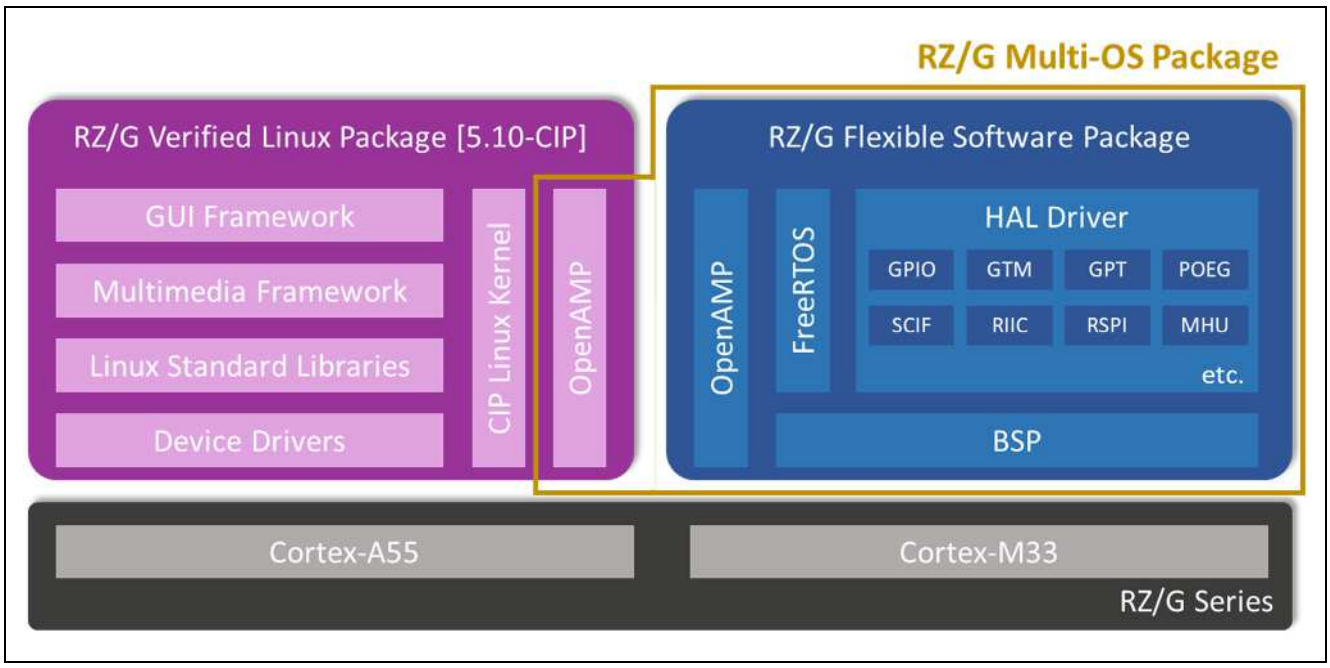
RZ/G3S

Quick Start Guide for RZ/G3S Multi-OS Package

Introduction

This document outlines the procedure for integrating the RZ/G Multi-OS Package into the RZ/G Verified Linux Package (referred to as VLP) for the RZ/G3S. By integrating the Multi-OS Package, users can efficiently establish a Multi-OS environment wherein Linux operates on the Cortex®-A55 and FreeRTOS/BareMetal runs on the Cortex-M33, with support for Inter-Processor Communication between these CPU cores.

This package requires the RZ/G Flexible Software Package (FSP) for an RTOS/BareMetal environment. The figure below illustrates the software stack for integrating the RZ/G Multi-OS Package with the RZ/G3S:



Here are brief descriptions of each component related to RZ/G Multi-OS Package:

- RZ/G FSP
  This software package consists of production ready peripheral drivers, FreeRTOS and portable middleware stacks and best in-case HAL drivers with low memory footprint.
- OpenAMP
  The framework includes the software components required for Asymmetric Multiprocessing (AMP) systems, such as Inter-Processor Communication.

Target Device

RZ/G3S

Contents

1. Specifications

Table 1-1 lists the on-chip peripheral modules to be used in this package.

Table 1-1 Peripheral modules to be used in this package

Peripheral module	Usage
Message Handling Unit (MHU)	Configure Inter-Processor Interrupt.
Serial Communications Interface with FIFO (SCIFA)	Perform standard serial communications sending and receiving console messages.
Interrupt controller (INTC)	Handle the following types of interrupts as shown below for example: • Processors should receive interrupts during buffered serial communications. • MHU module fires Inter-Processor Interrupt.
General Purpose Input Output (GPIO)	Configure I/O lines used by serial communications.
General Timer (GTM)	Configure the tick for FreeRTOS.

2. Verified Operation Conditions

Table 2-1 shows the verified operation conditions.

Table 2-1 Verified Operation Conditions

Item	Contents
Integrated Development Environment	e^2 studio 2025-07
Toolchain	GNU Arm Toolchain 13.3.Rel1 AArch32 bare-metal target (arm-none-eabi)
Dependent Software	• RZ/G Flexible Software Package (FSP) v3.1.0 • RZ/G Verified Linux Package v3.0.7

3. Sample Program Setup

3.1 Flexible Software Package Setup

Multi-OS Package expects RZ/G Flexible Software Package (FSP) to be installed in advance. For details on the installation, please refer to Getting Started with Flexible Software Package.

3.2 Integration of Multi-OS Package related stuff

This section describes how to integrate OpenAMP related stuff to RZ/G Verified Linux Package [5.1-CIP] (hereinafter referred to as VLP). The steps are based on **SMARC EVK of RZ/G3S Linux Start-up Guide** (hereinafter referred to as **Linux Start-up Guide**) included in **RZ/G VLP v3.0.7**.

1. Follow the procedure stated from the beginning of **2.2 Building Images** to **(3) Add layers** of **Linux Start-up Guide**.
2. Download Multi-OS Package (r01an5869ej0300-rzg-multi-os-pkg.zip) to a working directory and run the commands stated below:

```
cd ~/rzg_vlp_<pkg ver>
$ unzip <Multi-OS Dir>/r01an5869ej0300-rzg-multi-os-pkg.zip
$ tar zxvf r01an5869ej0300-rzg-multi-os-pkg/meta-rz-features_multi-os_v3.0.0.tar.gz
```

Here, <Multi-OS Dir> indicates the path to the directory where Multi-OS Package is placed.

3. Add the layer for Multi-OS Package.

```
$ cd build
$ bitbake-layers add-layer ../meta-rz-features/meta-rz-multi-os/meta-rzg3s
```

(Optional for remoteproc support)

4. Apply the modification stated below to **meta-rz-features/meta-rz-multi-os/meta-rzg3s/recipes-kernel/linux/linux-renesas_5.10.bbappend** for enabling remoteproc support:

```
$ FILESEXTRAPATHS_prepend := "${THISDIR}/${PN}:"
$ ENABLE_REMOTEPROC = “1”
```

5. Start a build as described in **(5) Start a build** of **2.2 Building Images** as shown below:

```
$ MACHINE=smarc-rzg3s bitbake core-image-<target>
```

For details on the allowable value of <target>, please refer to **Linux Start-up Guide**.

3.3 Note for integration

The peripherals which are NOT enabled enter Module Standby Mode after Linux kernel is booted up. That means the peripherals used on CM33 side might stop working at that time. To avoid such a situation, Multi-OS Package incorporates the patch below:

- 0001-Set-SCIF1-and-OSTM1-OSTM2-as-critical-clock.patch

This patch prevents SCIF channel1, GTM channel 1 and GTM channel 2 used in RPMsg demo program from entering Module Standby Mode. If you have any other peripherals which you would like to stop entering Module Standby implicitly, please update the patch as shown below:

```
diff --git a/drivers/clk/renesas/r9a08g045-cpg.c b/drivers/clk/renesas/r9a08g045-cpg.c
index 33a204fbe25c..dba2b4925e66 100644
--- a/drivers/clk/renesas/r9a08g045-cpg.c
+++ b/drivers/clk/renesas/r9a08g045-cpg.c
@@ -381,6 +381,9 @@ static const unsigned int r9a08g045_crit_mod_clks[] __initconst = {
  MOD_CLK_BASE + R9A08G045_IA55_CLK,
  MOD_CLK_BASE + R9A08G045_DMAC_ACLK,
  MOD_CLK_BASE + R9A08G045_VBAT_BCLK,
+ MOD_CLK_BASE + R9A08G045_SCIF1_CLK_PCK,
+ MOD_CLK_BASE + R9A08G045_OSTM1_PCLK,
+ MOD_CLK_BASE + R9A08G045_OSTM2_PCLK,
+ MOD_CLK_BASE + R9A08G045_xxxx,
 };

 const struct rzg2l_cpg_info r9a08g045_cpg_info = {
```

With respect to the allowable value for **xxxx** above, please refer to the source code below:

- https://github.com/renesas-rz/rz_linux-cip/blob/rz-5.10-cip54/drivers/clk/renesas/r9a08g045-cpg.c#L213-L298

3.4 Deployment of RZ/G VLP

With respect to the deployment of Linux kernel, device tree and root filesystem for RZ/G3S, please refer to **Linux Start-up Guide**.

4. Sample Program Invocation on RZ/G3S

4.1 Hardware Setup

1. Connect J-Link to RZ/G3S SMARC EVK. For details, please refer to Getting Started with Flexible Software Package.
2. Connect Pmod USBUART to the upper side of PMOD 3A connector of Smarc EVK as shown below for securing the console for sample program.

Figure 4-1. Connection between Pmod USBUART and RZ/G3S SMARC EVK

4.2 CM33 Sample Program Setup

Here are the procedures for setting up the sample program running on CM33:

1. Extract **r01an5869ej0300-rzg-multi-os-pkg.zip** on your development PC.
2. Extract **<device>_rpmsg_<com_type>_demo.zip** included in **r01an5869ej300-rzg-multi-os-pkg**. Here, <device> should be any of **rzg3s_cm33** or **rzg3s_cm33_fpu**. Also, <com_type> should either of **linux-rtos** or **rtos-rtos**.
3. Open e^2 studio 2025-07 and click **File** > **Import**.
4. Double-click **General** and select **Existing Projects into Workspace** as shown in Figure 4-2:

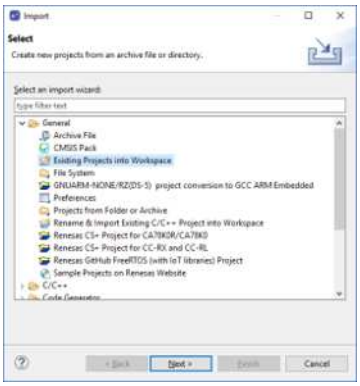


Figure 4-2. Import sample project (1)

5. Input the path to the directory of sample project you would like to import to **Select root directory**, press **Enter** key and click **Finish** button.

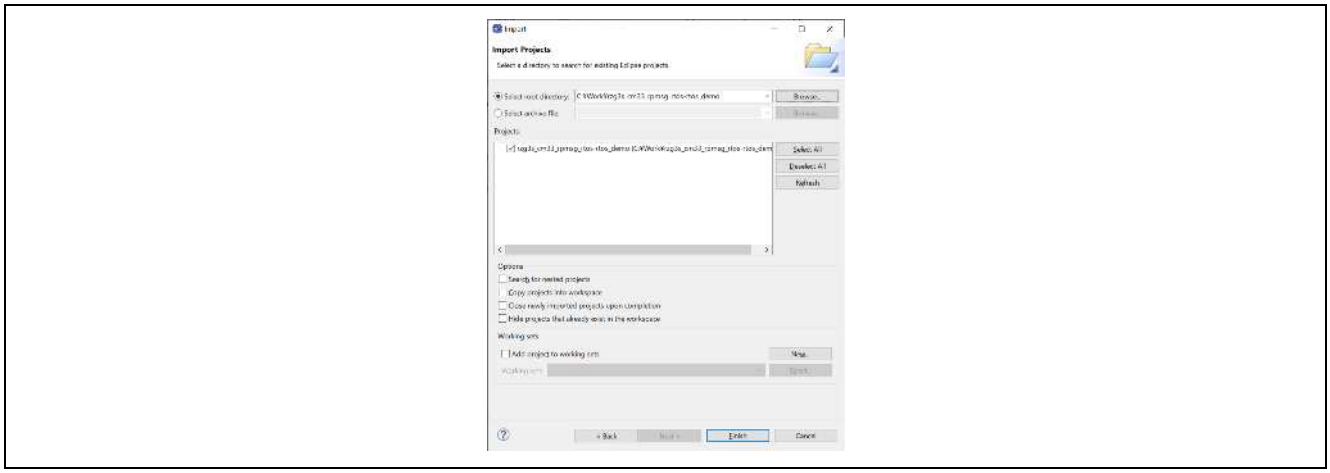


Figure 4-3. Import sample project (2)

(Optional)

6. By default, RPMsg channel 0 is configured to be used on CM33. If you would like to change the channel, you need to open the property of **MainTask#0** on FSP Smart Configurator, specify the channel number you would like to use for **Thread Context** and push **Generate Project Content** button. If **Generate Project Content** pop-up is shown, click **Proceed** to reflect the changes to source code.

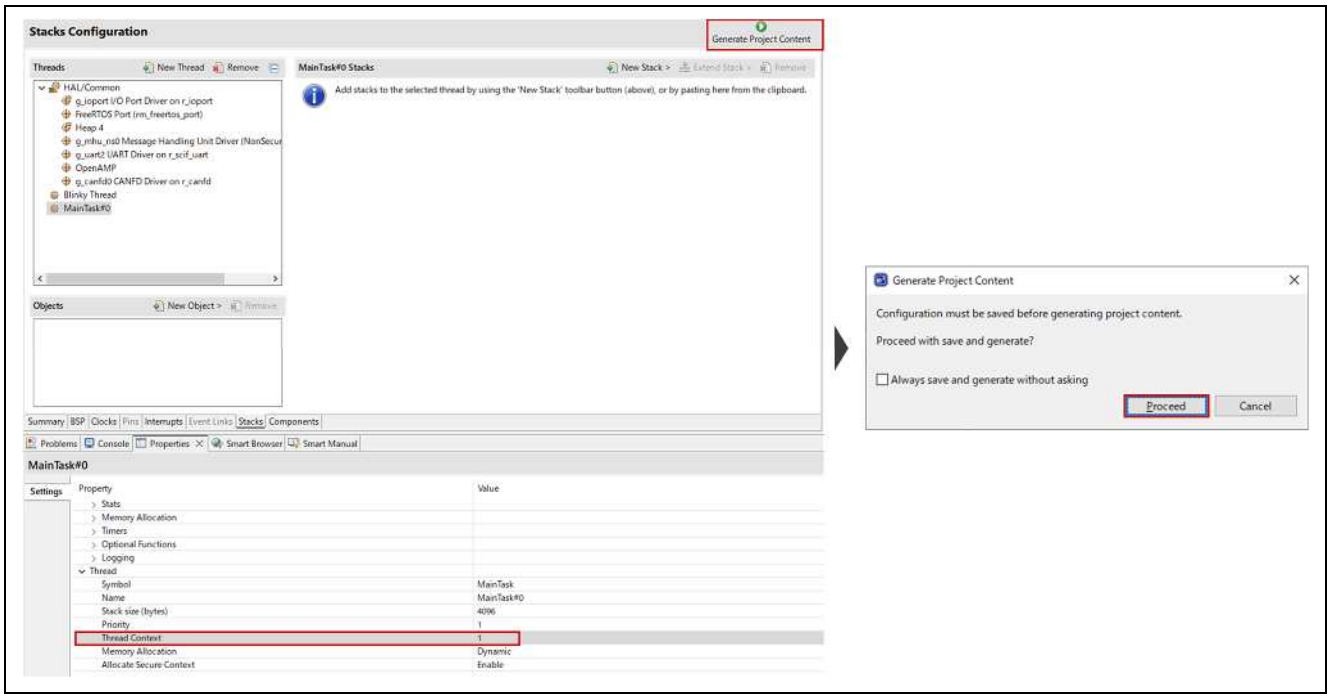


Figure 4-4. RPMsg Channel Setting

(Optional for remoteproc support)

7. Change the value for **ENABLE_REMOTEPROC** defined in **platform_info.h** from 0 to 1 as shown below:

```
#define ENABLE_REMOTEPROC (1U)
```

(Optional for CM33 cold boot support)

8. Configure **Launch Cortex-A55(core0)** as **Enabled**.

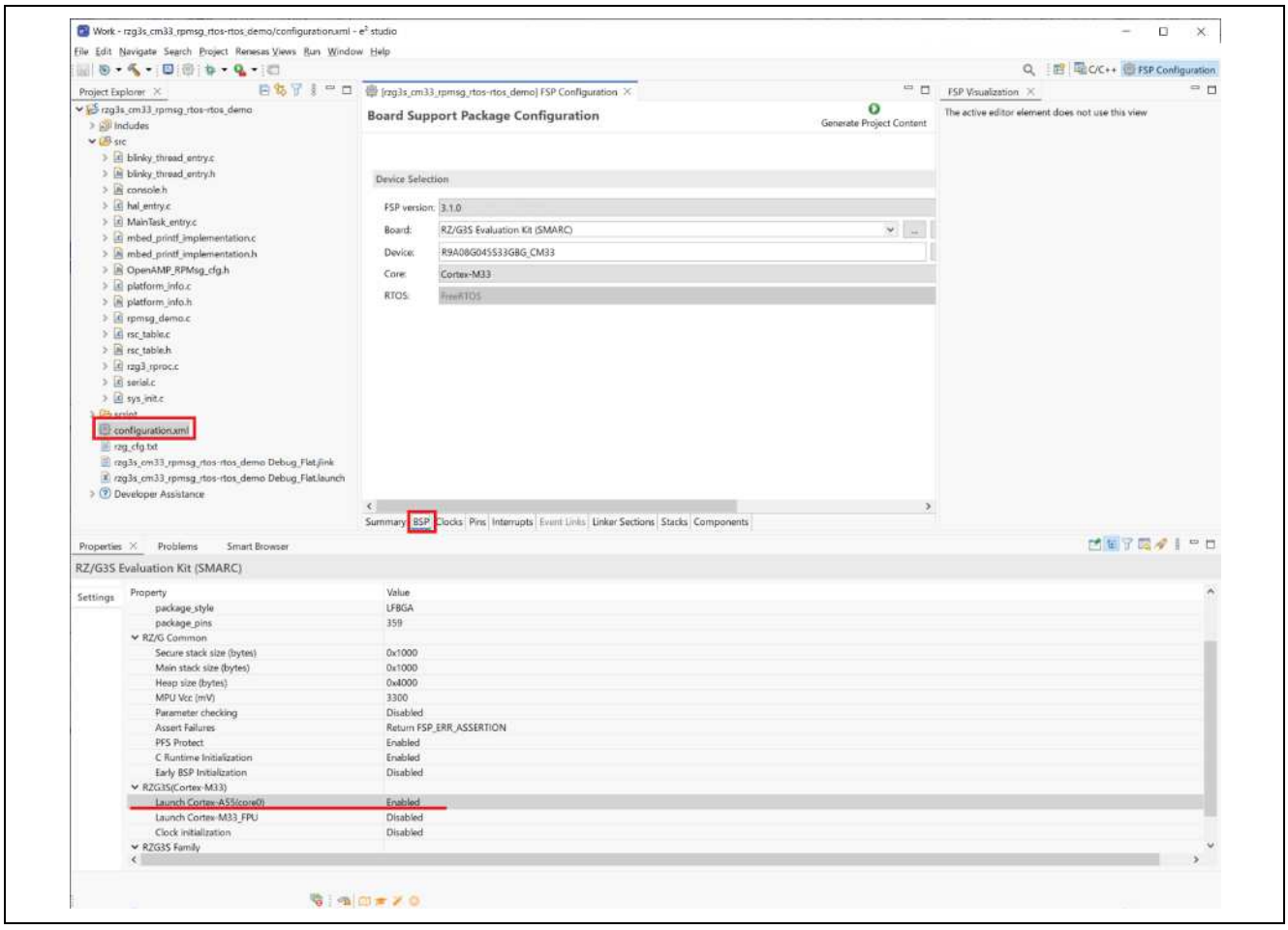


Figure 4-5. Linux boot configuration from CM33 cold boot

(Optional for CM33 cold boot support)

9. Click **Generate Project Content** to generate the updated source code:

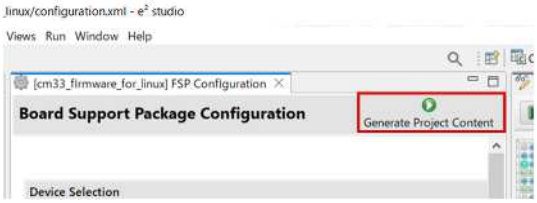


Figure 4-6. Generate Project Content

10. Build the project from **Choose Project** > **Build Project**.
11. If the build is successfully completed, the following files should be generated in Debug and/or Release folder in accordance with the active Build Configuration.
    - <device>_rpmsg_linux-rtos_demo.elf (Note1)
    - <device>_rpmsg_linux-rtos_demo.srec (Note 1)
    - <device>_rpmsg_rtos-rtos_demo.elf (Note 1)
    - <device>_rpmsg_rtos-rtos_demo.srec (Note 1)

Notes: 1. The possible string for <device> is any of rzg3s_cm33 and rzg3s_cm33_fpu.

4.3 CM33 Sample Program Invocation for communicating with Linux

4.3.1 CM33 Sample Program Invocation using Segger J-Link

You need to follow the following steps to invocate CM33 sample program with Segger J-Link.

(Optional for CM33 cold boot support)

1. Select **Run** > **Debug Configurations...** if CM33 is configured as Boot CPU for RZ/G3S.

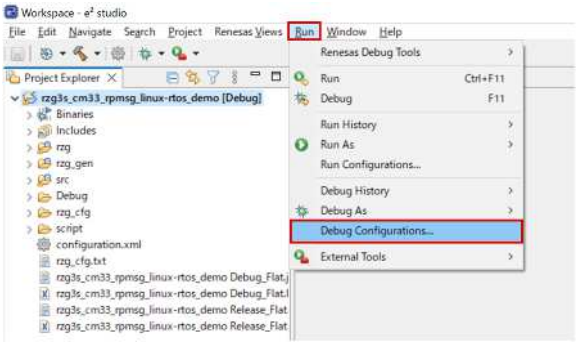


Figure 4-7. Debug Configuration (1)

(Optional for CM33 cold boot support)

2. Click **rzg3s_cm33_rpmsg_<com_type>_demo Debug_Flat** or **rzg3s_cm33_rpmsg_<com_type>_demo Release_Flat**.

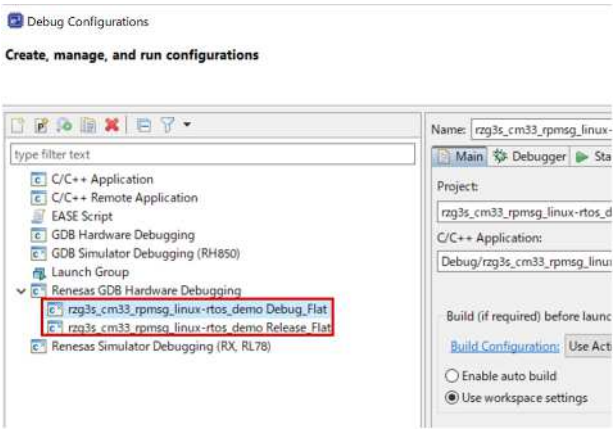


Figure 4-8. Debug Configuration (2)

(Optional for CM33 cold boot support)

3. Click **Debugger** tab and select **Connection Settings** as shown below:

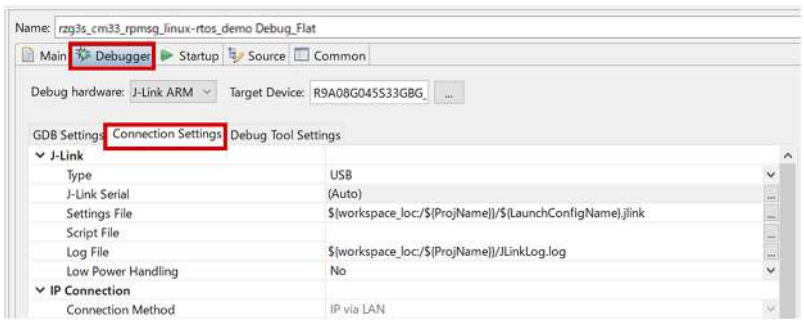


Figure 4-9. Debugger - Connection Settings

(Optional for CM33 cold boot support)

4. Configure **Reset after download** as **Yes**.

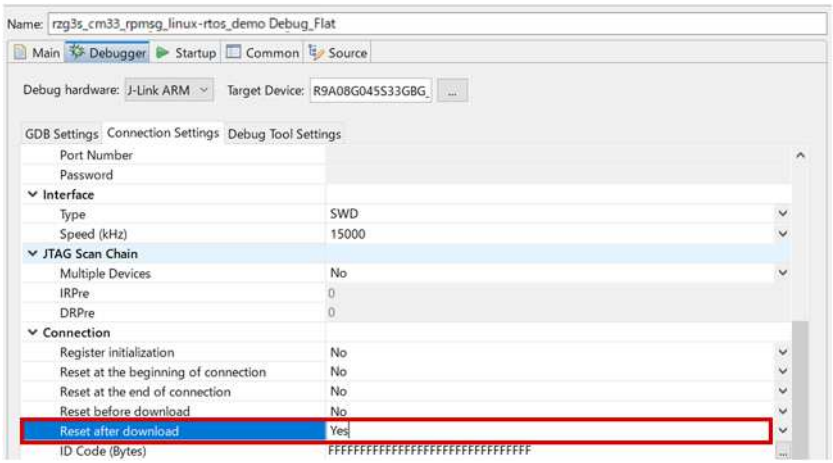


Figure 4-10. Reset after download Setting

(Optional for CM33 cold boot support)

5. Select **Startup** tab and click **Add...** as shown below:

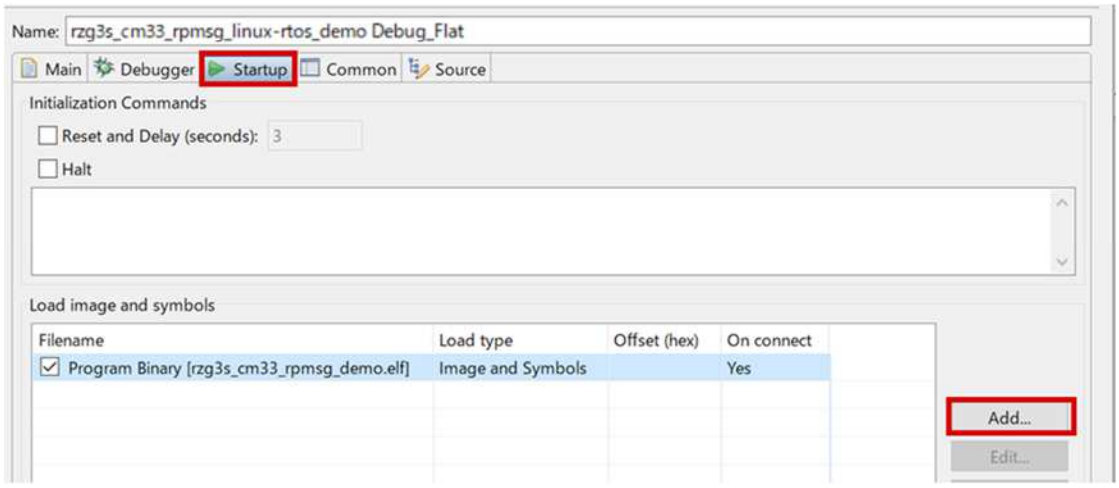


Figure 4-11. Add download module (1)

(Optional for CM33 cold boot support)

6. Click **Workspage...**, choose **rzg3s_cm33_rpmsg_<com_type>_demo_cm33boot.srec** and click **OK**.

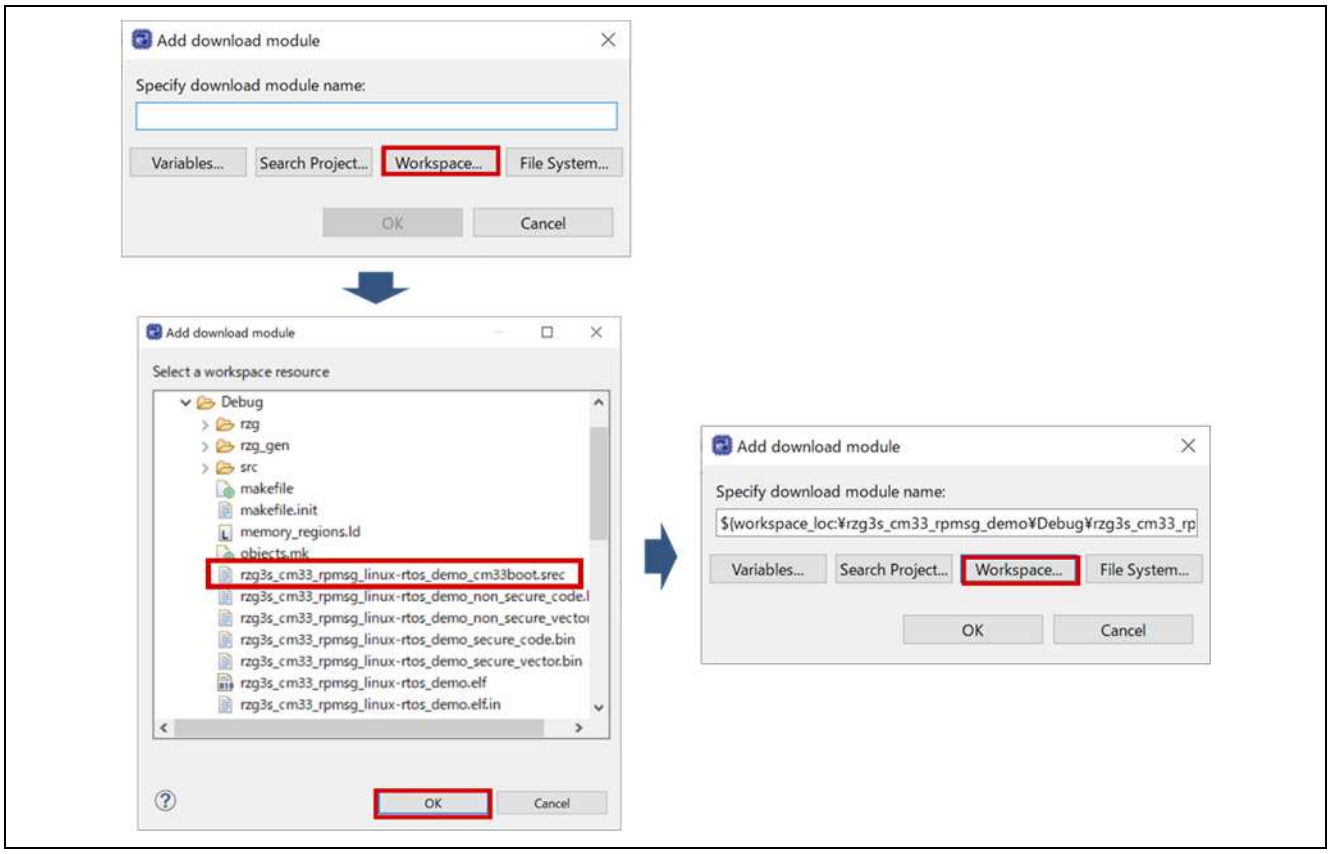


Figure 4-12. Add download module (2)

(Optional for CM33 cold boot support)

7. Configure **Load type** of **Program Binary [rzg3s_cm33_rpmsg_<com_type>_demo.elf]** and **rzg3s_cm33_rpmsg_<com_type>_demo_cm33boot.srec** as **Symbols only** and **Image only**, respectively.

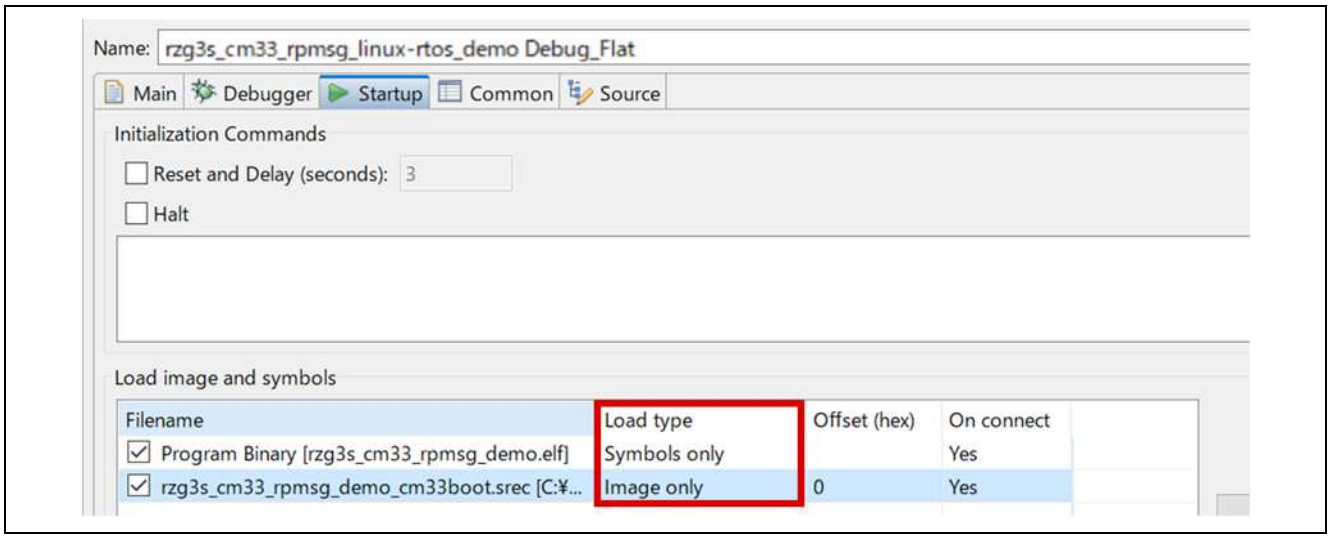


Figure 4-13. Configuration of Load type

8. Click Debug button to launch Debug Perspective.

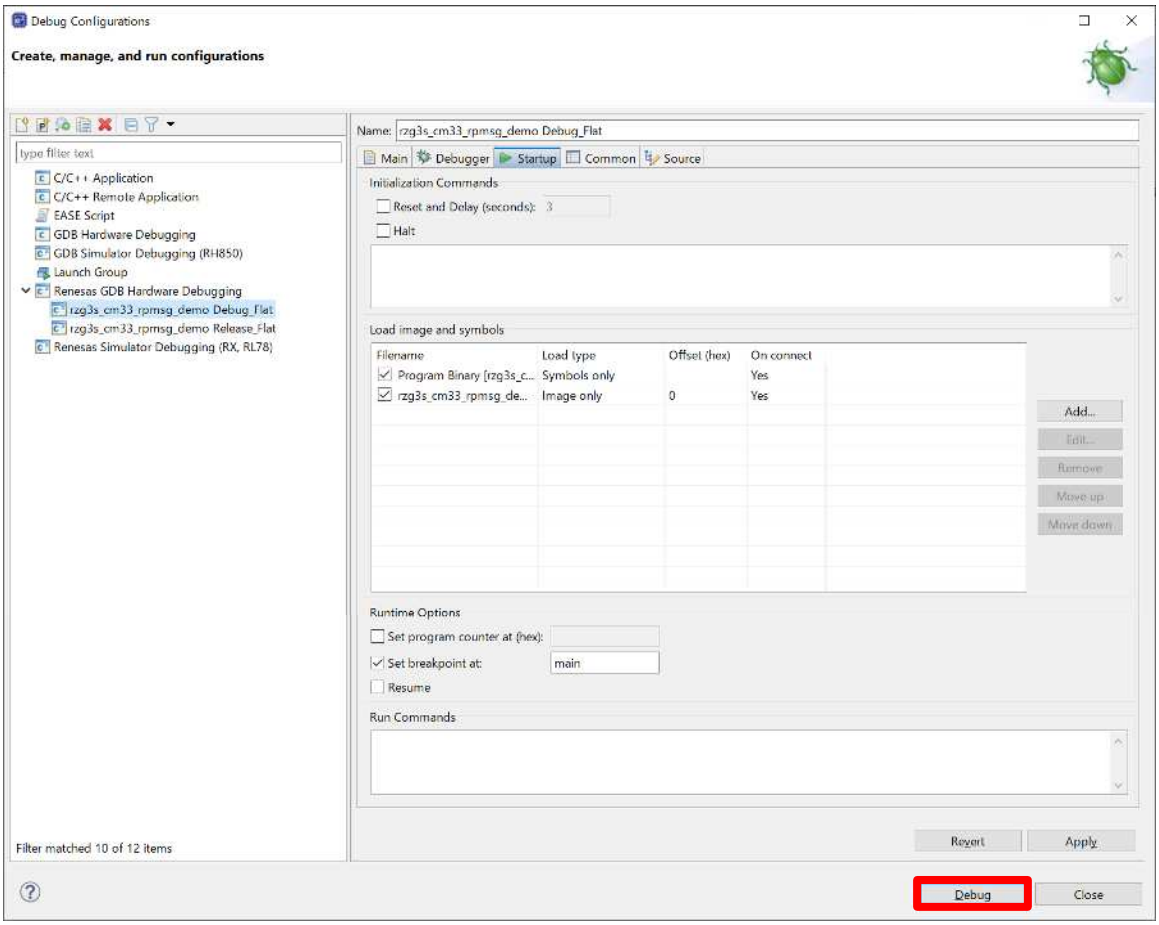


Figure 4-14. Debug Perspective Launch

If **Confirmation Perspective Switch** window below apprears, press **Switch** to continue:

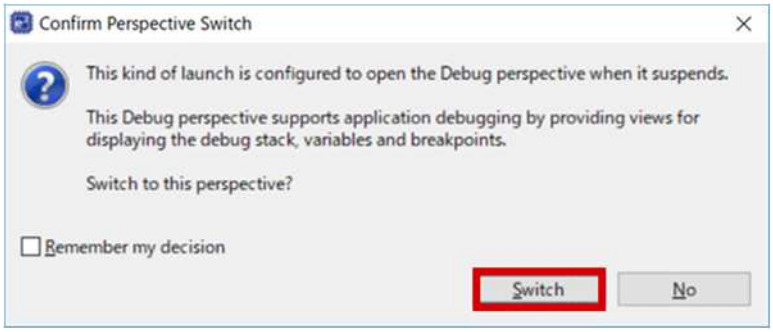


Figure 4-15. Confirm Perspective Switch

9. When the debug perspective is opened, Program Counter (PC) should be located at the top of Warm_Reset_S function. Then, you need to press the button indicated by a red arrow in Figure 4-17:

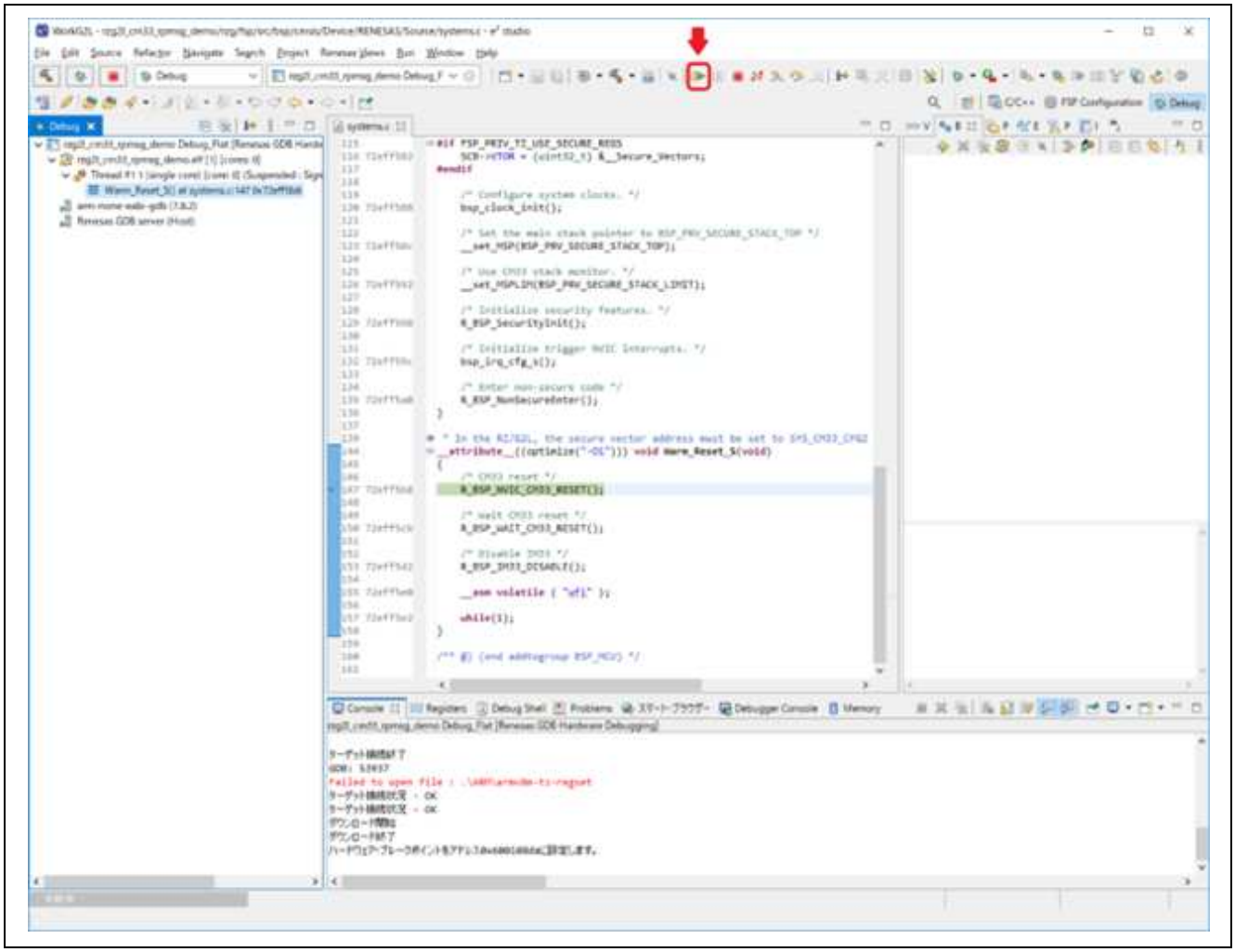


Figure 4-16. Start to debug RPMgs Sample Program (1)

10. The program should stop at the top of the **main** function. Then, click the same button as the previous step.

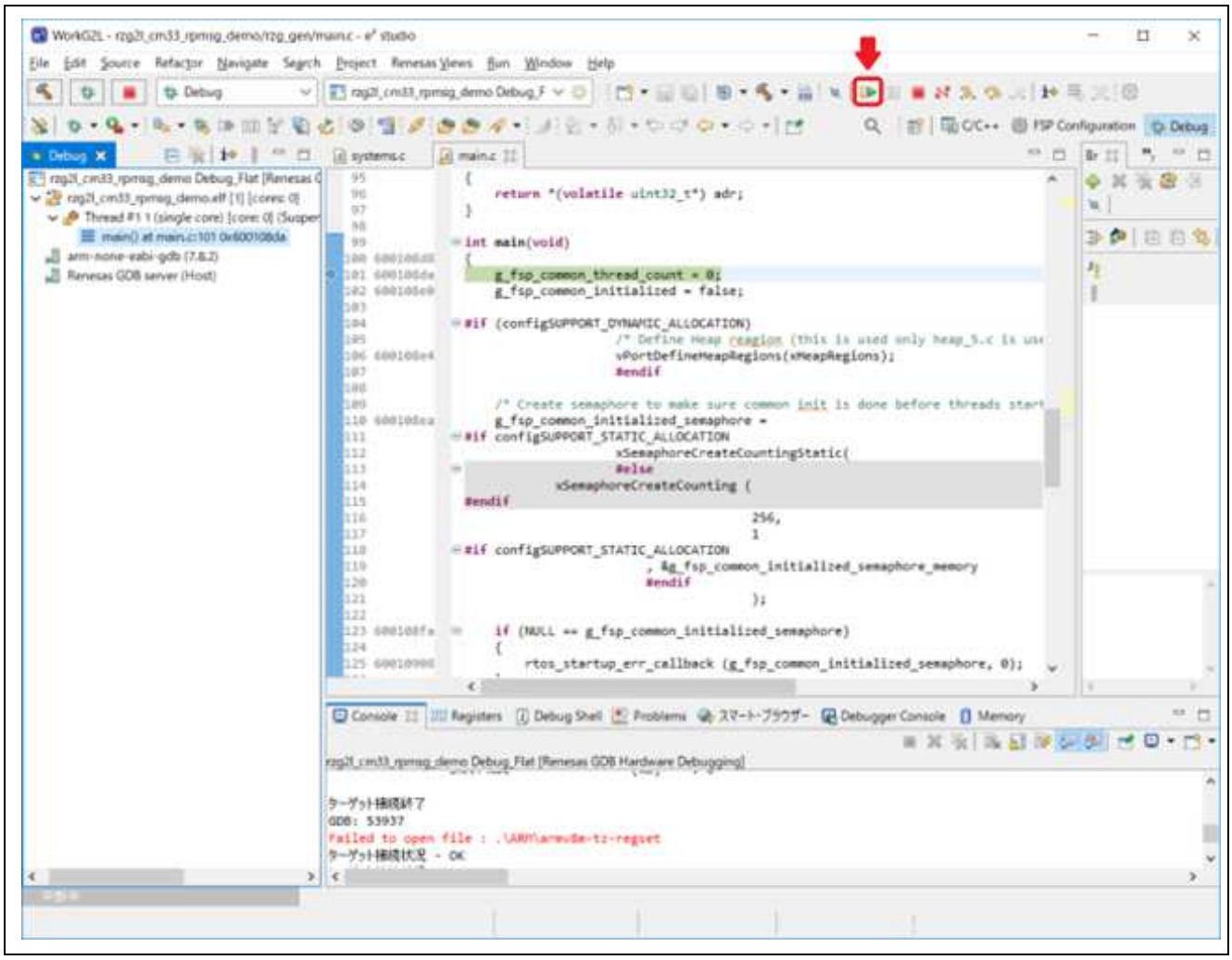


Figure 4-17. Start to debug RPMgs Sample Program (2)

11. Now that CM33 sample program has been started, the following message is shown on the console connected to Pmod USBUART: (Note)

```
Successfully probed IPI device
Successfully open uio device: 42F00000.rsctbl.
Successfully added memory device 42F00000.rsctbl.
Successfully open uio device: 43000000.vring-ctl0.
Successfully added memory device 43000000.vring-ctl0.
Successfully open uio device: 43200000.vring-shm0.
Successfully added memory device 43200000.vring-shm0.
Initialize remoteproc successfully.
creating remoteproc virtio
initializing rpmsg vdev
```

At this point of time, the CM33 program is waiting for the establishment of rpmsg channel with CA55.

4.3.2 CM33 Sample Program Invocation from remoteproc

On RZ/G3S SMARC EVK, you can invoke RPMsg sample program with remoteproc by following the procedure stated below:

1. Booting up Linux by following **5. Booting and Running Linux** of **Linux Start-up Guide**
2. Invoke the command below to specify RPMsg sample program to be loaded:

```
root@smarc-rzg3s:~# echo <device>_rpmsg_linux-rtos_demo.elf > /sys/class/remoteproc/remoteprocX/firmware
(Note 1)(Note 2)
```

3. Kick CM33 by invoking the command below:

```
root@smarc-rzg3s:~# echo start > /sys/class/remoteproc/remoteprocX/state
```

If CM33 starts to work successfully, the following message should be shown:

```
root@smarc-rzg3s:~# echo start > /sys/class/remoteproc/remoteproc0/state
[  152.569813] remoteproc remoteproc0: powering up cm33
[  152.647167] remoteproc remoteproc0: Booting fw image rzg3s_cm33_rpmsg_linux-rtos_demo.elf, size
1068216
[  152.657050] remoteproc remoteproc0: unsupported resource 4
[  152.669150]  remoteproc0#vdev0buffer: assigned reserved memory node vdev0buffer@0x43200000
[  152.682507]  remoteproc0#vdev0buffer: registered virtio1 (type 7)
[  152.692313] remoteproc remoteproc0: remote processor cm33 is now up
```

Note: 1. **<device>** should be either rzg3s_cm33 or rzg3s_cm33-fpu.
2. **remoteprocX** can be either remoteproc0 or remoteproc1. When you would like to kick CM33, remoteproc0 should be specified. Also, remoteproc1 should be specified for kicking CM33_FPU.

4.3.3 CM33 Sample Program Invocation with BL2 of Trusted Firmware-A

On RZ/G3S SMARC EVK, you can invoke RPMsg sample program from BL2 of Trusted Firmware-A by the procedure stated below. Be sure to configure CA55 as boot CPU when enabling this feature.

1. Apply the following modification in red character to meta-renesas/meta-rzg3s/recipes-bsp/trusted-firmware-a/trusted-firmware-a.bbappend.

```
require trusted-firmware-a.inc

COMPATIBLE_MACHINE_rzg3s = "(rzg3s-dev|smarc-rzg3s)"

PLATFORM_rzg3s-dev = "g3s"
EXTRA_FLAGS_rzg3s-dev = "BOARD=dev14_1_lpddr PLAT_SYSTEM_SUSPEND=vbat"
EXTRA_FLAGS_smarc-rzg3s = "BOARD=smarc PLAT_SYSTEM_SUSPEND=vbat PLAT_M33_BOOT_SUPPORT=1"
```

2. Rebuild Trusted Firmware-A.
3. Re-program the resultant BL2 and FIP binary files using FlashWriter.
4. Program rzg3s_cm33_rpmsg_<com_type>_demo.srec using FlashWriter with the parameter stated below:

- For Boot Mode 1

Partition Area	Start Address in sector	Program Start Address
1	1000	80200000

- For Boot Mode 2

Address to load to RAM	Address to save to ROM
80200000	200000

4.4 CA55 Sample Program Invocation

On RZ/G3S SMARC EVK, you need to follow the procedure shown below to invoke CA55 sample program running on Linux.

1. Boot up Linux by executing the following command on u-boot:

```
run bootcmd
```

2. Login as **root**.

```
smarc-<device> login: root
```

3. Run CA55 sample program by executing the following command on Linux.

```
root@smarc-<device>:~# rpmsg_sample_client
```

4. Then, you can see the following message on the console of Linux side.

```
**************************************
*   rpmsg communication sample program   *
**************************************

1. communicate between CM33 cores
2. communicate between CM33 and CA55

e. exit

please input
>
```

5. Input the number which performs the communication you would like to try on the console. Please note that 1 is allowable ONLY when remoteproc support is enabled. Also, you must NOT invoke the CM33 program in advance. Meanwhile, in case of selecting 1, you need to invoke the CM33 program in advance.

6. In case of typing 1, the communication between CM33 cores should be established and the communication log is repeatedly displayed via the Pmod USBUART. Also, when 2 is typed, you can see the following message on Linux console:

```
[XXX] proc_id:0 rsc_id:0 mbx_id:0
metal: info:      metal_uio_dev_open: No IRQ for device 10400000.mbox-uio.
metal: info:      metal_uio_dev_open: No IRQ for device 11010000.cpg-uio.
[XXX] Successfully probed IPI device
metal: info:      metal_uio_dev_open: No IRQ for device 42f00000.rsctbl.
[XXX] Successfully open uio device: 42f00000.rsctbl.
[XXX] Successfully added memory device 42f00000.rsctbl.
metal: info:      metal_uio_dev_open: No IRQ for device 43000000.vring-ctl0.
[XXX] Successfully open uio device: 43000000.vring-ctl0.
[XXX] Successfully added memory device 43000000.vring-ctl0.
metal: info:      metal_uio_dev_open: No IRQ for device 43200000.vring-shm0.
[XXX] Successfully open uio device: 43200000.vring-shm0.
[XXX] Successfully added memory device 43200000.vring-shm0.
metal: info:      metal_uio_dev_open: No IRQ for device 43100000.vring-ctl1.
[XXX] Successfully open uio device: 43100000.vring-ctl1.
[XXX] Successfully added memory device 43100000.vring-ctl1.
metal: info:      metal_uio_dev_open: No IRQ for device 43500000.vring-shm1.
[XXX] Successfully open uio device: 43500000.vring-shm1.
[XXX] Successfully added memory device 43500000.vring-shm1.
metal: info:      metal_uio_dev_open: No IRQ for device 42f01000.mhu-shm.
[XXX] Successfully open uio device: 42f01000.mhu-shm.
[XXX] Successfully added memory device 42f01000.mhu-shm.
[XXX] Initialize remoteproc successfully.
[XXX] proc_id:1 rsc_id:1 mbx_id:0
[XXX] Initialize remoteproc successfully.
[XXX] proc_id:0 rsc_id:0 mbx_id:1
[XXX] Initialize remoteproc successfully.
[XXX] proc_id:1 rsc_id:1 mbx_id:1
[XXX] Initialize remoteproc successfully.

****************************************
*   rpmsg communication sample program   *
****************************************

1. communicate with CM33 ch0
2. communicate with CM33 ch1
3. communicate with CM33_FPU ch0
4. communicate with CM33_FPU ch1
5. communicate with CM33 ch0 and CM33_FPU ch1

e. exit

please input
>
```

7. Input the number which performs the communication between CM33 and CA55 you would like to try on the console.

4.5 Overview of Sample Program's behavior

This section describes the overview of sample program's behavior.

1. When the CA55 sample program is successfully executed, the communication channel among CA55 and CM33 is established.
2. The CA55 sample program starts to send the message to CM33 with incrementing the message size from the minimum value 17 to the maximum value 488. During the communication, the message as shown below is displayed on your console:

```
[xxx] Sending payload number 148 of size 165
```

3. When CM33 sample program receives the message sent from CA55, the echo reply is sent back to CA55 sample program.
4. When CA55 receives the echo reply, the message below should be displayed on your console:

```
[xxx] received payload number 148 of size 165
```

5. After the 488-byte sized payload is sent from CA55 to CM33, CM33 sends back the echo reply, the message indicating the termination of the communication channel is sent from CA55 to CM33. Then, the CA55 sample program outputs the following log messages to your console:

- **Termination message on CA55**

```
**********************************
Test Results: Error count = 0
**********************************
Quitting application .. Echo test end
Stopping application...
```

- **Termination message on CM33**

```
De-initializing remoteproc
```

Then, CM33 side re-waits for the establishment of connection channel. You can see the following log on the console a short time later:

```
creating remoteproc virtio
initializing rpmsg vdev
```

5. CM33 cold boot support

This chapter describes how CA55 and CM33 related stuff should be deployed for CM33 cold boot.

5.1 RZ/G VLP Setup

This section described how to integrate AWO related stuff to RZ/G VLP v3.0.7.

1. Follow the procedure from the beginning of **2.2 Building Images** to **(3) Add layers** of **SMARC EVK of RZ/G3S Linux Start-up Guide**.

2. Download Multi-OS Feature Package (r01an5869ej0300-rzg-multi-os-pkg.zip) to your working directory and run the commands stated below:

```
$ cd ~/rzg_vlp_<pkg ver>
$ unzip <Multi-OS download dir>/r01an5869ej0300-rzg-multi-os-pkg.zip
$ tar zxvf r01an5869ej0300-rzg-multi-os-pkg/meta-rz-features_multi-os_v3.0.0.tar.gz
```

3. Apply the patch file as follows:

```
$ cd ~/rzg_vlp_<pkg_ver>
$ patch -p1 < ./r01an5869ej0300-rzg-multi-os-pkg/0001-bl2-cm33-coldboot-support.patch
```

Note: the other 3 patches must not be applied in this CM33 cold boot environment.

4. Continue to set up VLP by following **(4) - (5) of 2.2 Building images** in **SMARC EVK of RZ/G3S Linux Start-up Guide**.

5.2 Deployment of CA55 Build Artifacts to SMARC EVK

If CM33 is configured as Boot CPU, you need to follow the procedure stated below for deploying bootloader files, Linux kernel image, device tree and rootfs:

1. Follow **3. Preparing the SD Card**, **4.1 Preparation of Hardware and Software**, **4.2 Startup Procedure** and **4.3 Download Flash Writer to RAM** of **SMARC EVK of RZ/G3S Linux Start-up Guide** to Invoke Flash Writer.

(Optional for Flash Writer settings)

2. Change the transfer rate of Flash Writer from the default one (115200bps) to the high speed one (921600bps) as shown below:

```
> sup
Scif speed UP
Please change to 921.6Kbps baud rate setting of the terminal.
```

3. Program **bl2_no_bp_spi-smarc-rzg3s.srec** with Flash Writer as shown below:

```
> XLS2
===== Qspi writing of RZ/G3 Board Command =============
Load Program to Spiflash
Writes to any of SPI address.
Program size & Qspi Save Address
===== Please Input Program Top Address ============
Please Input : H'a1e00
===== Please Input Qspi Save Address ===
Please Input : H'200000
Please send ! ('.' & CR stop load)
```

Send **bl2_no_bp_spi-smarc-rzg3s.srec** via terminal software (e.g., TeraTerm) after the message **Please send ! ('.' & CR stop load)** is output on your console as shown above.

When **bl2_no_bp_spi-smarc-rzg3s.srec** is programmed successfully, the following message is shown on your console:

```
Erase SPI Flash memory...
Erase Completed
Write to SPI Flash memory.
======= Qspi Save Information =================
SpiFlashMemory Stat Address : H'00200000
SpiFlashMemory End Address  : H'0021EB58
================================================

SPI Data Clear(H'FF) Check : H'00000000-0000FFFF,Clear OK?(y/n)
```

Finally, type **y** to continue

4. Program **fip-smarc-rzg3s.srec** with Flash Writer as shown below:

```
> XLS2
===== Qspi writing of RZ/G3 Board Command =============
Load Program to Spiflash
Writes to any of SPI address.
Program size & Qspi Save Address
===== Please Input Program Top Address ============
Please Input : H'0
===== Please Input Qspi Save Address ===
Please Input : H'264000
Please send ! ('.' & CR stop load)
```

Send **fip-smarc-rzg3s.srec** via terminal software (e.g., TeraTerm) after the message **Please send ! ('.' & CR stop load)** is output on your console as shown above.

When **fip-smarc-rzg3s.srec** is programmed successfully, the following message is shown on your console:

```
Erase SPI Flash memory...
Erase Completed
Write to SPI Flash memory.
======= Qspi Save Information =================
SpiFlashMemory Stat Address : H'00264000
SpiFlashMemory End Address  : H'00342B6E
================================================

SPI Data Clear(H'FF) Check : H'00000000-0000FFFF,Clear OK?(y/n)
```

Finally, type **y** to continue.

5.3 Setup and deployment of CM33 related stuff

Refer to **4.2 CM33 Sample Program Setup** and follow the procedure including the item "**(Optional for CM33 cold boot support)**".

Note: Do not follow the procedure "**(Optional for remoteproc support)**" at this time.

6. Reference Documents

- R01AN5924 RZ/G2L RZ/G2LC RZ/G2UL RZ/G3S RZ/G3E Getting Started with Flexible Software Package
- R01UH1076 RZ/G3S SMARC Module Board User's Manual: Hardware
- R01UH1077 RZ SMARC Series Carrier Board II User's Manual: Hardware

Revision History

Rev.	Date	Description	
		Page	Summary
3.00	Jul.22.2025	-	First edition.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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