To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

User's Manual

Renesas Starter Kit for H8S/2456R

User's Manual

RENESAS SINGLE-CHIP MICROCOMPUTER
H8S FAMILY

Renesas Electronics
www.renesas.com

Rev.1.00 2009.04

Disclaimer

By using this Renesas Starter Kit (RSK), the user accepts the following terms. The RSK is not guaranteed to be error free, and the entire risk as to the results and performance of the RSK is assumed by the User. The RSK is provided by Renesas on an “as is” basis without warranty of any kind whether express or implied, including but not limited to the implied warranties of satisfactory quality, fitness for a particular purpose, title and non-infringement of intellectual property rights with regard to the RSK. Renesas expressly disclaims all such warranties. Renesas or its affiliates shall in no event be liable for any loss of profit, loss of data, loss of contract, loss of business, damage to reputation or goodwill, any economic loss, any reprogramming or recall costs (whether the foregoing losses are direct or indirect) nor shall Renesas or its affiliates be liable for any other direct or indirect special, incidental or consequential damages arising out of or in relation to the use of this RSK, even if Renesas or its affiliates have been advised of the possibility of such damages.

Precautions

This Renesas Starter Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not is use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

Table of Contents

Chapter 1. Preface

Cautions

This document may be, wholly or partially, subject to change without notice.

Trademarks

All brand or product names used in this manual are trademarks or registered trademarks of their respective companies or organisations.

Copyright

Website: www.renesas.com

Glossary

ADC	Analog to Digital Converter	CD	Compact Disc
CPU	Central Processing Unit	DAC	Digital to Analog Converter
E10A	'E10A for Starter Kit' debugger	LCD	Liquid Crystal Display
ESD	Electrostatic Discharge	EMC	Electromagnetic compatibility
HEW	High-Performance Embedded Workshop	I/O	Input / Output
LED	Light Emitting Diode	MCU	Microcontroller Unit
PC	Personal Computer	RAM	Random Access Memory
ROM	Read-Only Memory	RSK	Renesas Starter Kit
SCI	Serial Communication Interface	USB	Universal Serial Bus

Chapter 2. Purpose

This RSK is an evaluation tool for Renesas microcontrollers.

This manual describes the technical details of the RSK hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

Features include:

- Renesas Microcontroller Programming.
- User Code Debugging.
- User Circuitry such as switches, LEDs and potentiometer(s).
- Sample Application.
- Sample peripheral device initialisation code.

The RSK board contains all the circuitry required for microcontroller operation.

Chapter 3. Power Supply

3.1. Requirements

This RSK board operates from a 5V DC power supply (supplied).

A diode provides reverse polarity protection only if a current limiting power supply is used.

All RSK boards are supplied with an E10A debugger.

All RSK boards have an optional centre positive supply connector using a 2.0mm barrel power jack.

Warning

The RSK board is neither under nor over voltage protected. Use a centre positive supply for this board.

3.2. Power–up Behaviour

When the RSK is purchased, the RSK board has the ‘Release’ or stand-alone code from the example tutorial code pre-programmed into the Renesas microcontroller. On powering up the board the user LEDs will start to flash. After 200 flashes or after pressing any switch the LEDs will flash at a rate controlled by the potentiometer.

Chapter 4. Board Layout

4.1. Component Layout

The following diagram shows the top layer component layout of the board.

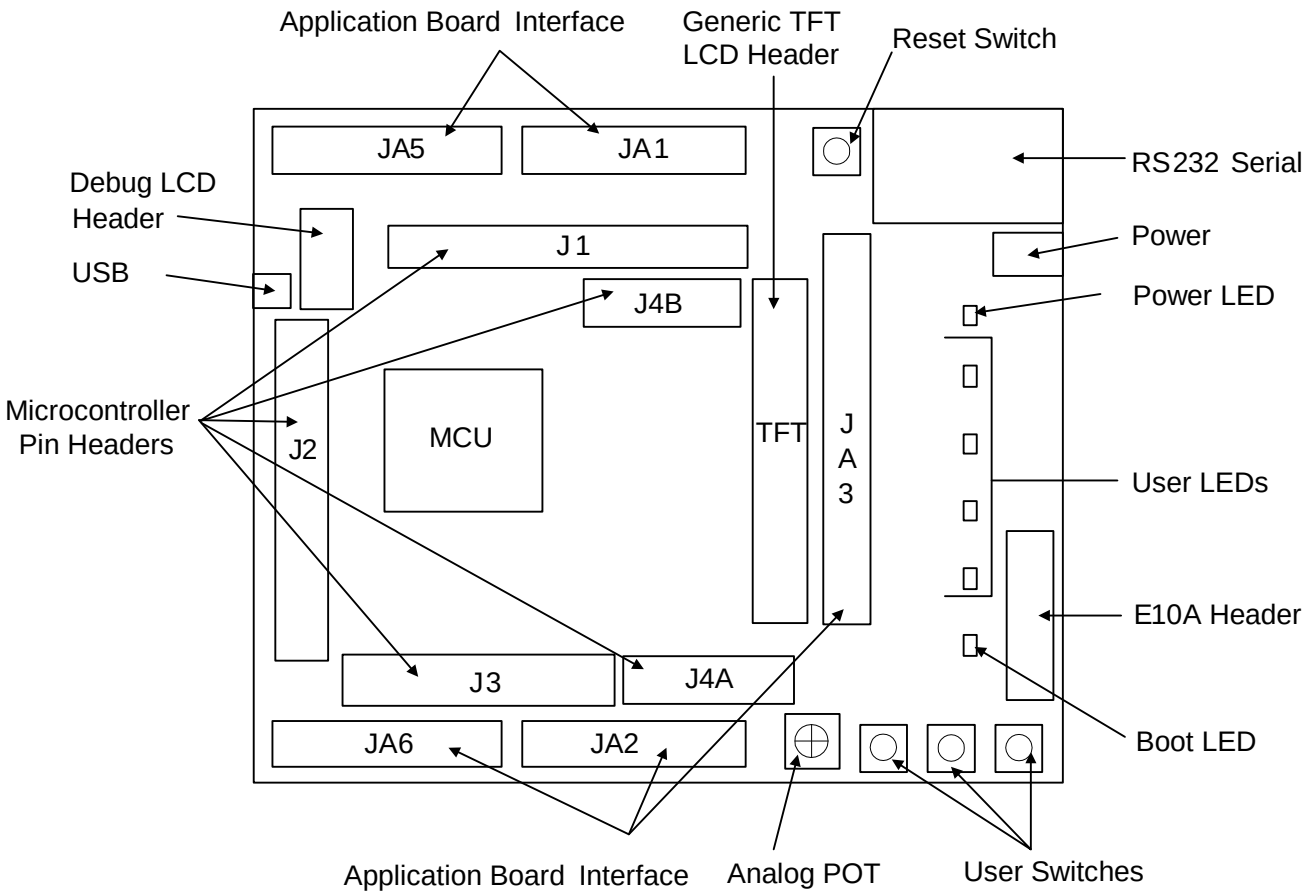


Figure 4-1: Board Layout

4.2. Board Dimensions

The following diagram gives the board dimensions and connector positions. All through-hole connectors are on a common 0.1” grid for easy interfacing.

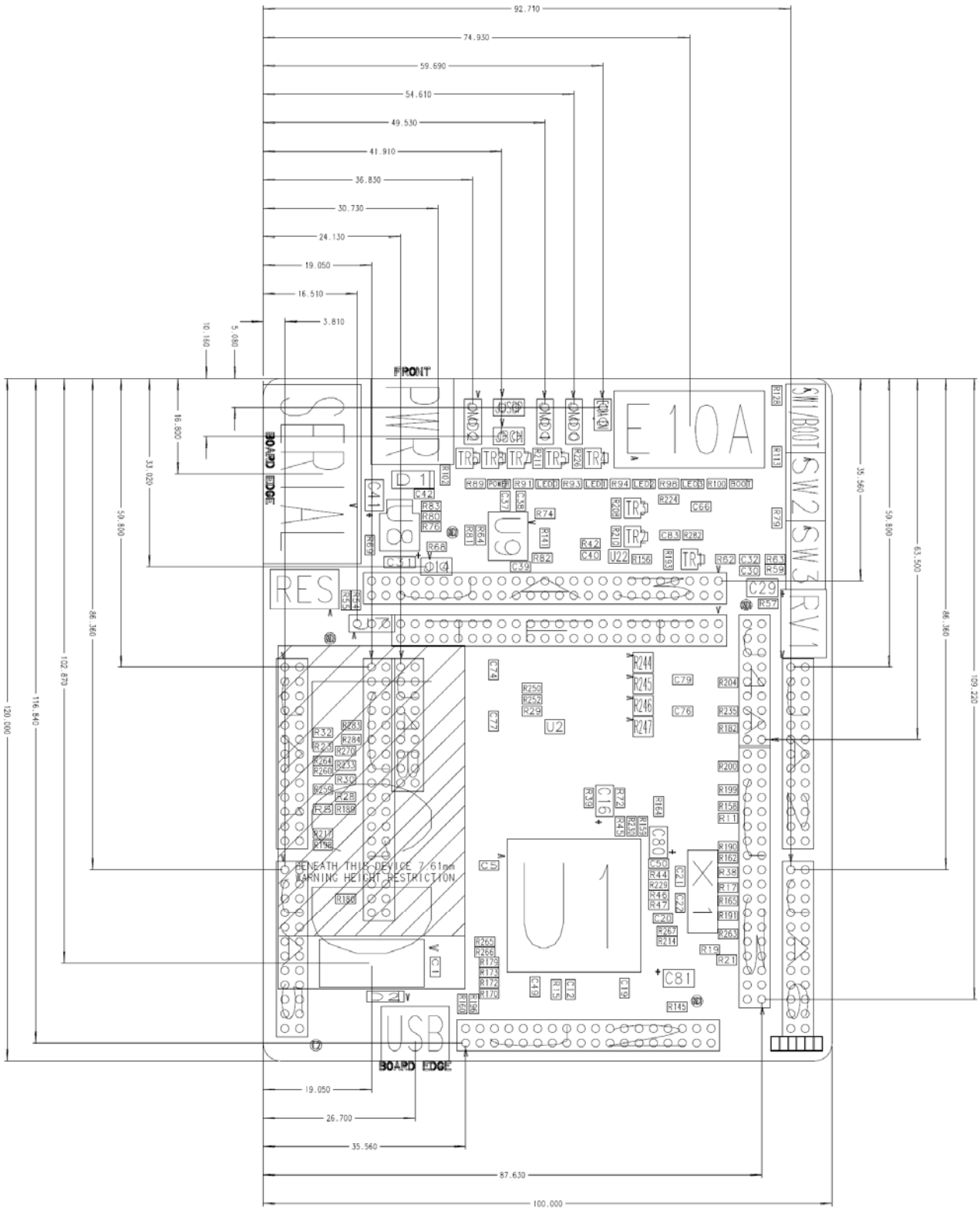


Figure 4-2: Board Dimensions

Chapter 5. Block Diagram

Figure 5-1 shows the RSK board components and their connectivity.

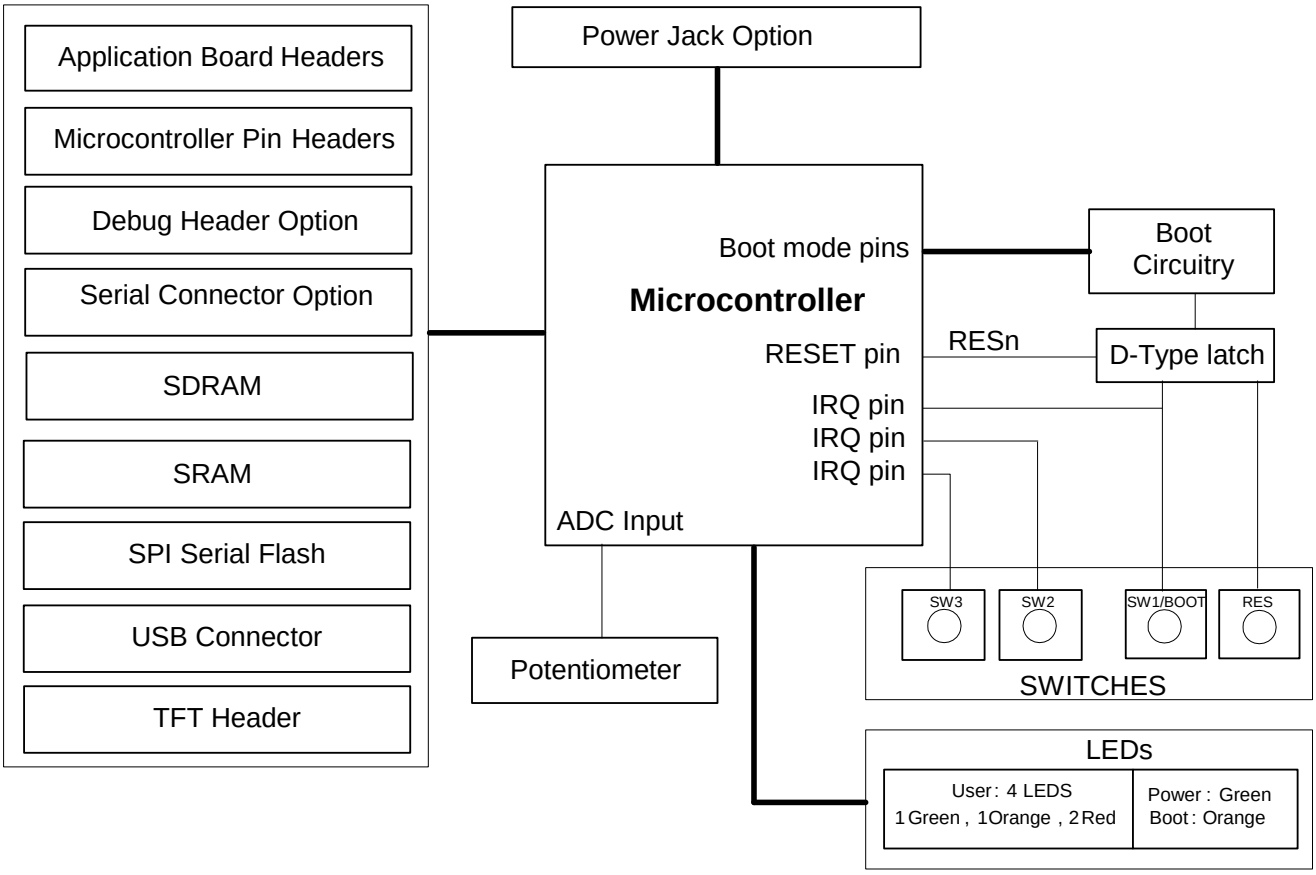


Figure 5-1: Block Diagram

Figure 5-2 shows E10A connections to the RSK.

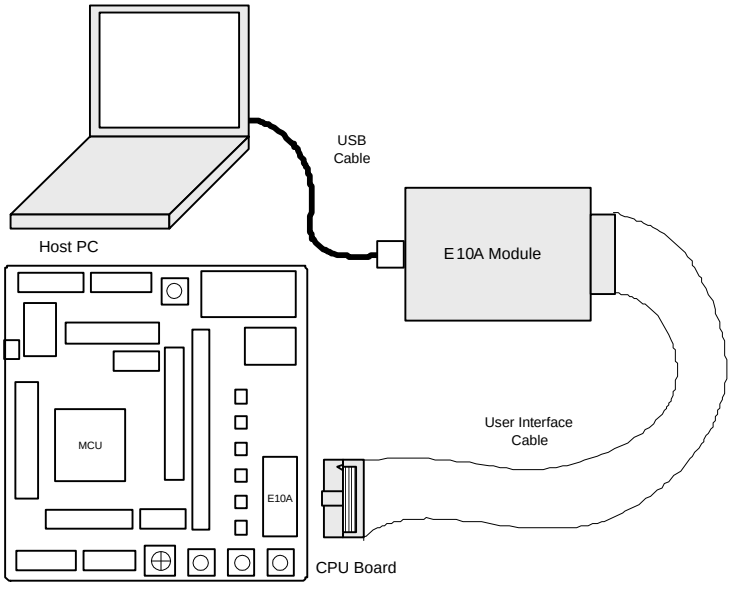


Figure 5-2: E10A RSK Connections

Chapter 6. User Circuitry

6.1. Switches

There are four switches located on the RSK board. The function of each switch and its connection are shown in **Table 6-1**

Switch	Function	Microcontroller
RES	When pressed, the microcontroller is reset.	RESn, Pin 92
SW1 / BOOT*	Connects to an IRQ input for user controls. The switch is also used in conjunction with the RES switch to place the device in BOOT mode when not using the E10A debugger.	IRQ9An, Pin 82 (Port 6, bit 1)
SW2*	Connects to an IRQ line for user controls.	IRQ1Bn, Pin 33 (Port 8, bit 1)
SW3*	Connects to an IRQ line for user controls. Option link allows connection to ADC trigger input. For more details on option links, please refer to Sec. 6.6.	IRQ2Bn, Pin 34 (Port 8, bit 2)

Table 6-1: Switch Functions

*Refer to the schematic for detailed connectivity information.

6.2. LEDs

There are six LEDs on the RSK board. The green 'POWER' LED lights when the board is powered. The orange BOOT LED indicates the device is in BOOT mode when lit. The four user LEDs are connected to an I/O port and will light when their corresponding port pin is set low.

Table 6-2 below shows the LED pin references and their corresponding microcontroller port pin connections.

LED Reference (As shown on silkscreen)	Colour	Microcontroller Port Pin function	Microcontroller Pin Number
LED0	Green	Port 6, bit 3	104
LED1	Orange	Port 6, bit 5	106
LED2	Red	Port J, bit 0	100
LED3	Red	Port J, bit 1	101

Table 6-2: LED Port

6.3. Potentiometer

A single-turn potentiometer is connected to pin AN0 (Port 4 bit 0, pin 113) of the microcontroller. This may be used to vary the input analog voltage value to this pin between AVCC and Ground.

Note: The potentiometer is fitted to offer an easy way of supplying a variable analogue input to the controller. It does not necessarily reflect the accuracy of the controller's ADC. Please see the device manual for details.

6.4. Serial port

Serial port SCI1 is connected to the standard RS232 header. Serial port SCI0 can optionally be connected to the RS232 transceiver by moving option resistors. The connections to be moved are listed in the **Table 6-3**.

Description	Function	Microcontroller Port Pin	Fit for RS232	Remove for RS232
SCI1	Default serial port (TX)	141 (Port 3, bit 1)	R150	R60, R256
SCI1	Default serial port (RX)	139 (Port 3, bit 3)	R151	R70, R257
SCI0	Spare Serial Port (TX)	142 (Port 3, bit 0)	R60	R150, R256
SCI0	Spare Serial Port (RX)	140 (Port 3, bit 2)	R70	R151, R257

Table 6-3: Serial port settings

The serial channels SCI0 and SCI1 are also available on the ring connector 'J4B'. The serial channel SCI0 is available on JA2.

The board is designed to accept a straight-through RS-232 male-to-female cable.

Serial port SCI3 can be connected to a 0.1" header, 'J7' by fitting 0Ω link resistors to R64 and R81.

6.5. USB

This RSK has a Full-speed (12 Mbps) USB port compliant to USB 2.0 specification. It is available as 'USB' (Mini-B receptacle) on the RSK. This port also allows boot mode programming.

Table 6-4 shows the pin allocation and signal names used on this connector.

Pin No.	Pin Name	Circuit Net Name	Device Pin
1	5V	VBUS	-
2	DNEG	USB-	54 (via 33 Ω resistor, R173)
3	DPOS	USB+	53 (via 33 Ω resistor, R172)
4	ID	-	-
5	GND	GROUND	-

Table 6-4: USB

For more details, please refer to H8S/2456 Group Hardware Manual.

6.6. Debug LCD Module

A debug LCD module is supplied to be connected to the connector LCD. This should be fitted so that the debug LCD module lies over J1. Care should be taken to ensure the pins are inserted correctly into LCD. The debug LCD module uses a 4 bit interface to reduce the pin allocation. No contrast control is provided; this is set by a resistor on the supplied display module.

Table 6-5 shows the pin allocation and signal names used on this connector.

The module supplied with the RSK board only supports 5V operation.

LCD					
Pin	**Circuit Net Name**	**Device Pin**	**Pin**	**Circuit Net Name**	**Device Pin**
1	Ground	-	2	5V	-
3	No Connection	-	4	DLCDRS	137 (Port 3, bit 5)
5	R/W (Wired to write only using 10K pull down))	-	6	DLCDE (+ 100k pull down to ground)	61 (Port 8, bit 5)
7	No Connection	-	8	No Connection	-
9	No Connection	-	10	No Connection	-
11	DLCD4	42 (Port 1, bit 0)	12	DLCD5	43 (Port 1, bit 1)
13	P26_DLCD6	57 (Port 2, bit 6)	14	P27_DLCD7	58 (Port 2, bit 7)

Table 6-5: Debug LCD Module Connections

6.7. Option Links

In this section, the default configuration is indicated by **BOLD** text.

Table 6-6 below describes the function of the option links associated with serial port configuration.

Option Link Settings				
Reference	**Function**	**Fitted**	**Alternative (Removed)**	**Related To**
R54	Serial Port Configuration	Connects channel 2 (Rx pin) of the RS232 transceiver to pin 7 of the D-type serial port connector	**Disconnects Channel 2 (RX pin) of the RS232 transceiver from the D-type serial port connector**	R55, R81
R55	Serial Port Configuration	Connects channel 2 (Tx pin) of the RS232 transceiver to pin 8 of the D-type serial port connector	**Disconnects Channel 2 (TX pin) of the RS232 transceiver from the D-type serial port connector**	R54, R64
R60	Serial Port Configuration	Connects the TxD pin of serial port SCI0 to the D-type connector via the RS232 transceiver	**Disconnects the TxD pin of serial port SCI0 from the D-type connector**	R70, R150, R256
R64	Serial Port Configuration	Connects the TxD pin of serial port SCI3 to the header 'J7' via the RS232 transceiver	**Disconnects the TxD pin of serial port SCI3 from the header 'J7'**	R55, R81
R70	Serial Port Configuration	Connects the RxD pin of serial port SCI0 to the D-type connector via the RS232 transceiver	**Disconnects the RxD pin of serial port SCI0 from the D-type connector**	R60, R151, R257
R78	Serial Port Configuration	Disables the RS-232 Transceiver. (Must be removed if R82 is fitted.)	**Enables the RS-232 Transceiver**	R82
R81	Serial Port Configuration	Connects the RxD pin of serial port SCI3 to the header 'J7' via the RS232 transceiver	**Disconnects the RxD pin of serial port SCI3 from the header 'J7'**	R54, R64
R82	Serial Port Configuration	**Enables the RS-232 Transceiver. (Must be removed if R78 is fitted.)**	Disables the RS-232 Transceiver	R78
R150	Serial Port Configuration	**Connects the TxD pin of serial port SCI1 to the D-type connector via the RS232 transceiver**	Disconnects the TxD pin of serial port SCI1 from the D-type connector	R151, R60, R256
R151	Serial Port Configuration	**Connects the RxD pin of serial port SCI1 to the D-type connector via the RS232 transceiver**	Disconnects the RxD pin of serial port SCI1 from the D-type connector	R150, R70, R257
R255	Serial Port Configuration	Connects the shield of D-type serial port connector to GROUND	**Disconnects the shield of D-type serial port connector from GROUND**	-
R256	Serial Port Configuration	Connects the RS232 serial port (Tx) to the application board interface (JA6-5).	**Disconnects the RS232 serial port (Tx) from application board interface (JA6-5)**	R257, R60, R150
R257	Serial Port Configuration	Connects the RS-232 serial port (Rx) to application board interface (JA6-6)	**Disconnects the RS-232 serial port (Rx) from application board interface (JA6-6)**	R256, R70, R151

Table 6-6: Serial port configuration links

Table 6-7 below describes the function of the option links associated with CPU Mode configuration.

Option Link Settings				
Reference	**Function**	**Fitted**	**Alternative (Removed)**	**Related To**
R147	CPU Mode Select	**MD2 pin can be controlled using the BOOT switch**	MD2 pin cannot be controlled using the BOOT switch. (Jumper JMD2 can be fitted to connect pins 1-2 to enable controlling the MD2 pin using the BOOT switch (i.e. SW1))	R248, R281
R248	CPU Mode Select	**MD0 pin can be controlled using the BOOT switch**	MD0 pin cannot be controlled using the BOOT switch. (Jumper JMD0 can be fitted to connect pins 1-2 to enable controlling the MD0 pin using the BOOT switch (i.e. SW1))	R147, R281
R249	CPU Mode Select	**USB in Self powered boot mode**	USB in Bus powered boot mode. Jumper JUSBP can be used as an alternate	-
R281	CPU Mode Select	**MD1 pin can be controlled using the BOOT switch**	MD1 pin cannot be controlled using the BOOT switch. (Jumper JMD1 can be fitted to connect pins 1-2 to enable controlling the MD1 pin using the BOOT switch (i.e. SW1))	R147, R248

Table 6-7: CPU Mode Select Configuration Links

Table 6-8 below describes the function of the option links associated with Power Source configuration.

Option Link Settings				
Reference	**Function**	**Fitted**	**Alternative (Removed)**	**Related To**
R68	Microcontroller Power Supply	**Supply power to the Microcontroller VCC pins**	Disables 5V power supply to the microcontroller VCC pins. Supply current to the sections powered from VCC pin of the MCU can be measured across 'J14'	-
R69	Power source	**5V source can be supplied to the voltage regulator IC (LM1117) at CON_5V (JA1-1)**	5V source can be supplied to the voltage regulator IC (LM1117) through PWR connector (if R102 is fitted) or from VBUS via the net '5V' (if R76 is fitted)	R76, R102
R76	Power source	**5V source can be supplied to the voltage regulator IC (LM1117) from VBUS via the net '5V'**	5V source can be supplied to the voltage regulator IC (LM1117) through PWR connector (if R102 is fitted) or through CON_5V (JA1-1) connector (if R69 is fitted)	R69, R102
R80	Power Source	**Connects the net CON_3V3 (JA1-3) to Board_VCC. External 3.3V supply can be connected at CON_3V3. (R83 Must be removed if supplying 3.3V from CON_3V3.)**	Disconnects CON_3V3 from Board_VCC	R83
R83	Power source	**Connects the 3.3V output of the on-board voltage regulator (LM1117) to Board_VCC (Must be removed if supplying 3.3V from CON_3V3.)**	Disconnects the 3.3V output of the on-board voltage regulator (LM1117) from Board_VCC	R80
R102	Power Source	**5V source can be supplied to the voltage regulator IC (LM1117) at PWR connector**	5V source can be supplied to the voltage regulator IC (LM1117) through CON_5V (JA1-1) connector (if R69 is fitted) or from VBUS via the net '5V' (if R76 is fitted)	R69, R76

Table 6-8: Power configuration links

Table 6-9 below describes the function of the option links associated with Analog Voltage Source configuration.

Option Link Settings				
Reference	**Function**	**Fitted**	**Alternative (Removed)**	**Related To**
R39	Analog Reference Voltage	Connects VREF to CON_VREF at JA1-7.	**Disconnects VREF from CON_VREF.**	R72
R56	Analog Voltage Source	**Connects AVCC to Board_VCC.**	Disconnects AVCC from Board_VCC.	R57
R57	Analog Voltage Source	Connects AVCC to CON_AVCC at JA1-5.	**Disconnects AVCC from CON_AVCC.**	R56
R62	Analog Voltage Source	**Links analog & digital ground signals.**	Separates analog & digital ground signals	-
R72	Analog Reference Voltage	**Connects VREF to Board_VCC.**	Disconnects VREF from Board_VCC.	R39

Table 6-9: Analog Configuration Links

Table 6-10 below describes the function of the option links associated with SDRAM interface.

Option Link Settings				
Reference	**Function**	**Fitted**	**Alternative (Removed)**	**Related To**
R45	SDRAM Interface	Connects CASn pin (port G, bit 3) of the MCU (part of SDRAM interface) to CON_CASn at J4A-2	**Disconnects CASn pin (port G, bit 3) of the MCU (part of SDRAM interface) from CON_CASn**	R230
R230	SDRAM Interface	Connects RASn pin (port G, bit 2) of the MCU (part of SDRAM interface) to CON_RASn at J4A-1	**Disconnects RASn pin (port G, bit 2) of the MCU (part of SDRAM interface) from CON_RASn**	R45
R265	SDRAM Interface	Connects SDRAM clock output pin of the MCU to the ring connector at J1-36	**Disconnects SDRAM clock output pin of the MCU from the ring connector**	R266
R266	SDRAM Interface	**Connects SDRAM clock output pin of the MCU to clock input pin of the on-board SDRAM**	Disconnects SDRAM clock output pin of the MCU from clock input pin of the on-board SDRAM	R265

Table 6-10: SDRAM Interface Configuration Links

Table 6-11 below describes the function of the option links associated with application board interface.

Option Link Settings				
Reference	**Function**	**Fitted**	**Alternative (Removed)**	**Related To**
R8	Application Board Interface	Connects MCU port pin P27 (pin 58) to IO7 at JA1-22	**Disconnects MCU port pin P27 (pin 58) from IO7**	R9
R9	Application Board Interface	**Connects MCU port pin P27 (pin 58) to P27_DLCD7 of the debug LCD**	Disconnects MCU port pin P27 (pin 58) from P27_DLCD7	R8
R10	Application Board Interface	**Connects MCU port pin P52 (pin 135) to SCK2 at JA6-10**	Disconnects MCU port pin P52 (pin 135) from SCK2	R11
R11	Application Board Interface	Connects MCU port pin P52 (pin 135) to IRQ2An at JA2-23	**Disconnects MCU port pin P52 (pin 135) from IRQ2An**	R10
R19	Application Board Interface	**Connects MCU port pin P85 (pin 61) to DLCDE pin of debug LCD**	Disconnects MCU port pin P85 (pin 61) from DLCDE pin of debug LCD	R21
R21	Application Board Interface	Connects MCU port pin P85 (pin 61) to SCK3 at JA6-11	**Disconnects MCU port pin P85 (pin 61) from SCK3**	R19
R23	Application Board Interface	Connects MCU port pin P10 (pin 42) to TIOCA0 at JA2-19	**Disconnects MCU port pin P10 (pin 42) from TIOCA0**	R25, R189
R25	Application Board Interface	**Connects MCU port pin P10 (pin 42) to DLCD4 of the debug LCD**	Disconnects MCU port pin P10 (pin 42) from DLCD4	R23, R189
R28	Application Board Interface	Connects MCU port pin P11 (pin 43) to IO5 at JA1-20	**Disconnects MCU port pin P11 (pin 43) from IO5**	R276, R233
R30	Application Board Interface	Connects MCU port pin PJ1 (pin 101) to IO3 at JA1-18	**Disconnects MCU port pin PJ1 (pin 101) from IO3**	R33, R273
R31	Application Board Interface	**Connects MCU port pin P40 (pin 113) to AD_POT**	Disconnects MCU port pin P40 (pin 113) from AD_POT	R32
R32	Application Board Interface	Connects MCU port pin P40 (pin 113) to AN0 at JA1-9	**Disconnects MCU port pin P40 (pin 113) from AN0**	R31
R33	Application Board Interface	**Connects MCU port pin PJ1 (pin 101) to LED3**	Disconnects MCU port pin PJ1 (pin 101) from LED3	R30, R273
R161	Application Board Interface	**Connects MCU port pin P61 (pin 82) to SW1 (as IRQ9An input)**	Disconnects MCU port pin P61 (pin 82) from SW1	R162
R162	Application Board Interface	Connects MCU port pin P61 (pin 82) to DREQ1n at JA6-1	**Disconnects MCU port pin P61 (pin 82) from DREQ1n**	R161
R180	Application Board Interface	**Connects MCU port pin P81 (pin 33) to SW2 (as IRQ1Bn input)**	Disconnects MCU port pin P81 (pin 33) from SW2	R251
R182	Application Board Interface	Connects MCU port pin P51 (pin 134) to IRQ1An at JA2-9	**Disconnects MCU port pin P51 (pin 134) from IRQ1An**	R184
R184	Application Board Interface	**Connects MCU port pin P51 (pin 134) to RXD2 at JA6-7**	Disconnects MCU port pin P51 (pin 134) from RXD2	R182

R185	Application Board Interface	**Connects MCU port pin P26 (pin 57) to P26_DLCD6 of the debug LCD**	Disconnects MCU port pin P26 (pin 57) from P26_DLCD6	R277
R186	Application Board Interface	**Connects MCU port pin P50 (pin 133) to TXD2 at JA6-8**	Disconnects MCU port pin P50 (pin 133) from TXD2	R235
R189	Application Board Interface	Connects MCU port pin P10 (pin 42) to IO4 at JA1-19	**Disconnects MCU port pin P10 (pin 42) from IO4**	R23, R25
R197	Application Board Interface	**Connects MCU port pin P35 (pin 137) to DLCDRS pin of debug LCD**	Disconnects MCU port pin P35 (pin 137) from DLCDRS pin of debug LCD	R198
R198	Application Board Interface	Connects MCU port pin P35 (pin 137) to SCL0 at JA1-26	**Disconnects MCU port pin P35 (pin 137) from SCL0**	R197
R206	Application Board Interface	**Connects MCU port pin P83 (pin 59) to SCSn at TFT-32**	Disconnects MCU port pin P83 (pin 59) from SCSn	R207, R263
R207	Application Board Interface	Connects MCU port pin P83 (pin 59) to IRQ3Bn at JA1-23	**Disconnects MCU port pin P83 (pin 59) from IRQ3Bn**	R206, R263
R217	Application Board Interface	**Connects MCU port pin P34 (pin 138) to SDA0 at JA1-25**	Disconnects MCU port pin P34 (pin 138) from SDA0	R218
R218	Application Board Interface	**Connects MCU port pin P34 (pin 138) to SCK0 at JA2-10**	Disconnects MCU port pin P34 (pin 138) from SCK0	R217
R233	Application Board Interface	**Connects MCU port pin P11 (pin 43) to DLCD5 of the debug LCD**	Disconnects MCU port pin P11 (pin 43) from DLCD5	R28, R276
R235	Application Board Interface	Connects MCU port pin P50 (pin 133) to IRQ0An at JA2-7	**Disconnects MCU port pin P50 (pin 133) from IRQ0An**	R186
R251	Application Board Interface	Connects MCU port pin P81 (pin 33) to TXD3 at JA6-9	**Disconnects MCU port pin P81 (pin 33) from TXD3**	R180
R258	Application Board Interface	**Connects MCU port pin PJ0 (pin 100) to LED2**	Disconnects MCU port pin PJ0 (pin 100) from LED2	R259, R272
R259	Application Board Interface	Connects MCU port pin PJ0 (pin 100) to IO2 at JA1-17	**Disconnects MCU port pin PJ0 (pin 100) from IO2**	R258, R272
R260	Application Board Interface	Connects MCU port pin P65 (pin 106) to IO1 at JA1-16	**Disconnects MCU port pin P65 (pin 106) from IO1**	R261, R271
R261	Application Board Interface	**Connects MCU port pin P65 (pin 106) to LED1**	Disconnects MCU port pin P65 (pin 106) from LED1	R260, R271
R262	Application Board Interface	**Connects MCU port pin P63 (pin 104) to LED0**	Disconnects MCU port pin P63 (pin 104) from LED0	R264, R270
R263	Application Board Interface	Connects MCU port pin P83 (pin 59) to RXD3 at JA6-12	**Disconnects MCU port pin P83 (pin 59) from RXD3**	R206, R207
R264	Application Board Interface	Connects MCU port pin P63 (pin 104) to IO0 at JA1-15	**Disconnects MCU port pin P63 (pin 104) from IO0**	R262, R270

R270	Application Board Interface	Connects MCU port pin P63 (pin 104) to TEND1n at JA6-3	**Disconnects MCU port pin P63 (pin 104) from TEND1n**	R262, R264
R271	Application Board Interface	Connects MCU port pin P65 (pin 106) to DACK1n at JA6-2	**Disconnects MCU port pin P65 (pin 106) from DACK1n**	R260, R261
R272	Application Board Interface	**Connects MCU port pin PJ0 (pin 100) to XDRIVE at TFT-41**	Disconnects MCU port pin PJ0 (pin 100) from XDRIVE	R258, R259
R273	Application Board Interface	**Connects MCU port pin PJ1 (pin 101) to YDRIVE at TFT-42**	Disconnects MCU port pin PJ1 (pin 101) from YDRIVE	R30, R33
R276	Application Board Interface	Connects MCU port pin P11 (pin 43) to TIOCB0 at JA2-20	**Disconnects MCU port pin P11 (pin 43) from TIOCB0**	R233, R28
R277	Application Board Interface	Connects MCU port pin P26 (pin 57) to IO6 at JA1-21	**Disconnects MCU port pin P26 (pin 57) from IO6**	R185

Table 6-11: Application Board Interface configuration links

Table 6-12 below describes the function of the option links associated with Clock configuration.

Option Link Settings				
Reference	**Function**	**Fitted**	**Alternative (Removed)**	**Related To**
R44	Main clock	External clock can be connected to the MCU between CON_EXTAL (at J3-25 or JA2-2) and CON_XTAL (at J3-24)	**On-board clock (X1) can be connected**	R46, R47
R46	Main clock	**Connects the on-board clock (X1) to the MCU (at MCU pins 97 and 96)**	External Clock Source can be connected.	R44, R47
R47	Main clock	External clock can be connected to the MCU between CON_EXTAL (at J3-25 or JA2-2) and CON_XTAL (at J3-24)	**On-board clock (X1) can be connected**	R44, R46
R229	Main clock	Parallel resistor for oscillator X1	**Not fitted.**	-
R267	Clock Output	**Connects the clock output (Φ) (port pin PF7, MCU pin 94) to the ring connector at J3-22**	Disconnects the clock output (Φ) from the ring connector	R214

Table 6-12: Clock configuration links

Table 6-13 below describes options links related to on-board memory interface.

Option Link Settings				
Reference	**Function**	**Fitted**	**Alternative (Removed)**	**Related To**
R144	Serial Flash Interface	Stops the serial communication with the serial flash (SST25VF016B)	**Enables the serial communication with the serial flash (SST25VF016B)**	-
R145	SRAM Interface	Enables byte mode access for on-board SRAM (R1LV1616R)	**Disables byte mode access for on-board SRAM (R1LV1616R)**	-
R216	Serial Flash Interface	Writing to the on-board serial flash (SST25VF016B) is disabled.	**Writing to the on-board serial flash (SST25VF016B) is enabled.**	-
R231	Chip select outputs	**Enables buffered data outputs for CS0 area**	Disables buffered data outputs for CS0 area	R232
R232	Chip select outputs	Enables buffered data outputs for CS1 area	**Disables buffered data outputs for CS1 area**	R231

Table 6-13: Memory Interface Option Links

Table 6-14 below describes options links related to various peripheral configurations.

Option Link Settings				
Reference	**Function**	**Fitted**	**Alternative (Removed)**	**Related To**
R59	User Switch	Connects MCU port pin PF0 (pin 84) to SW3 (as ADTRG0Bn input)	**Disconnects MCU port pin PF0 (pin 84) from SW3**	R63
R63	User Switch	**Connects MCU port pin P82 (pin 34) to SW3 (as IRQ2Bn input)**	Disconnects MCU port pin P82 (pin 34) from SW3	R59
R146	USB Interface	Connects shield of USB receptacle to GROUND	**Disconnects shield of USB receptacle from GROUND**	-
R214	TFT LCD Interface	Connects MCU port pin PF7 (pin 94) to LCD_GPIO4_PHI at TFT-36	**Disconnects MCU port pin PF7 (pin 94) from LCD_GPIO4_PHI**	R219, R267
R219	TFT LCD Interface	**Connects MCU port pin P62 (pin 83) to LCD_GPIO4_PHI at TFT-36**	Disconnects MCU port pin P62 (pin 83) from LCD_GPIO4_PHI	R214

Table 6-14: Peripheral Configuration Option Links

6.8. Oscillator Sources

A crystal oscillator is fitted on the RSK board and used to supply the main clock input to the Renesas microcontroller. **Table 6-15** details the oscillators that are fitted on this RSK:

Component		
Crystal (X1)	Fitted	16 MHz (HC49/4H package)

Table 6-15: Oscillators / Resonators

6.9. Reset Circuit

A reset control IC (i.e. RNA51957BFP) has been used to generate the reset signal required for the H8S/2456R CPU.

Please check the hardware manual for the detailed reset requirements to ensure the reset circuit on the user's board meets all the reset timing requirements.

Chapter 7. Modes

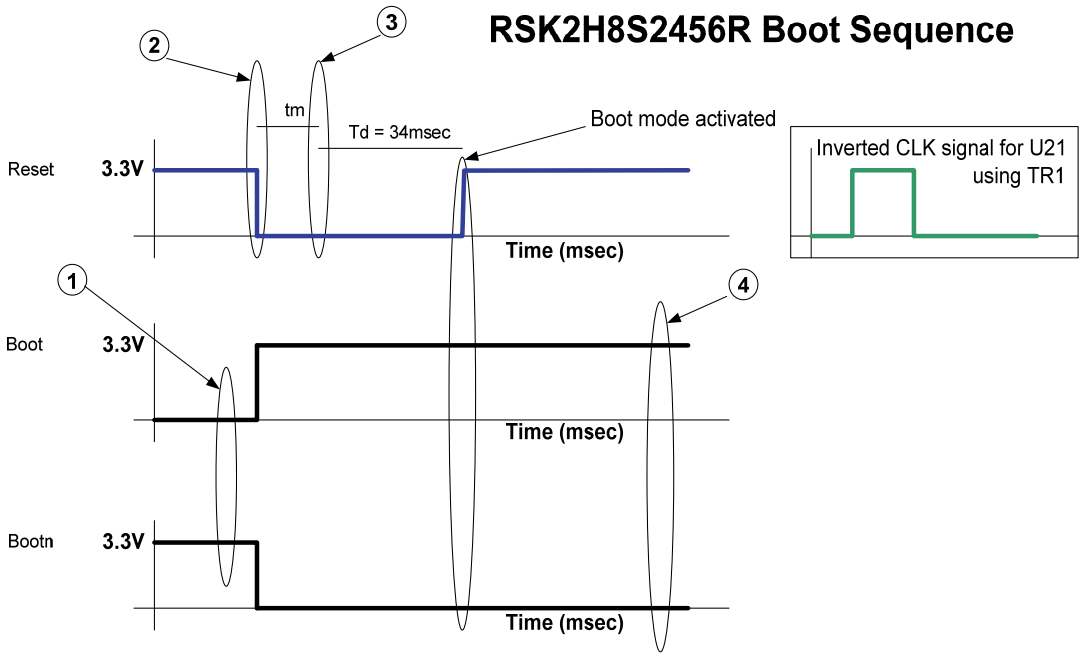
This RSK supports Boot modes, User Program Modes and User mode.

This RSK provides the capability of changing between User and Boot mode using a simple latch circuit. This is only to provide a simple mode control on this board when the E10A debugger is not in use.

The mode pins should change state only while the reset signal is active to avoid possible device damage.

This circuit is not required on customer's boards as it is intended for providing easy evaluation of the operating modes of the device on the RSK.

To manually enter the Boot mode, press and hold the SW1/BOOT. The mode pins are held in their boot states while reset is pressed and released. Release the boot button. The BOOT LED will be illuminated to indicate that the microcontroller is in boot mode.



Boot Procedure

1- Press and Hold SW1/Boot switch
2- Press and Hold Reset switch
3- Release Reset switch
4- Release SW1/Boot switch

tm = Time in msec during the Reset switch is pressed.
td = Reset time in msec for the Renesas reset chip after Reset switch released

Note:

Please note that the Reset signal is also acting as CLK signal for the U21. CLK signal logic is inverted using TR1 on the schematics.

Figure 7-1: RSK2H8S2456R Boot Sequence

More information on the operating modes and programming the flash memory can be found in the H8S/2456 Group hardware manual.

7.1. Boot modes

The Boot mode (i.e. CPU mode 3) settings for this RSK board are shown in **Table 7-1** below:

Mode	MD2	MD1	MD0	Description	Port Pin P27	Port Pin P26	I/P clock frequency	On-Chip ROM	External Data Bus Max Value
3	0	1	1	SCI Boot Mode	0	0	-	Enabled	16
3	0	1	1	USB Boot mode	0	1	16 MHz	Enabled	16

Table 7-1: Boot Mode pin settings

7.2. User Program Modes

This RSK supports single-chip and memory expanded user modes. The default mode of this RSK is indicated by **BOLD** text.

Mode	MD2	MD1	MD0	Description	On-Chip ROM	External Data Bus Initial Value	External Data Bus Max Value
1	0	0	1	Expansion Mode	Disabled	16	16
2	0	1	0	Expansion Mode	Disabled	8	16
4	**1**	**0**	**0**	**Expansion Mode**	**Enabled**	**8**	**16**
7	1	1	1	Single Chip Mode	Enabled	-	16

Table 7-2: User Mode pin settings

Chapter 8. Programming Methods

The board is intended for use with HEW and the supplied E10A debugger. Refer to H8S/2456 Group Hardware Manual for details of programming the microcontroller without using these tools. Please note that, to use E10A debugger, jumper ‘E10A_EN’ must be fitted.

Chapter 9. Headers

9.1. Microcontroller Ring Headers

The microcontroller pin headers and their corresponding microcontroller connections are detailed in **Table 9-1** to **Table 9-5**.

Header Pin	Circuit Net Name	Device pin	Header Pin	Circuit Net Name	Device pin
1	MD2	1	2	GROUND	2
3	EDREQ2n	3	4	UC_VCC	4
5	A(0)	5	6	A(1)	6
7	A(2)	7	8	A(3)	8
9	A(4)	9	10	GROUND	10
11	A(5)	11	12	A(6)	12
13	A(7)	13	14	A(8)	14
15	A(9)	15	16	A(10)	16
17	A(11)	17	18	GROUND	18
19	A(12)	19	20	A(13)	20
21	A(14)	21	22	A(15)	22
23	A(16)	23	24	A(17)	24
25	GROUND	25	26	A(18)	26
27	A(19)	27	28	A(20)	28
29	A(21)	29	30	A(22)	30
31	A(23)	31	32	EMLE	32
33	IRQ1Bn_TXD3	33	34	IRQ2Bn	34
35	WEn	35	36	CON_SDCLK	36 (via R265)

Table 9-1: J1 microcontroller header

Header Pin	Circuit Net Name	Device pin	Header Pin	Circuit Net Name	Device pin
1	CS6n	37	2	CKE	38
3	TDO	39	4	NMIn	40
5	NC	---	6	TIOCA0_DLCD4_IO4	42
7	TIOCB0_DLCD5_IO5	43	8	TIOCC0	44
9	TIOCD0	45	10	SSO0A_TIOCA1	46
11	SSI0A	47	12	SSCK0A_TIOCA2	48
13	P17_SCS0An	49	14	GROUND	50
15	PUPD+	51	16	UC_VCC	52
17	NC	---	18	NC	---
19	GROUND	55	20	VbusDTCT	56
21	P26_DLCD6_IO6	57	22	P27_DLCD7_IO7	58
23	SCSn_IRQ3Bn_RXD3	59	24	EDACK2n	60
25	DLCDE_SCK3	61	26	PJ2	62
27	D(0)	63	28	D(1)	64
29	D(2)	65	30	D(3)	66
31	D(4)	67	32	D(5)	68
33	D(6)	69	34	GROUND	70
35	D(7)	71	36	UC_VCC	72

Table 9-2: J2 microcontroller header

Header Pin	Circuit Net Name	Device pin	Header Pin	Circuit Net Name	Device pin
1	D(8)	73	2	D(9)	74
3	D(10)	75	4	D(11)	76
5	D(12)	77	6	D(13)	78
7	D(14)	79	8	D(15)	80
9	LCD_GPIO3	81	10	IRQ9An_DREQ1n	82
11	LCD_GPIO4	83	12	ADTRG0Bn	84
13	DQMU	85	14	DQML	86
15	LWRn	87	16	HWRn	88
17	RDn	89	18	ASn	90
19	UC_VCC	91	20	RESn	92
21	GROUND	93	22	CON_PF7_PHI	94 (via R267)
23	GROUND	95	24	CON_XTAL	96 (via R47)
25	CON_EXTAL	97 (via R44)	26	UC_VCC	98
27	UC_VCC	99	28	XDRIVE_LED2_IO2	100
29	YDRIVE_LED3_IO3	101	30	GROUND	102
31	STBYn	103	32	TEND1n_LED0_IO0	104
33	CSn_SDRAM	105	34	DACK1n_LED1_IO1	106
35	CS0n	107	36	CS1n	108

Table 9-3: J3 microcontroller header

Header Pin	Circuit Net Name	Device pin	Header Pin	Circuit Net Name	Device pin
1	CON_RASn	109 (via R230)	2	CON_CASn	110 (via R45)
3	CON_AVCC	---	4	CON_VREF	---
5	AD_POT_AN0	113	6	X_INPUT1	114
7	Y_INPUT1	115	8	X_INPUT2	116
9	Y_INPUT2	117	10	AN5	118
11	AN6	119	12	AN7	120
13	AN81	121	14	AN91	122
15	AN101	123	16	AN111	124
17	DA2	125	18	DA3	126

Table 9-4: J4A microcontroller header

Header Pin	Circuit Net Name	Device pin	Header Pin	Circuit Net Name	Device pin
1	AN141	127	2	AN151	128
3	AVSS	129	4	TCK	130
5	TMS	131	6	TDI	132
7	IRQ0An_TXD2	133	8	IRQ1An_RXD2	134
9	IRQ2An_SCK2	135	10	TRSTn	136
11	DLCDRS_SCL0	137	12	SCK0_SDA0	138
13	RXD1	139	14	RXD0	140
15	TXD1	141	16	TXD0	142
17	MD0	143	18	MD1	144

Table 9-5: J4B microcontroller header

9.2. Application Headers

Standard application header connections are detailed in **Table 9-6** to **Table 9-10**.

Header Pin	Generic Header Name	RSK board Signal Name	Device Pin	Header Pin	Generic Header Name	RSK board Signal Name	Device pin
1	5V	CON_5V	---	2	0V(5V)	GROUND	---
3	3V3	CON_3V3	---	4	0V(3V3)	GROUND	---
5	AVcc	CON_AVCC	---	6	AVss	AVSS	129
7	AVref	CON_VREF	---	8	ADTRG	ADTRG0Bn	84
9	AD0	AN0	113*	10	AD1	X_INPUT1	114
11	AD2	Y_INPUT1	115	12	AD3	X_INPUT2	116
13	DAC0	DA2	125	14	DAC1	DA3	126
15	IO_0	IO0	104*	16	IO_1	IO1	106*
17	IO_2	IO2	100*	18	IO_3	IO3	101*
19	IO_4	IO4	42*	20	IO_5	IO5	43*
21	IO_6	IO6	57*	22	IO_7	IO7	58*
23	IRQ3	IRQ3Bn	59*	24	IIC_EX	NC	---
25	IIC_SDA	SDA0	138*	26	IIC_SCL	SCL0	137*

Table 9-6: JA1 Standard Generic Header

Header Pin	Generic Header Name	RSK board Signal Name	Device Pin	Header Pin	Generic Header Name	RSK board Signal Name	Device Pin
1	RESn	RESn	92	2	EXTAL	CON_EXTAL	97*
3	NMIn	NMIn	40	4	Vss1	GROUND	---
5	WDT_OVF	TDO	39	6	SCIaTX	TXD0	142
7	IRQ0	IRQ0An	133*	8	SCIaRX	RXD0	140
9	IRQ1	IRQ1An	134*	10	SCIaCK	SCK0	138*
11	UD	NC	---	12	CTSRTS	NC	---
13	Up	NC	---	14	Un	NC	---
15	Vp	NC	---	16	Vn	NC	---
17	Wp	NC	---	18	Wn	NC	---
19	TMR0	TIOCA0	42*	20	TMR1	TIOCB0	43*
21	TRIGa	TIOCC0	44	22	TRIGb	TIOCD0	45
23	IRQ2	IRQ2An	135*	24	TRISTn	NC	---
25	Reserved	NC	---	26	Reserved	NC	---

Table 9-7: JA2 Standard Generic Header

Header Pin	Generic Header Name	RSK board Signal Name	Device Pin	Header Pin	Generic Header Name	RSK board Signal Name	Device Pin
1	A0	BA(0)	---	2	A1	BA(1)	---
3	A2	BA(2)	---	4	A3	BA(3)	---
5	A4	BA(4)	---	6	A5	BA(5)	---
7	A6	BA(6)	---	8	A7	BA(7)	---
9	A8	BA(8)	---	10	A9	BA(9)	---
11	A10	BA(10)	---	12	A11	BA(11)	---
13	A12	BA(12)	---	14	A13	BA(13)	---
15	A14	BA(14)	---	16	A15	BA(15)	---
17	D0	BD(0)	---	18	D1	BD(1)	---
19	D2	BD(2)	---	20	D3	BD(3)	---
21	D4	BD(4)	---	22	D5	BD(5)	---
23	D6	BD(6)	---	24	D7	BD(7)	---
25	RDn	BRDn	---	26	WRn	NC	---
27	CSan	BCS0n*	---	28	CSbn	BCS6n*	---
29	D8	BD(8)	---	30	D9	BD(9)	---
31	D10	BD(10)	---	32	D11	BD(11)	---
33	D12	BD(12)	---	34	D13	BD(13)	---
35	D14	BD(14)	---	36	D15	BD(15)	---
37	A16	BA(16)	---	38	A17	BA(17)	---
39	A18	BA(18)	---	40	A19	BA(19)	---
41	A20	BA(20)	---	42	A21	BA(21)	---
43	A22	BA(22)	---	44	Reserved	NC	---
45	CScn	BCS1n*	---	46	ALE	NC	---
47	HWRn	BHWRn	---	48	LWRn	BLWRn	---
49	Reserved	NC	---	50	Reserved	NC	---

Table 9-8: JA3 Standard Generic Header

Header Pin	Generic Header Name	RSK board Signal Name	Device Pin	Header Pin	Generic Header Name	RSK board Signal Name	Device Pin
1	AD4	Y_INPUT2	117	2	AD5	AN5	118
3	AD6	AN6	119	4	AD7	AN7	120
5	CAN1TX	NC	---	6	CAN1RX	NC	---
7	CAN2TX	NC	---	8	CAN2TX	NC	---
9	Reserved	NC	---	10	Reserved	NC	---
11	Reserved	NC	---	12	Reserved	NC	---
13	Reserved	NC	---	14	Reserved	NC	---
15	Reserved	NC	---	16	Reserved	NC	---
17	Reserved	NC	---	18	Reserved	NC	---
19	Reserved	NC	---	20	Reserved	NC	---
21	Reserved	NC	---	22	Reserved	NC	---
23	Reserved	NC	---	24	Reserved	NC	---

Table 9-9: JA5 Standard Generic Header

Header Pin	Generic Header Name	RSK board Signal Name	Device Pin	Header Pin	Generic Header Name	RSK board Signal Name	Device Pin
1	DREQ	DREQ1n	82*	2	DACK	DACK1n	106*
3	TEND	TEND1n	104*	4	STBYn	STBYn	103
5	RS232TX	RS232TX	---	6	RS232RX	RS232RX	---
7	SCIbRX	RXD2	134*	8	SCIbTX	TXD2	133*
9	SCIcTX	TXD3	33*	10	SCIbCK	SCK2	135*
11	SCIcCK	SCK3	61*	12	SCIcRX	RXD3	59*
13	Reserved	NC	---	14	Reserved	NC	---
15	Reserved	NC	---	16	Reserved	NC	---
17	Reserved	NC	---	18	Reserved	NC	---
19	Reserved	NC	---	20	Reserved	NC	---
21	Reserved	NC	---	22	Reserved	NC	---
23	Reserved	NC	---	24	Reserved	NC	---

Table 9-10: JA6 Standard Generic Header

Note: Pins marked with '*' are connected via option links.

9.3. Generic TFT LCD Header

Generic TFT LCD header connections are detailed in **Table 9-11**.

Header Pin	Generic TFT LCD Header Name	RSK board Signal Name	Device Pin	Header Pin	Generic TFT LCD Header Name	RSK board Signal Name	Device Pin
1	---	5V	---	2	---	5V	---
3	---	Board_VCC	---	4	---	Board_VCC	---
5	NC	NC	-	6	NC	NC	---
7	B1	D(0)	63	8	B2	D(1)	64
9	B3	D(2)	65	10	B4	D(3)	66
11	B5	D(4)	67	12	G0	D(5)	68
13	G1	D(6)	69	14	G2	D(7)	71
15	G3	D(8)	73	16	G4	D(9)	74
17	G5	D(10)	75	18	R1	D(11)	76
19	R2	D(12)	77	20	R3	D(13)	78
21	R4	D(14)	79	22	R5	D(15)	80
23	GPIO0	EDACK2n	60	24	HSYNC	TIOCC0	44
25	DOT CLK	SSCK0A_TIOCA2	48	26	GPIO1	SSO0A_TIOCA1	46
27	VSYNC	TIOCD0	45	28	GPIO2	EDREQ2n	3
29	SSCK	SCK0	138*	30	SSI	RXD0	140
31	SSO	TXD0	142	32	CSn	SCSn	59
33	RESn	RESn	92	34	---	GROUND	---
35	GPIO3	LCD_GPIO3	81	36	GPIO4	LCD_GPIO4_PHI	83*, 94*
37	---	GROUND	-	38	---	GROUND	---
39	---	GROUND	-	40	---	GROUND	---
41	---	XDRIVE	100*	42	---	YDRIVE	101*
43	---	X_INPUT1	114	44	---	Y_INPUT1	115
45	---	X_INPUT2	116	46	---	Y_INPUT2	117

Table 9-11: TFT Header

Note: Pins marked with '*' are connected via option links.

Chapter 10. Code Development

10.1. Overview

Note: For all code debugging using Renesas software tools, the RSK board must be connected to a PC USB port via an E10A.

Due to the continuous process of improvements undertaken by Renesas the user is recommended to review the information provided on the Renesas website at www.renesas.com to check for the latest updates to the Compiler and Debugger manuals.

10.2. Compiler Restrictions

The compiler supplied with this RSK is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the linker will limit the object size to a maximum of 64k code and data. To use the compiler with programs greater than this size you will need to purchase the full tools from your distributor.

Warning: The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

10.3. Breakpoint Support

This RSK is supplied with an E10A emulator which supports breakpoints in ROM and RAM. Double clicking in the breakpoint column in the code sets the breakpoint. Breakpoints will be retained unless they are double clicked to remove them. For more details on breakpoints & E10A functions please refer to the '*E10A-USB Emulator User's Manual*'.

10.4. Event point Support

This RSK is supplied with an E10A emulator which supports event points in ROM. Maximum 6 event points can be placed. For more details on event points & E10A functions please refer to the '*E10A-USB Emulator User's Manual*'.

10.5. Memory Map

The memory map shown below gives the locations of each memory area.

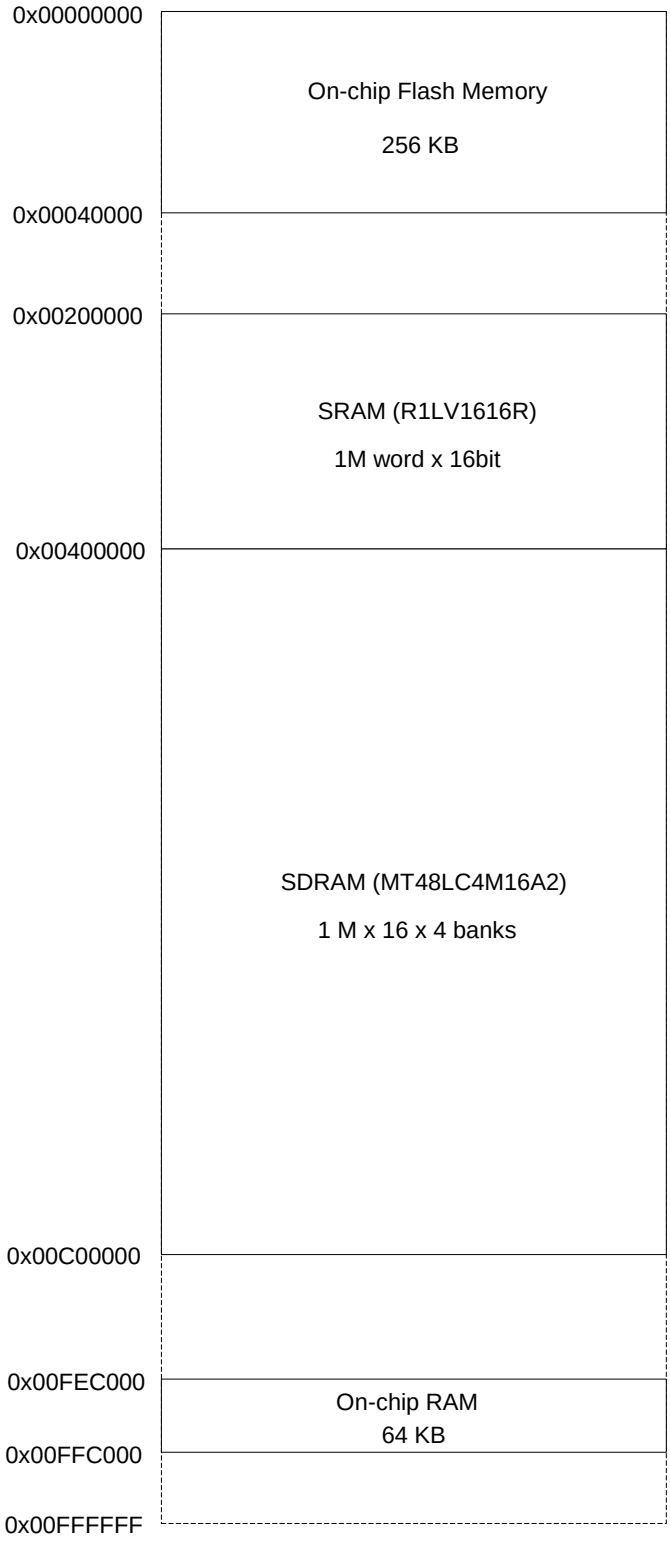


Figure 10-1: RSK2H8S2456R Memory Map

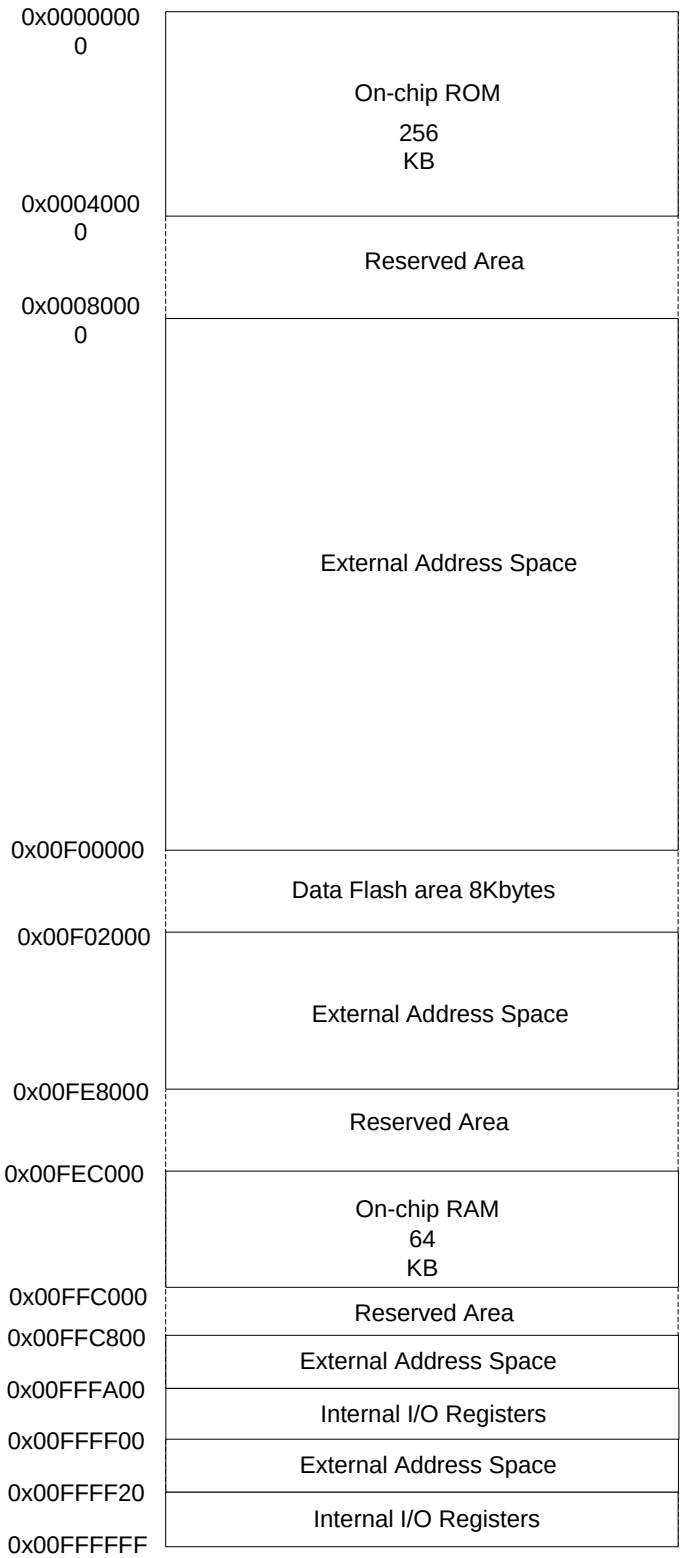


Figure 10-2: CPU memory map (H8S/24569R)

Chapter 11. Component Placement

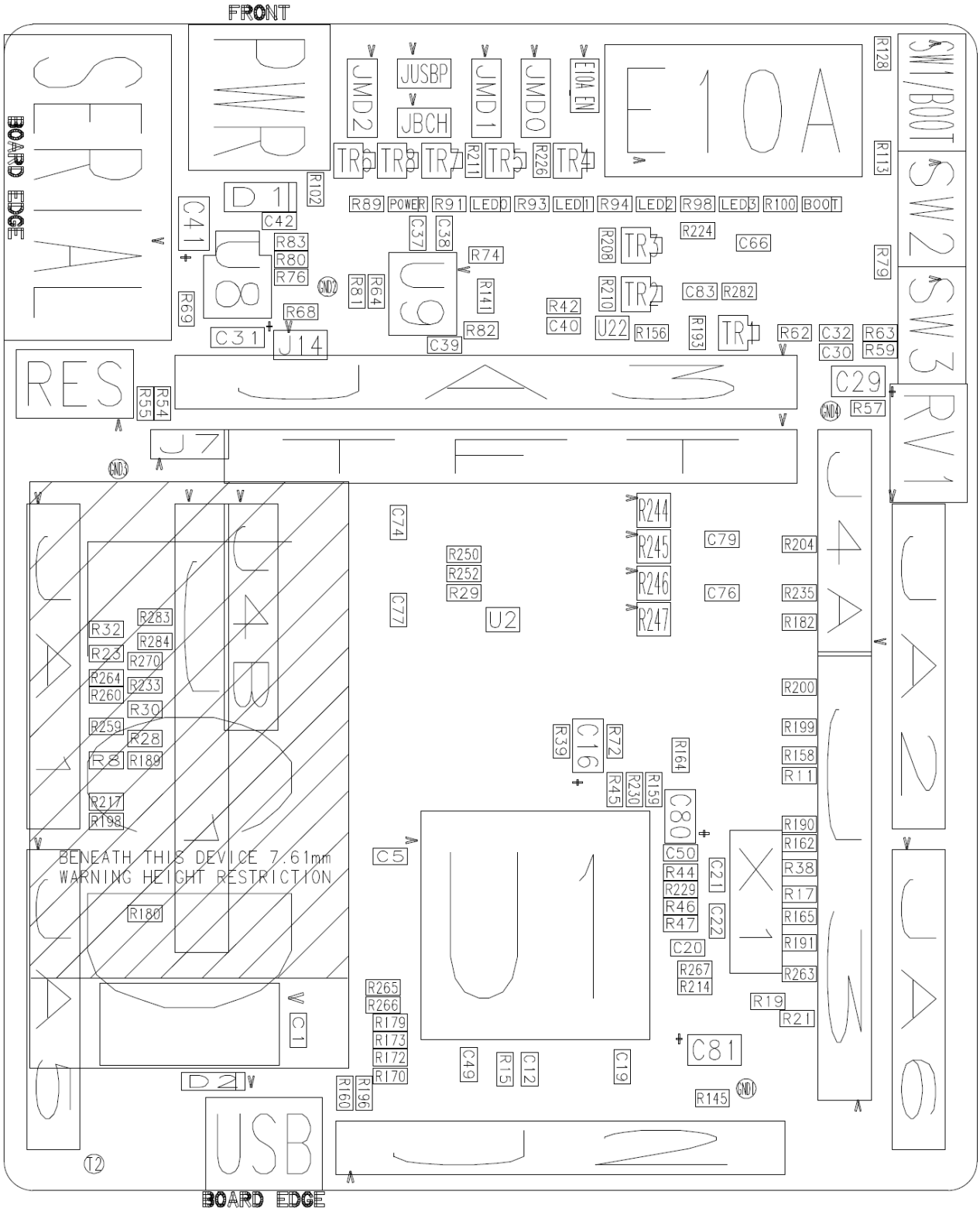


Figure 11-1: Component Placement (Top Layer)

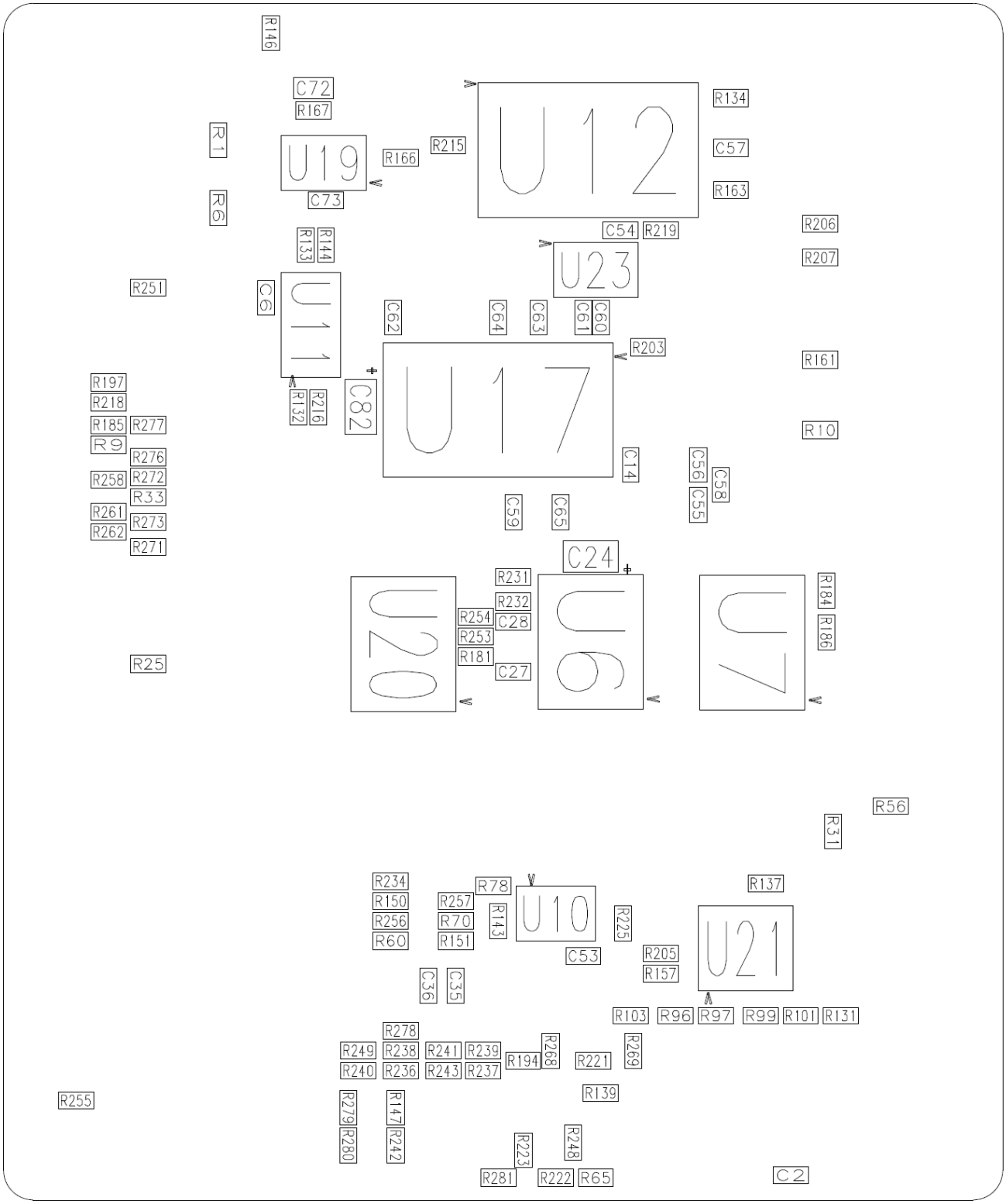


Figure 11-2: Component Placement (Bottom Layer)

Chapter 12. Additional Information

For details on how to use High-performance Embedded Workshop (HEW), refer to the HEW manual available on the CD or installed in the Manual Navigator.

For information about the H8S/2456R microcontrollers refer to the *H8S/2456 Group Hardware Manual*

For information about the H8S/2456R assembly language, refer to the *H8S/2600 Series, H8S/2000 Series Software Manual*

For information about the E10A Emulator, please refer to the *E10A-USB Emulator User's Manual*

Online technical support and information is available at: www.renesas.com/renesas_starter_kits

Technical Contact Details

America: techsupport.rta@renesas.com

Europe: tools.support.eu@renesas.com

Japan: csc@renesas.com

General information on Renesas Microcontrollers can be found on the Renesas website at: www.renesas.com

Renesas Starter Kit for H8S/2456R

User's Manual

Publication Date Rev.1.00 08.APR.2009

Published by: Renesas Technology Europe Ltd.
Duke’s Meadow, Millboard Road, Bourne End
Buckinghamshire SL8 5FH, United Kingdom

Renesas Starter Kit for H8S/2456R
User's Manual

Renesas Electronics Corporation
1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan

REG10J0144-0100