RZ/G3E

AWO Example Program Startup Guide

Introduction

This material shows how to set up and invoke AWO Example Program for RZ/G3E.

Target Device

RZ/G3E

Contents

1. Specifications

1.1 Deliverables

Table 1-1. Deliverables of RZ/G AWO Example Project

Deliverables	File name	Description
RZ/G3E Cortex®-M33 AWO example project	freertos_w_awo_rzg3e_evk_ep.zip	AWO example project for RZ/G3E.
RZ/G3E AWO Example Program Start-up Guide	r01an7882ej0100-rzg3e-awo-example-program-startup-guide.pdf	This material.

2. Proven Environment

Environments	Contents and versions
Integrated Development Environment	e2 studio 2025-07
JTAG Emulator	Segger J-Link 7.96j
Dependent Software	• RZ/G3E Linux BSP v1.0.0 • RZ/G Flexible Software Package (FSP) v3.1.0

3. AWO Example Program Setup for RZ/G3E

3.1 Setup of Cortex-A55 software related stuff

The steps are based on **RZ/G3E-EVKIT Linux Start-up Guide** (hereinafter referred to as **Linux Start-up Guide**) included in **RZ/G3E Linux BSP v1.0.0**.

1. Follow the procedure stated from the beginning of **2.2 Building Images** to **(3) Add layers** of **Linux Start-up Guide**.
2. Download Multi-OS Package (r01an5869ej0300-rzg-multi-os-pkg.zip) to a working directory and run the commands stated below:

```
cd ~/rzg_vlp_<pkg ver>
$ unzip <Multi-OS Dir>/r01an5869ej0300-rzg-multi-os-pkg.zip
$ tar zxvf r01an5869ej0300-rzg-multi-os-pkg/meta-rz-features_multi-os_v3.0.0.tar.gz
```

Here, <Multi-OS Dir> indicates the path to the directory where Multi-OS Package is placed.

3. Uncomment the following lines in **meta-rz-features/meta-rz-multi-os/meta-rzg3e/conf/layer.conf**.

```
MACHINE_FEATURES_append = " RZG3E_CM33_BOOT"
#MACHINE_FEATURES_append = " CM33_FIRMWARE_LOAD"
#MACHINE_FEATURES_append = " CA55_CPU_CLOCKUP"
```

   Be sure NOT to uncomment the above-mentioned 3rd and 4th line when CM33 cold boot support is enabled.

4. Add the layer for Multi-OS Package.

```
$ cd build
$ bitbake-layers add-layer ../meta-rz-features/meta-rz-multi-os/meta-rzg3e
```

5. Start a build as described in **(5) Start a build** of **2.2 Building Images** as shown below:

```
$ MACHINE=smarc-rzg3e bitbake core-image-<target>
```

For details on the allowable value of <target>, please refer to **Linux Start-up Guilde**.

3.2 Deployment of CA55 Build Artifacts

1. Connect SER3_UART of RZG3E SMARC EVK with Host PC and established serial port connection.
2. Configure DIPSW of RZ/G3E SMARC EVK as follows, to specify CA55 cold boot and SCIF download mode.

BOOT

	1	2	3	4	5	6
ON						
OFF	■	■	■	■	■	■

SW_MODE

	1	2	3	4
ON		■		■
OFF	■		■	

3. Turn on RZ/G3E SMARC EVK. Then, the following message is shown on your terminal:

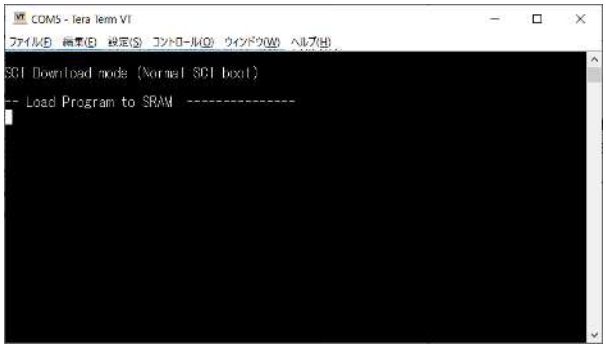

Figure 5-3. SCIF Download mode

4. Send **Flash_Writer_SCIF_RZG3E_EVK_LPDDR4X.mot** to RZ/G3E SMARC EVK via terminal software. If it's successfully transferred, the following message is shown on your terminal:

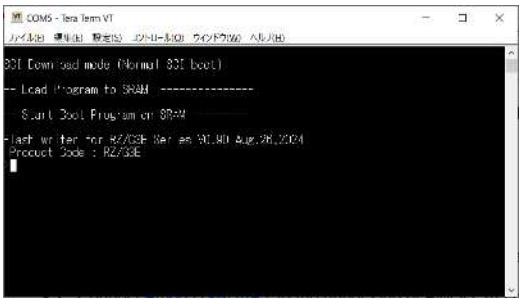

Figure 5-4. Flash Writer invocation

5. Program **bl2_bp_spi-smarc-rzg3e.srec** with Flash Writer as shown below:

```
xls2
===== Qspi writing of RZ/G2 Board Command =============
Load Program to Spiflash
Writes to any of SPI address.
Program size & Qspi Save Address
===== Please Input Program Top Address ============
  Please Input : H'8003600

===== Please Input Qspi Save Address ===
  Please Input : H'100000
please send ! ('.' & CR stop load)
Erase SPI Flash memory...
Erase Completed
Write to SPI Flash memory.
======= Qspi  Save Information  =================
SpiFlashMemory Stat Address : H'00100000
SpiFlashMemory End Address  : H'00136D17
============================================================
```

6. Program **fip-smarc-rzg3e.srec** with Flash Writer as shown below:

```
xls2
===== Qspi writing of RZ/G2 Board Command =============
Load Program to Spiflash
Writes to any of SPI address.
Program size & Qspi Save Address
===== Please Input Program Top Address ============
  Please Input : H'00000

===== Please Input Qspi Save Address ===
  Please Input : H'160000
please send ! ('.' & CR stop load)
Erase SPI Flash memory...
Erase Completed
Write to SPI Flash memory.
======= Qspi  Save Information  =================
SpiFlashMemory Stat Address : H'00280000
SpiFlashMemory End Address  : H'0033C2BE
============================================================
```

3.3 Setup of CM33 software related stuff

1. Extract **r01an5869ej0300-rzg-multi-os-pkg.zip** on your development PC.
2. Extract either of **freertos_w_awo_rzg3e_evk_ep.zip** included in **r01an5869ej0300-rzg-multi-os-pkg**.
3. Invoke e^2 studio 2025-07 and click **File** > **Import**.
4. Double-click **General** and select **Existing Projects into Workspace** as shown in Figure 3-1:

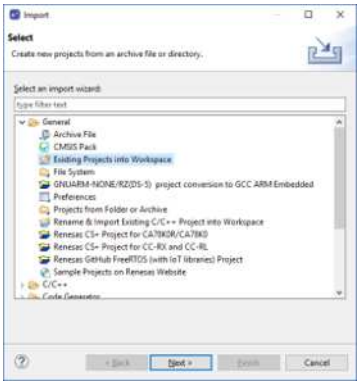

Figure 3-1. Import sample project (1)

5. Input the path to the directory of sample project you would like to import to **Select root directory**, press **Enter** key and click **Finish** button.

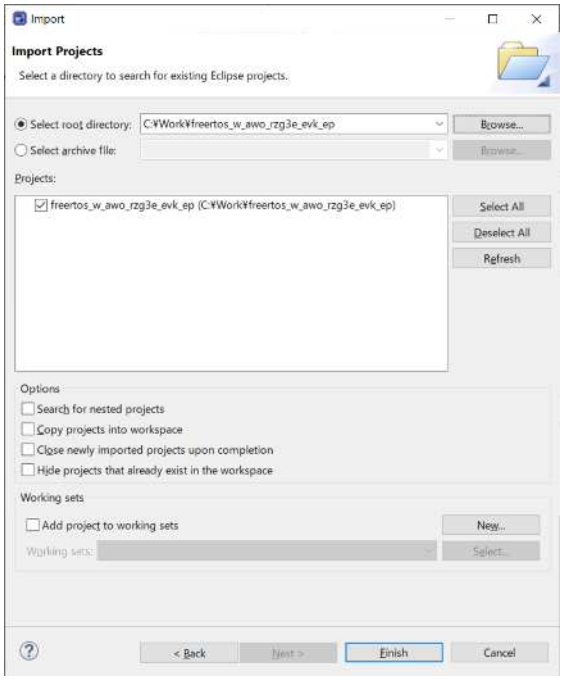

Figure 3-2. Import sample project (2)

6. Open **configurator.xml** in the project and choose **BSP** tab.
7. Configure **Launch CA55(core0)** as Enabled. Also, enabled **Clock up for CA55** if you would like to configure operational frequency of CA55 as 1.8GHz.
8. Click **Generate Project Content** to reflect the changes to your project.

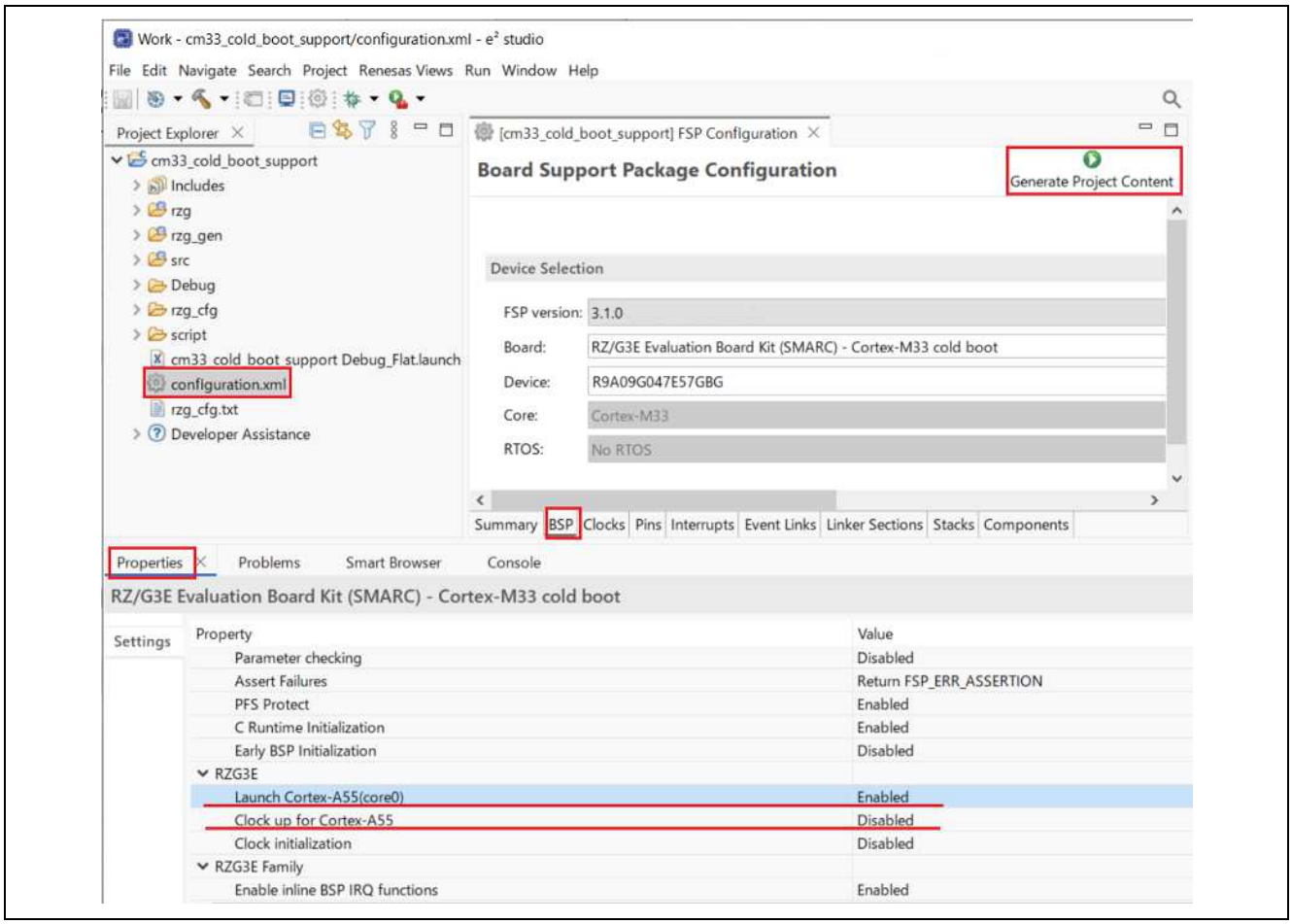

Figure 3-3. CM33 project setting for CM33 cold boot

9. Build the project from **Choose Project** > **Build Project**.
10. If building project is successfully completed, build artifacts as listed below should be generated in **Debug** or **Release** directory of the project you imported in accordance with the active Build Configuration.
    - freertos_w_awo_rzg3e_evk_ep.elf

3.4 Deployment and debugging of AWO Example program

1. Click **Run** > **Debug Configurations...** , expand **Renesas GDB Hardware Debugging** and choose **freertos_w_awo_rzg3e_evk_ep Debug_Flat**.

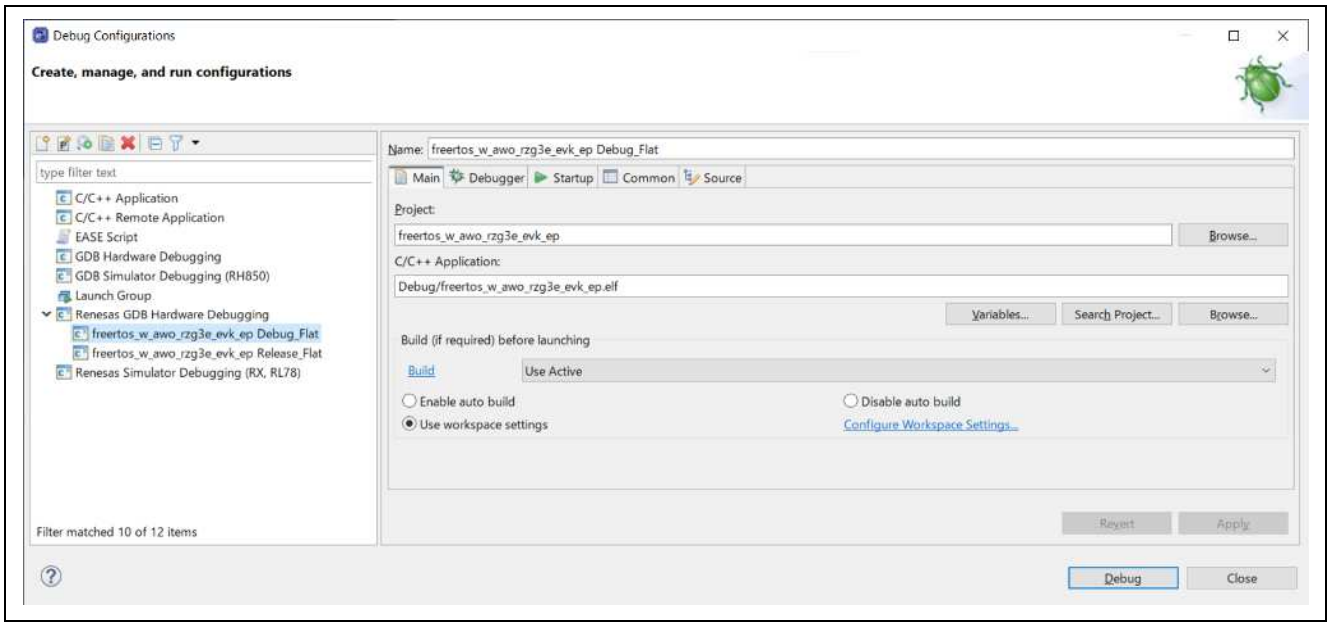

Figure 3-4. Debug Configuration Launch

(Optional)

2. Create a CA55_SREC folder directly under the project. Then copy the files used in **3.2 Deployment of CA55 Build Artifacts** into the folder.

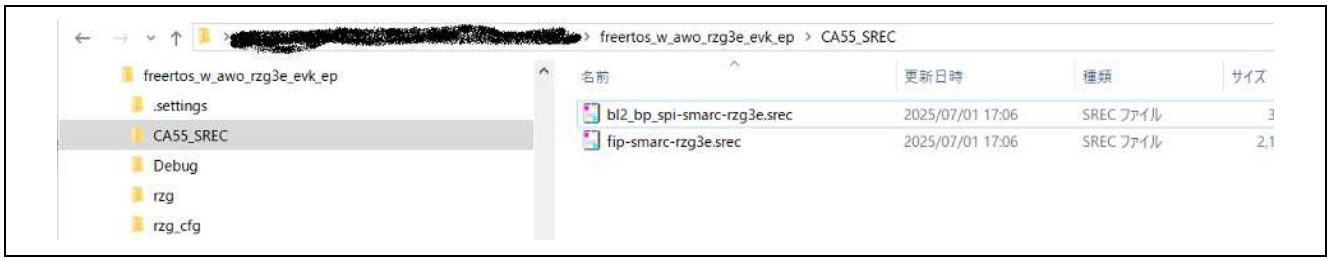

Figure 3-5. Copy of CA55 build artifacts

(Optional)

3. Check the following boxes in the debugger connection settings. Then the files copied in Step 2 will be written at the same time.

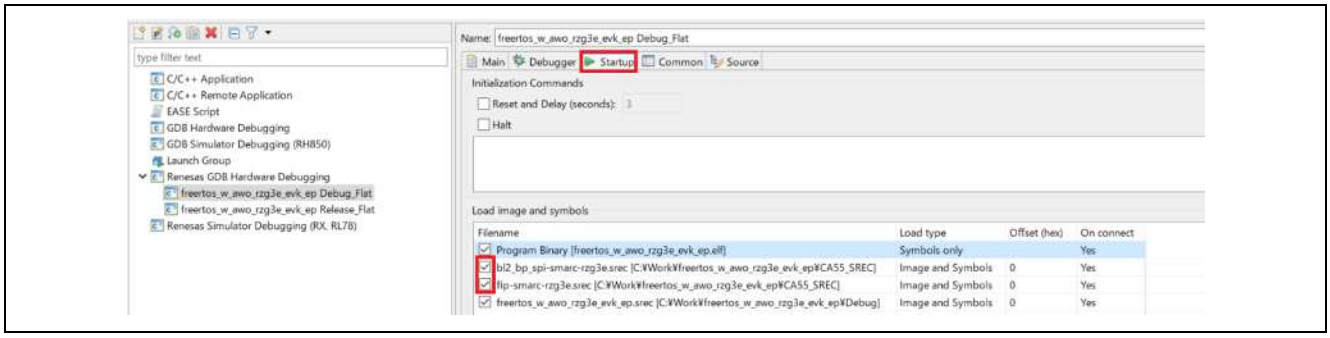

Figure 3-6. Specify the download of additional files

4. Click **Debug** button as shown below:

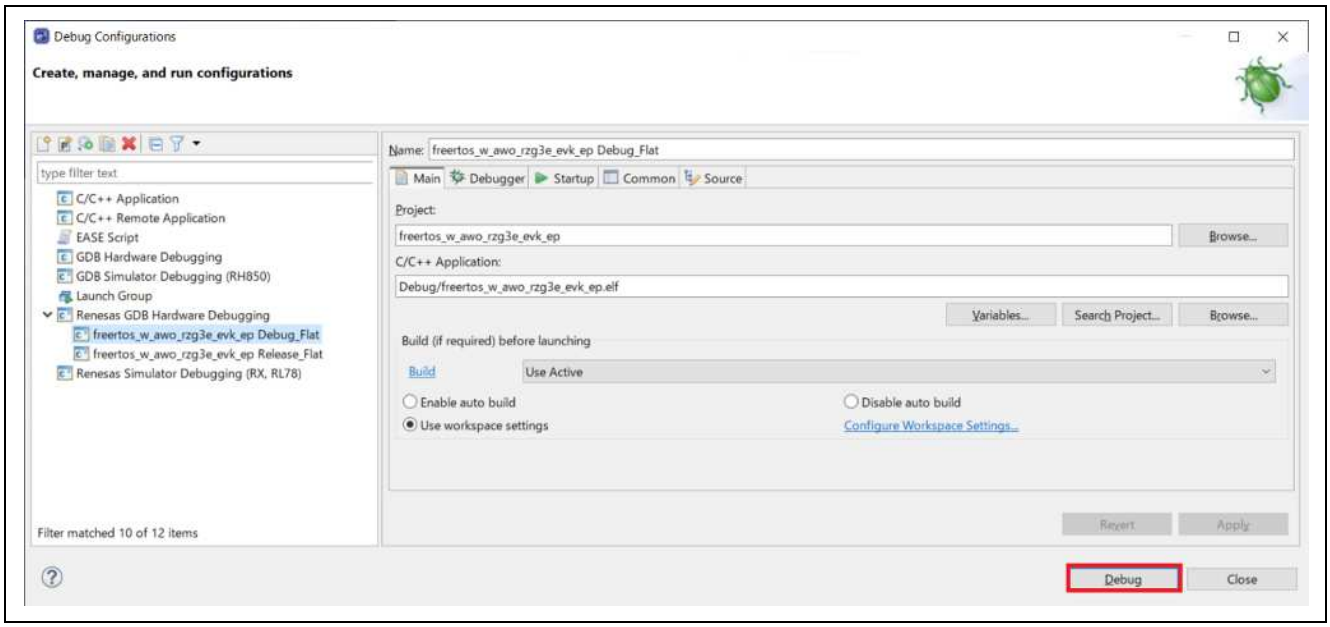

Figure 3-7. Debug Perspective Launch (1)

Note1: Configure DIPSW of RZ/G3E SMARC EVK as follows, to specify CM33 cold boot and SPI boot mode in advance.

BOOT

	1	2	3	4	5	6
ON		■				
OFF	■		■	■	■	■

SW_MODE

	1	2	3	4
ON				■
OFF	■	■	■	

If the following **Confirm Perspective Switch** window appears, press **Switch** to go ahead.

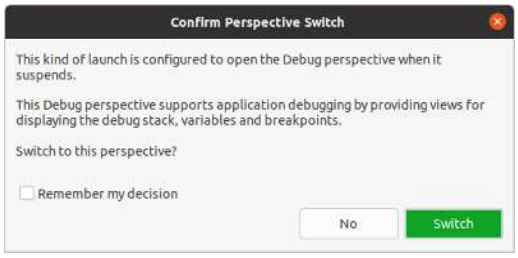

Figure 3-8. Debug Perspective Launch (3)

4. When **Debug Perspective** is opened, Program Counter (PC) should be located as shown in Figure 3-9. Then, continue the program to push the button shown in Figure 3-9.

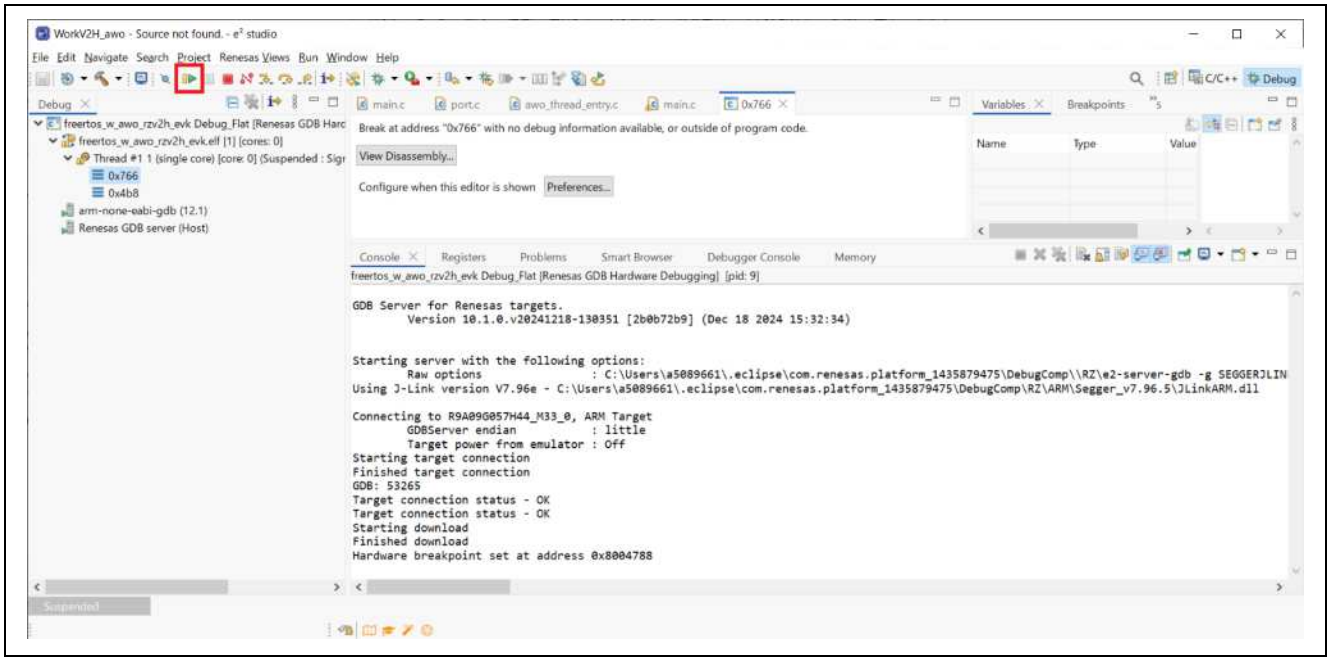

Figure 3-9. How to start to AWO Example Program (1)

5. PC should be stopped at the top of **main** function. Then, click the same button in the previous step to continue.

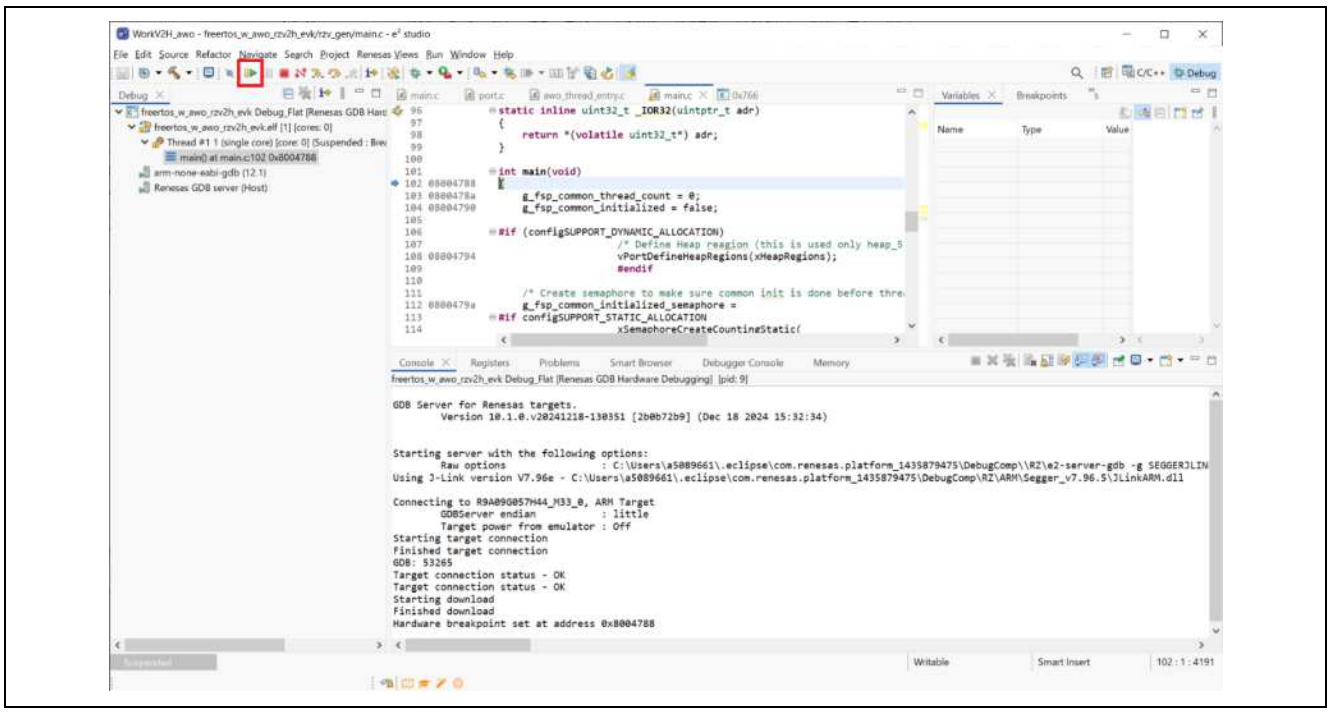

Figure 3-10. How to start to AWO Example Program (2)

CM33 AWO example program now starts, loads CA55 build artifacts and kick CA55.

4. AWO Example Program Invocation

This chapter describes how AWO Example Program works.

1. Boot up Linux kernel.
2. Login as **root**.

```
smarc-rzg3e login: root
```

3. Load **AWO Notifier** which notifies CM33 that CA55 becomes ready to enter AWO.

```
root@smarc-rzg3e:~# insmod ./awo-notifier.ko
```

4. Issue shutdown command as shown below:

```
root@smarc-rzg3e:~# shutdown -h now
```

   While CA55 is being shut down, AWO Notifier fires an external interrupt.
5. Once CM33 AWO example project detects the external interrupt, RZ/G3E is configured as AWO. Then, the following message is shown on your console:

```
CM33: AWO request accept.
Hit any key to go to ALLON mode.
```

6. When hitting any key on your development PC, CM33 AWO example project configures RZ/G3E as ALLON, load BL2 of TrustedFirmware-A to internal SRAM and kick CA55 for restart.

```
CM33: Set GreenPAK to ALLON
```

5. Function Reference of AWO Example Project

5.1.1 awo_thread_entry

```
void awo_thread_entry (void *pvParameters)
```

- **Parameters**
  - pvParameters
    Pointer to the parameter passed to AWO task.

- **Returns**
  None

- **Description**
  This function is the entry function of AWO thread.
  Here is the overview of processing flow:
  1. Wait for notification of shutdown from Arm® Cortex®-A55 (hereinafter referred to as CA55) Linux.
  2. Configure RZ/G3E and PMIC as AWO.
  3. Wait until key input to console is issued.
  4. Configure RZ/G3E and PMIC as ALLON.
  5. Return to 1.

5.1.2 awo_req_isr

```
void awo_req_isr (void)
```

- **Parameters**
  - None

- **Returns**
  None

- **Description**
  This function is an interrupt handler that receives inter-core interrupts from CA55.

5.1.3 transition_to_awo

```
static void transition_to_awo(void)
```

- **Parameters**
  None

- **Returns**
  None

- **Description**
  Transitioning the Power Mode of the RZ/G3E from ALL_ON to AWO.

5.1.4 transition_to_all_on

```
static void transition_to_all_on(void)
```

- **Parameters**
  None

- **Returns**
  None

- **Description**
  Transitioning the Power Mode of the RZ/G3E from AWO to ALL_ON.

5.1.5 pmic_sleep_to_active

```
fsp_err_t pmic_sleep_to_active(void)
```

- **Parameters**
  None

- **Returns**
  Returns a FSP_SUCCESS upon successful completion.
  If an error occurs in I2C communication, the error code returned by the I2C driver is returned.

- **Description**
  Configure Power/Reset control IC GreenPAK SLG7RN47054 mounted on RZ/G3E SMARC EVK specific to AWO mode.

5.1.6 cluster_warm_reset_ca55

```
void cluster_warm_reset_ca55(void)
```

- **Parameters**
  None

- **Returns**
  None

- **Description**
  Carry out Normal Reset Procedure of CA55.

5.1.7 release_cluster_warm_reset_ca55

```
void release_cluster_warm_reset_ca55(void)
```

- **Parameters**
- None

- **Returns**
  None

- **Description**
  Carry out Normal Reset Release and Core 0 Startup Procedure of CA55.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul 22, 2025	-	First edition.

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2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
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   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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