IS-1715AEH

Total Dose Test Report

This report documents the results of Low Dose Rate (LDR) total dose testing of the IS-1715AEH, Radiation Hardened Complementary Switch FET Driver. The tests were conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of bias sensitivity. Parts were irradiated biased and unbiased at LDR (0.01rad(Si)/s) to 100krad(Si). The IS-1715AEH is rated to 50krad(Si) at LDR.

Product Description

The radiation hardened IS-1715AEH, built in the dielectrically isolated Rad Hard Silicon Gate (RSG) process, is a high speed, high current, complementary power FET driver designed for use in synchronous rectification circuits. Soft switching transitions for the two output waveforms can be managed by setting the independently programmable delays. Alternatively, the delay pins can be configured for zero-voltage sensing to allow for precise switching control.

The IS-1715AEH has a single input, which is PWM and TTL compatible, and can run at frequencies up to 1MHz. The AUX output switches immediately at the rising edge of the INPUT but waits for the T2 delay before responding to the falling edge. A logic low on the enable pin (ENBL) places both outputs into an active-low mode, and an Undervoltage Lockout (UVLO) function is set at 9V (maximum).

The block diagram for the IS-1715AEH is shown in Figure 1.

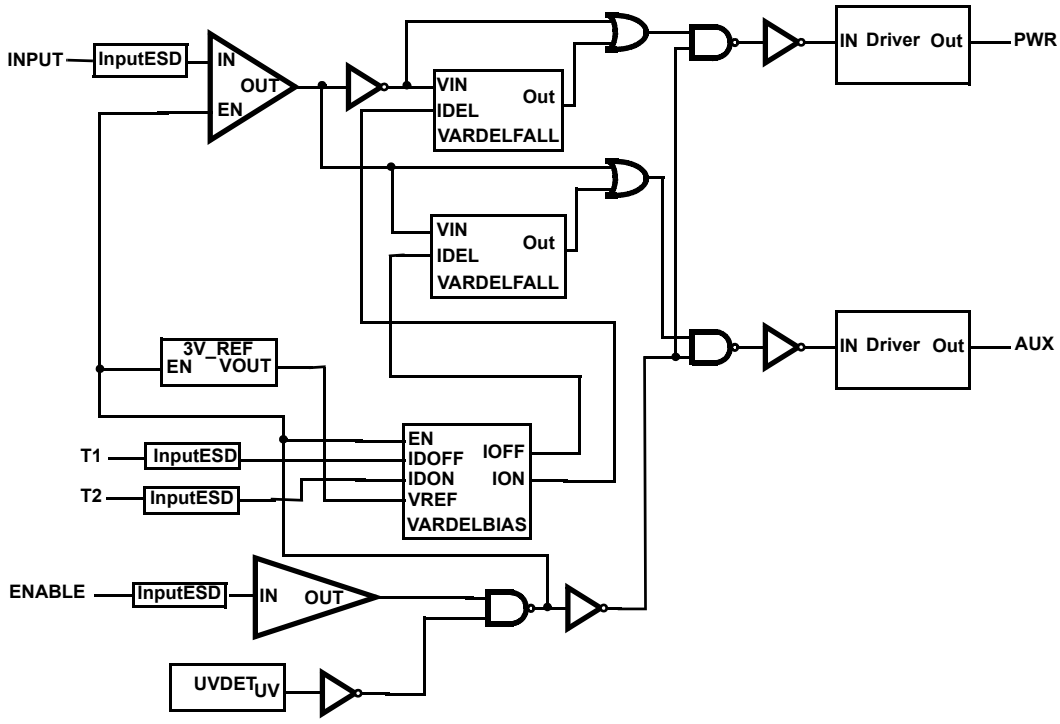

Figure 1. IS-1715AEH Block Diagram

Related Information

For a full list of related documents, visit our website:

- MIL-STD-883 Test Method 1019
- IS-1715AEH device page

The pin configuration for the IS-1715AEH is shown in Figure 2 with the pin descriptions shown in Table 1.

Flatpack (CDFP4-F16)

Top View

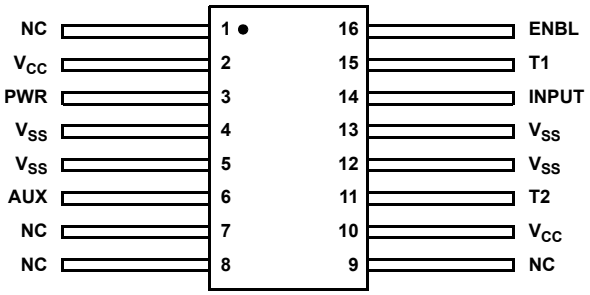

Figure 2. IS-1715AEH Package and Pin Configuration

Table 1. IS-1715AEH Pin Descriptions

Pin Number	Pin Name	Description
1, 7, 8, 9	NC	No connection.
2, 10	V_{CC}	Chip positive supply (10V to 18V).
3	PWR	Output. PWR switches immediately (neglecting propagation delay) at the falling edge of the INPUT but is delayed after the rising edge by the value of the resistance on T1. PWR is capable of sinking and sourcing 3.0A of peak gate drive current. During sleep mode, PWR is active low.
4, 5, 12,13	V_{SS}	Chip negative supply (ground connection).
6	AUX	Output. AUX switches immediately (neglecting propagation delay) at the rising edge of the INPUT but is delayed after the falling edge before switching by the value of the resistance on T2. AUX is capable of sinking and sourcing 3.0A of peak gate drive current. During sleep mode, AUX is active low.
11	T2	Input. A resistor to ground programs the time delay between PWR switch turn-off and AUX turn-on.
14	INPUT	Input. INPUT switches at TTL logic levels but the allowable range is from 0V to VCC, allowing direct connection to most common IC PWM controller outputs. The rising edge immediately switches the AUX output, and initiates a timing delay, T1, before switching on the PWR output. Similarly, the INPUT falling edge immediately turns off the PWR output and initiates a timing delay, T2, before switching the AUX output.
15	T1	Input. A resistor to ground programs the time delay between AXU switch turn-off and PWR turn-on.
16	ENBL	Input. The ENABLE input switches at TTL logic levels, but the allowable range is from 0 to VCC. The ENABLE input places the device into sleep mode when it is a logic low. The current into VCC during sleep mode is typically 500µA.
N/A	LID	No connection (floating).

1. Test Description

1.1 Irradiation Facilities

The irradiation was performed at 0.01rad(Si)/s using the Renesas Palm Bay Hopewell Designs N40 panoramic commercial irradiator. This irradiator uses PbAl spectrum hardening filters to shield the test board and devices under test against low energy secondary gamma radiation.

1.2 Test Fixturing

Figure 3 shows the configuration used for biased irradiation.

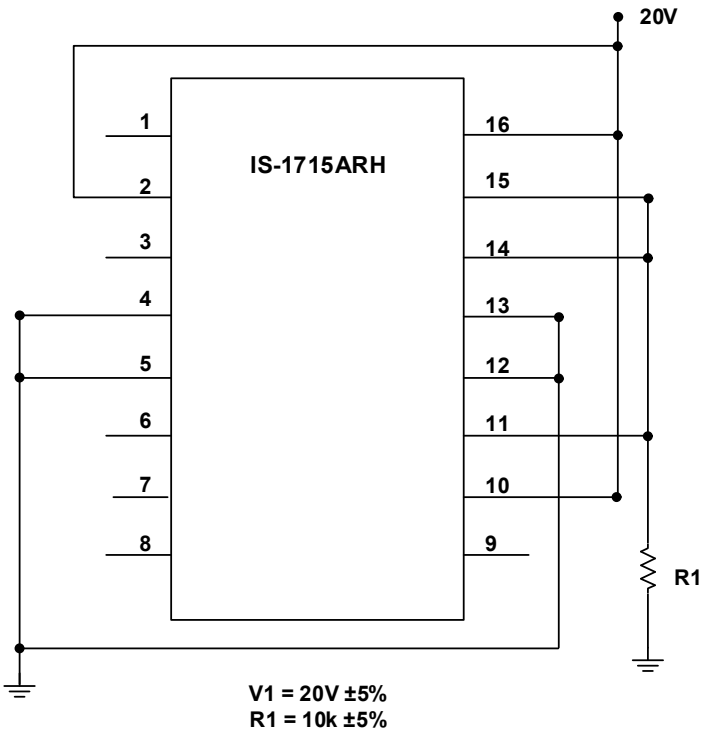

Figure 3. IS-1715AEH TID Bias Schematic

1.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator, using production Automated Test Equipment (ATE) with data logging at each downpoint.

1.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 34 samples irradiated under bias and 34 samples irradiated with all pins grounded.

The IS-1715AEH samples were drawn from wafer lot G2M8MBA (Tracecode - G2M8MBAEH). All samples were packaged in the standard 16 pin CDFP package (PKG Code CDFP4-16). Samples were processed through the standard burn-in cycle before irradiation.

1.5 Downpoints

Downpoints for the tests were 0, 10, 30, 50, and 100krad(Si). For unknown reasons, the 10krad(Si) data for the grounded parts did not get recorded, but all parts passed at the next downpoint of 30krad(Si). The data are extrapolated as a continuous line in the graphs.

2. Test Results

2.1 Attributes Data

Total dose testing of the IS-1715AEH was completed. All tested parameters passed the SMD limits. Table 2 summarizes the results.

Table 2. IS-1715AEH Total Dose Test Attributes Data

Dose Rate (Rad(Si)/s)	Condition	Sample Size	Downpoint	Pass[1]	Fail
0.01	Biased (Figure 3)	34	Pre-irradiation	34	
			10krad(Si)	34	0
			30krad(Si)	34	0
			50krad(Si)	34	0
			100krad(Si)	34	0
0.01	GND	34	Pre-irradiation	34	
			10krad(Si)	N/A	N/A
			30krad(Si)	34	0
			50krad(Si)	34	0
			100krad(Si)	34	0

1. A *Pass* indicates a sample that passes all post-irradiation SMD limits. *N/A* = Data not available, but parts passed next downpoint

2.2 Key Parameter Variables Data

The plots in Figure 4 through Figure 21 illustrate the TID response of selected parameters as shown in Table 3 in the Appendix. The plots show the average tested values of the key parameters as a function of total dose for both conditions, biased and grounded. The plots also include error bars at each downpoint, representing the minimum and maximum measured values of the samples, although in some plots the error bars are not visible because of their values compared to the scale of the graph.

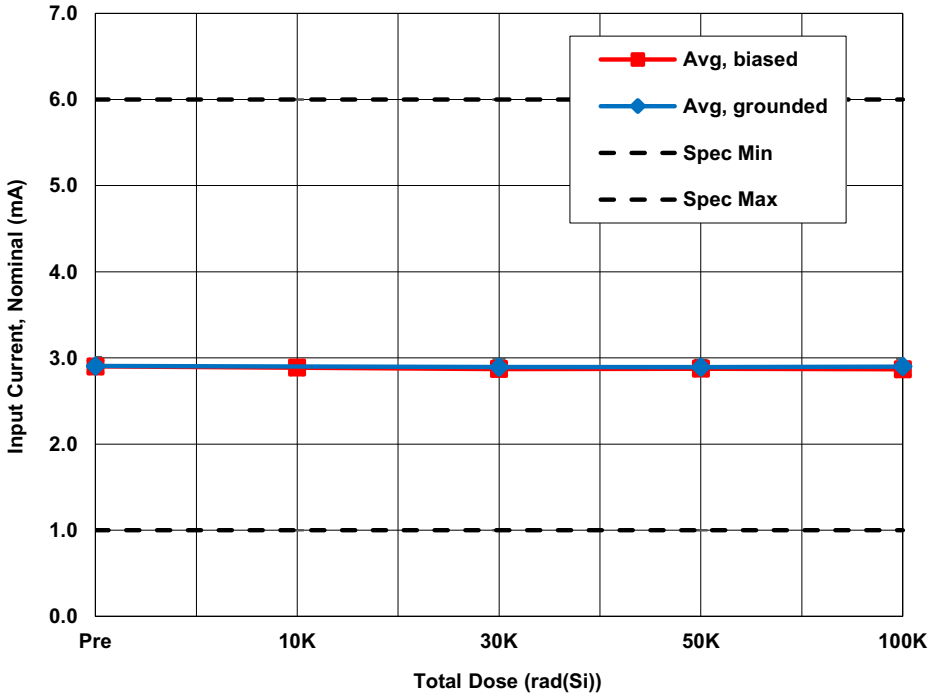

Figure 4. IS-1715AEH average input current, nominal (I_{CC}) with V_{CC} = 18V and ENBL = 3V as a function of LDR irradiation. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 1mA minimum and 6mA maximum.

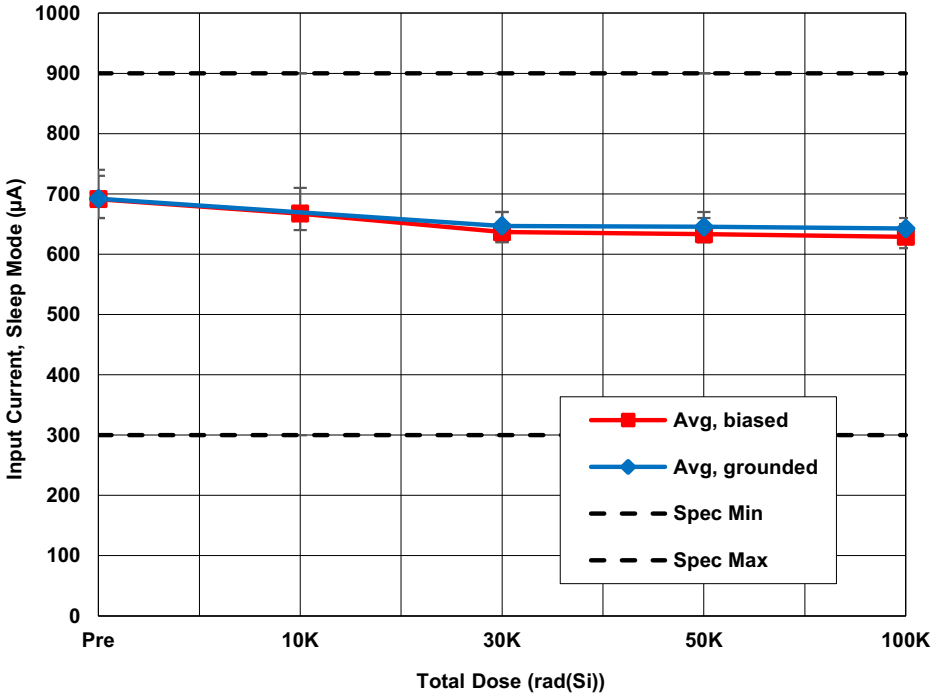

Figure 5. IS-1715AEH average input current, sleep mode (I_{CCS}) with V_{CC} = 18V and ENBL = 0.8V as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limits are 300µA minimum and 900µA maximum.

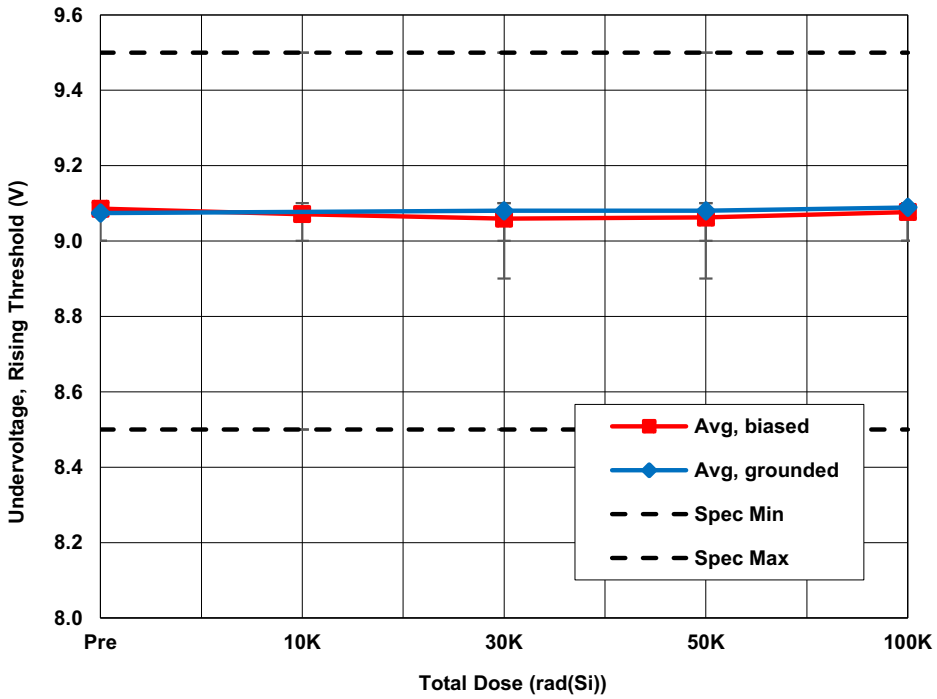

Figure 6. IS-1715AEH average undervoltage, rising threshold (UV+) as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limits are 8.5V minimum and 9.5V maximum.

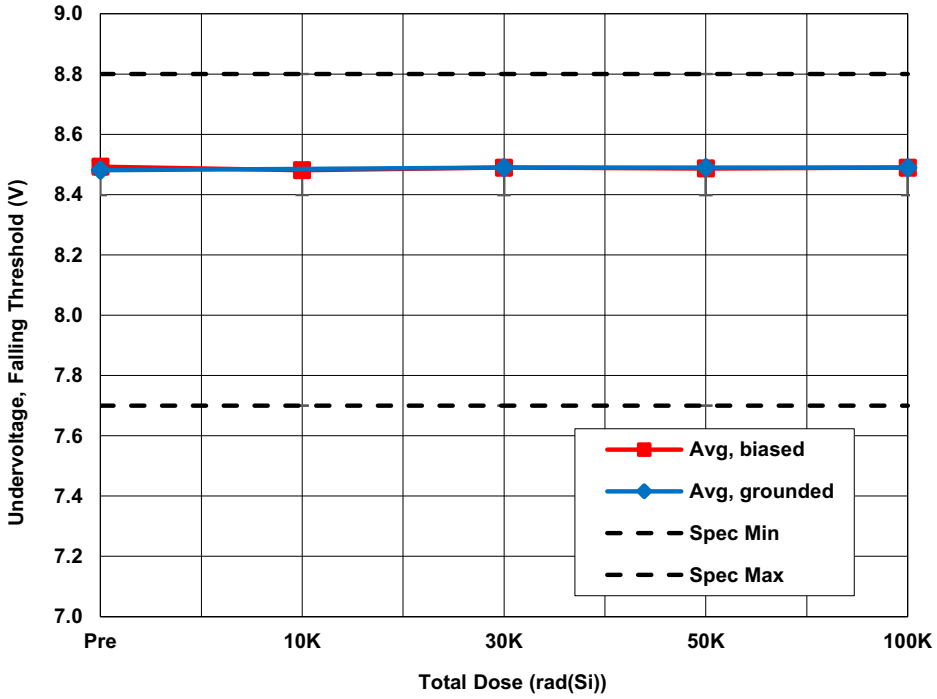

Figure 7. IS-1715AEH average undervoltage, falling threshold (UV-) as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limits are 7.7V minimum and 8.8V maximum.

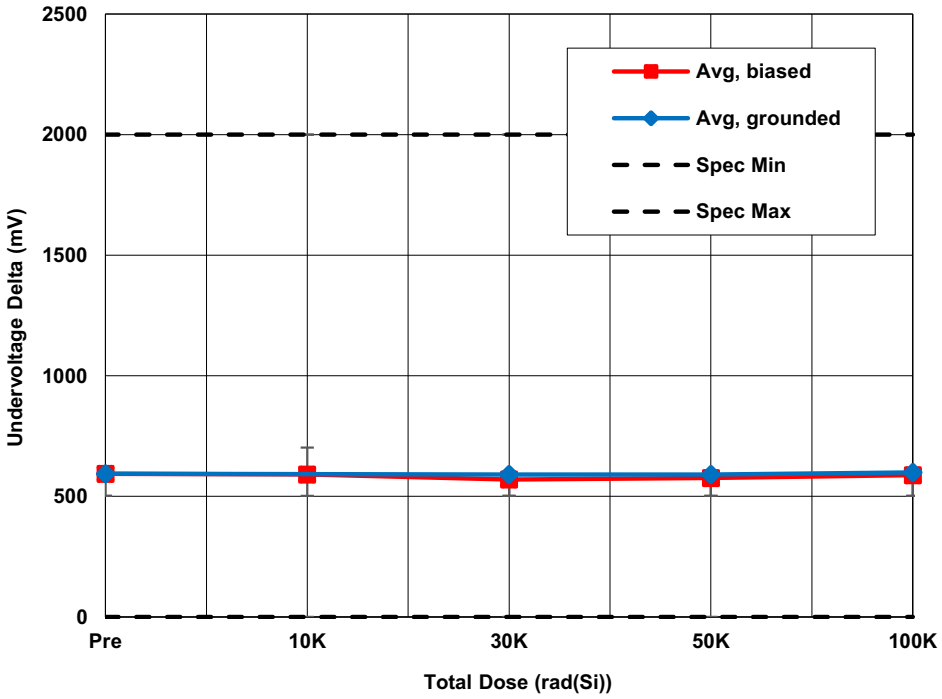

Figure 8. IS-1715AEH average undervoltage delta (UVD) as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limits are 0V minimum and 2V maximum.

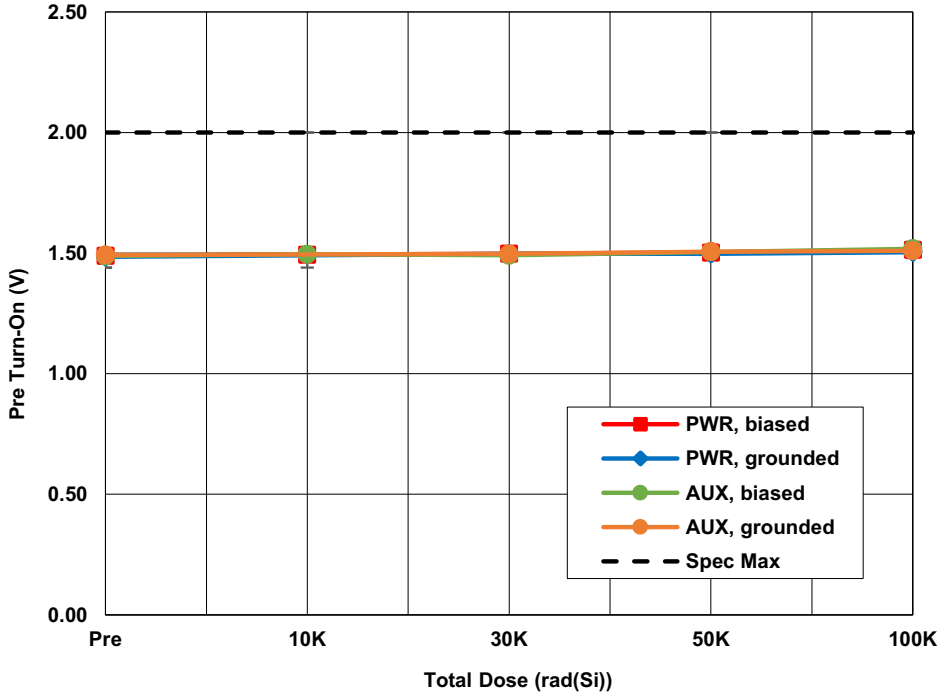

Figure 9. IS-1715AEH average pre turn-on voltage PWR output, low (V_{PPWR}) with V_{CC} = 0V, ENBL = 0.8V, and I_{OUT} = 10mA as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limit is 2.0V maximum.

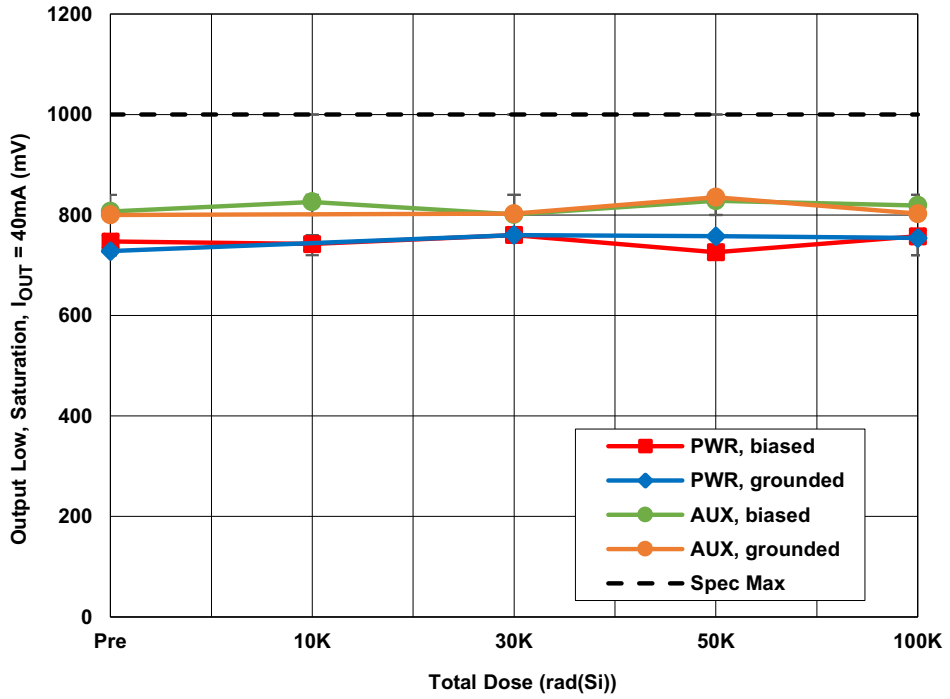

Figure 10. IS-1715AEH average PWR pin output low voltage, saturation (V_{PWR}) with INPUT = 0.8V, I_{OUT} = 40mA as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limit is 1.0V maximum.

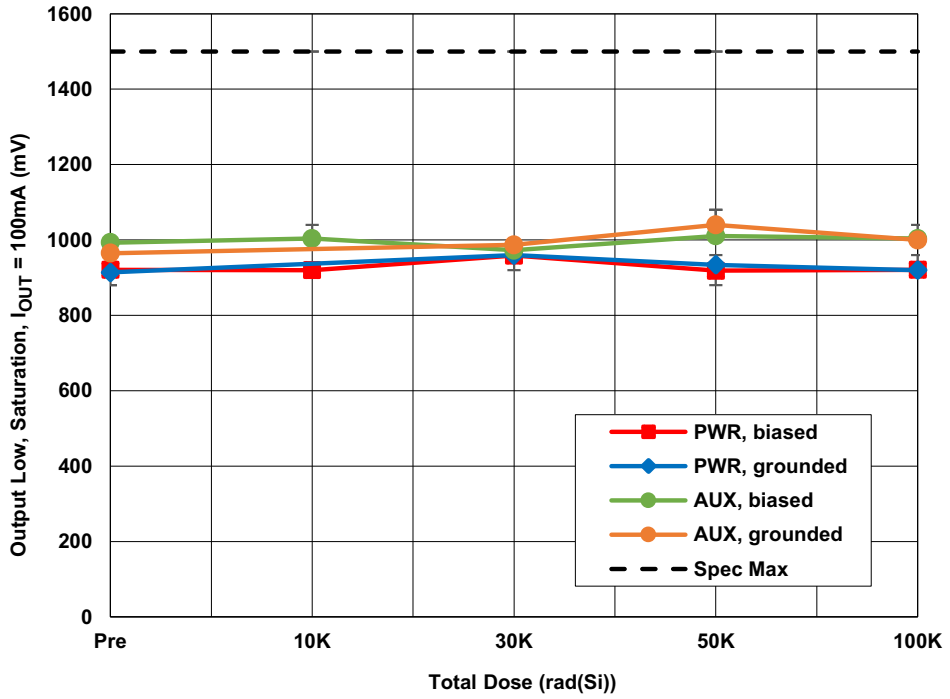

Figure 11. IS-1715AEH average PWR pin output low voltage, saturation (V_{PWR}) with INPUT = 0.8V, I_{OUT} = 100mA as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limit is 1.5V maximum.

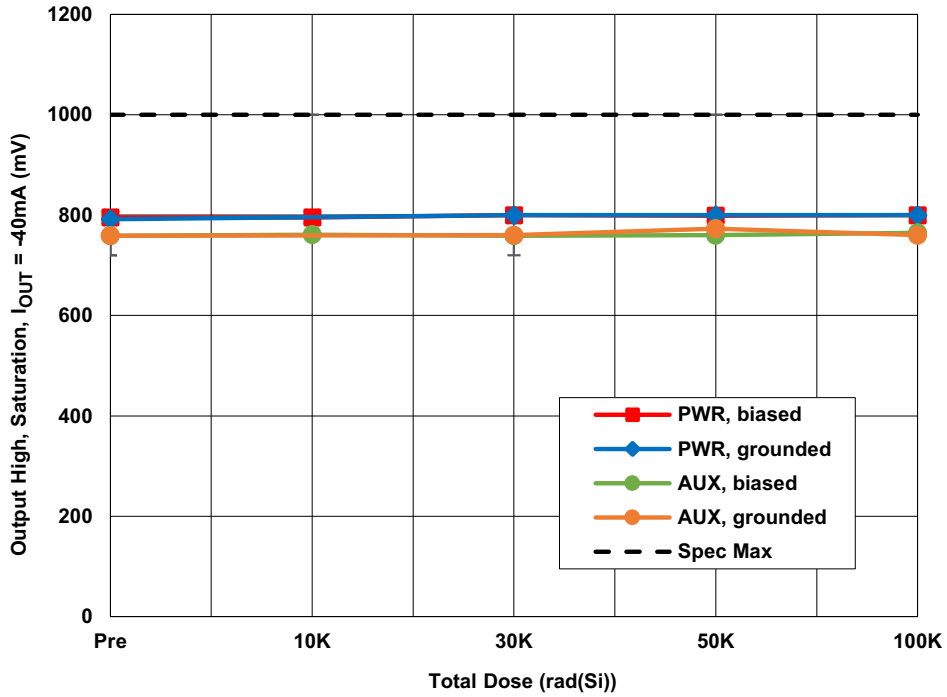

Figure 12. IS-1715AEH average PWR pin output high voltage, saturation (V_{CC} - V_{PWR}) with INPUT = 3.0V, I_{OUT} = -40mA as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limit is 1.0V maximum.

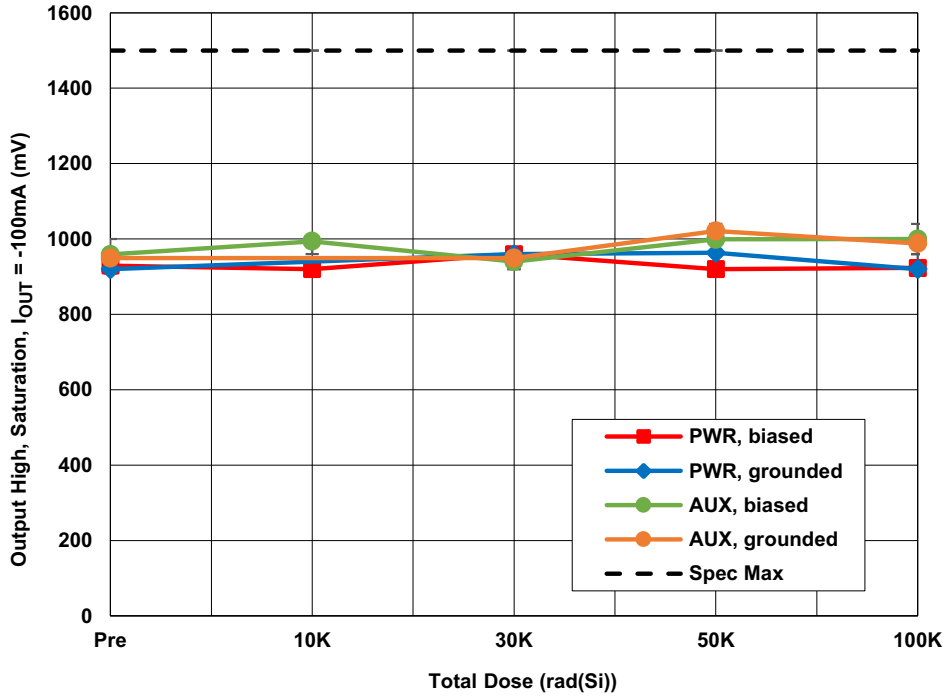

Figure 13. IS-1715AEH average PWR pin output low voltage, saturation (V_{CC} - V_{PWR}) with INPUT = 3.0V, I_{OUT} = -100mA as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limit is 1.5V maximum.

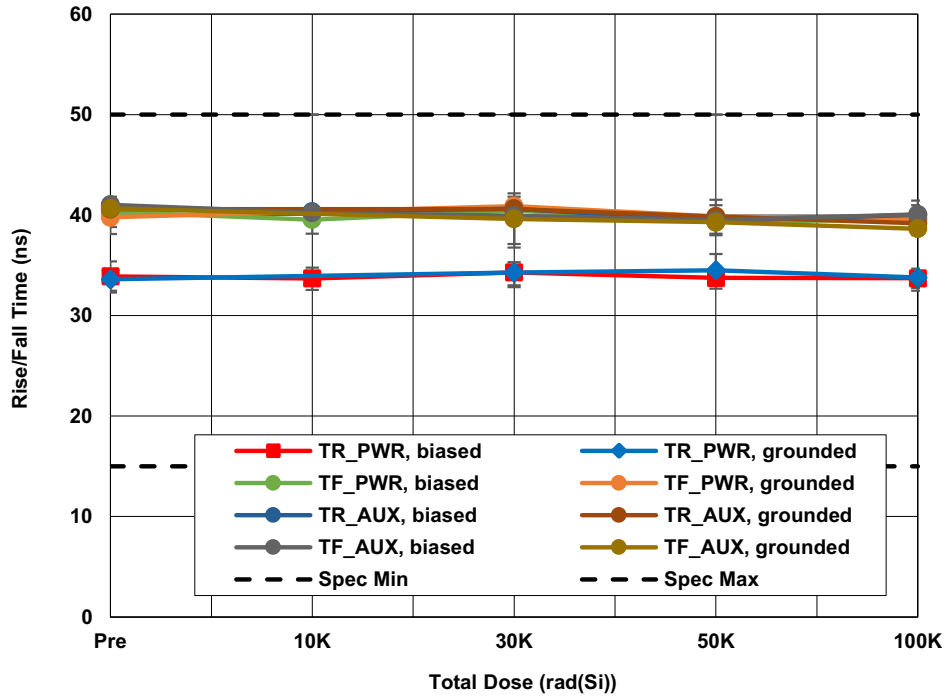

Figure 14. IS-1715AEH average rise (T_{RP}) and fall (T_{FP}) times of PWR and AUX with V_{CC} = 10V and C_L = 2200pF as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limits are 15ns minimum and 50ns maximum.

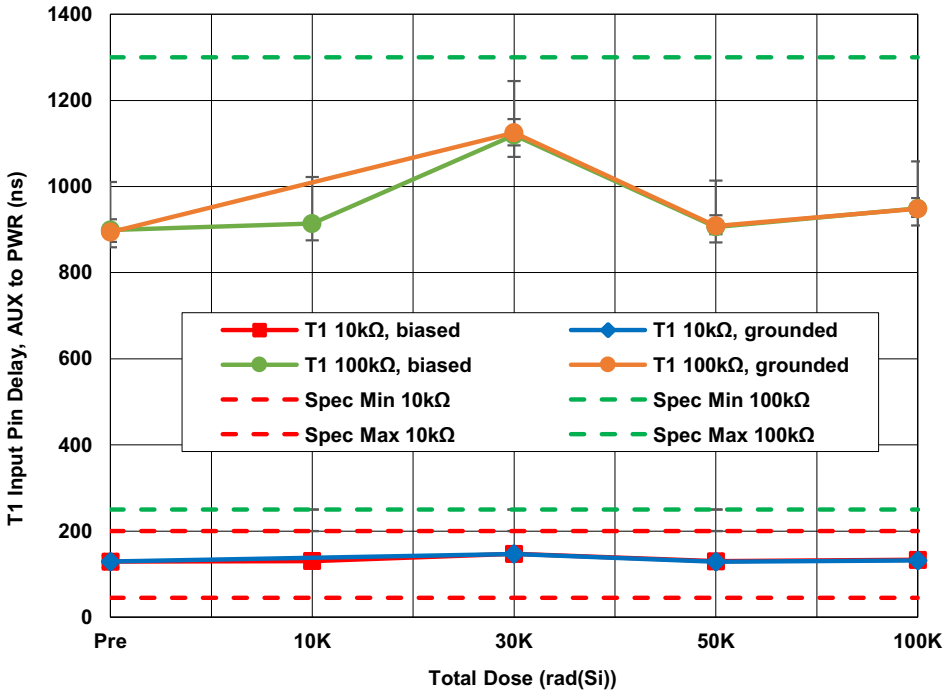

Figure 15. IS-1715AEH average T1 input pin delay, AUX to PWR (t_{T1}) with R_{T1} = 10kΩ and 100kΩ as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limits are 45ns minimum and 200ns maximum for R_{T1} = 10kΩ and 250ns minimum and 1300ns maximum for R_{T1} = 100kΩ.

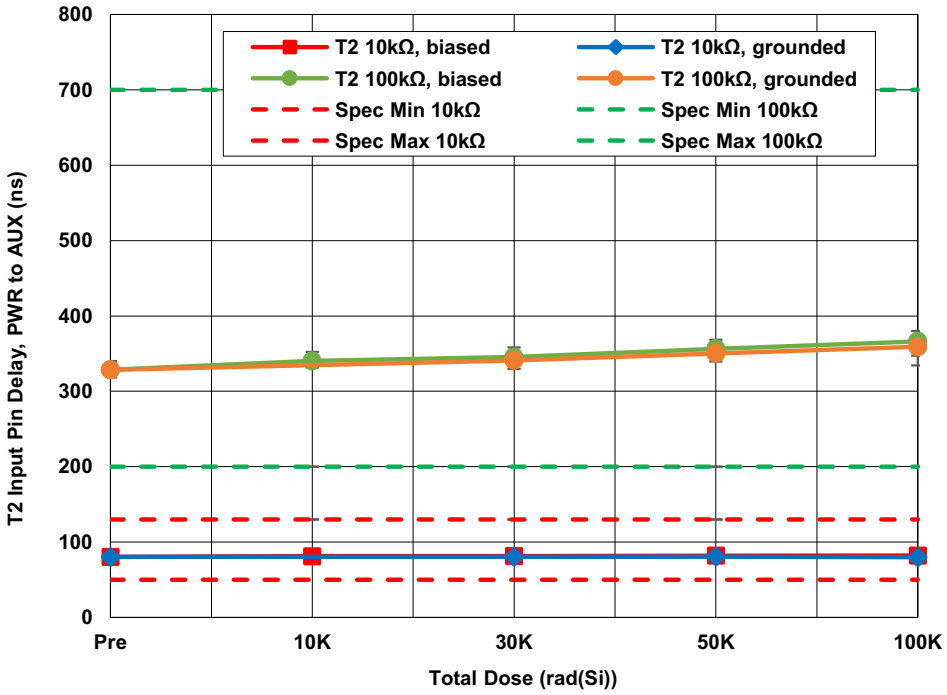

Figure 16. IS-1715AEH average T2 input pin delay, PWR to AUX (t_{T2}) with R_{T2} = 10kΩ and 100kΩ as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limits are 50ns minimum and 130ns maximum for R_{T2} = 10kΩ and 200ns minimum and 700ns maximum for R_{T2} = 100kΩ.

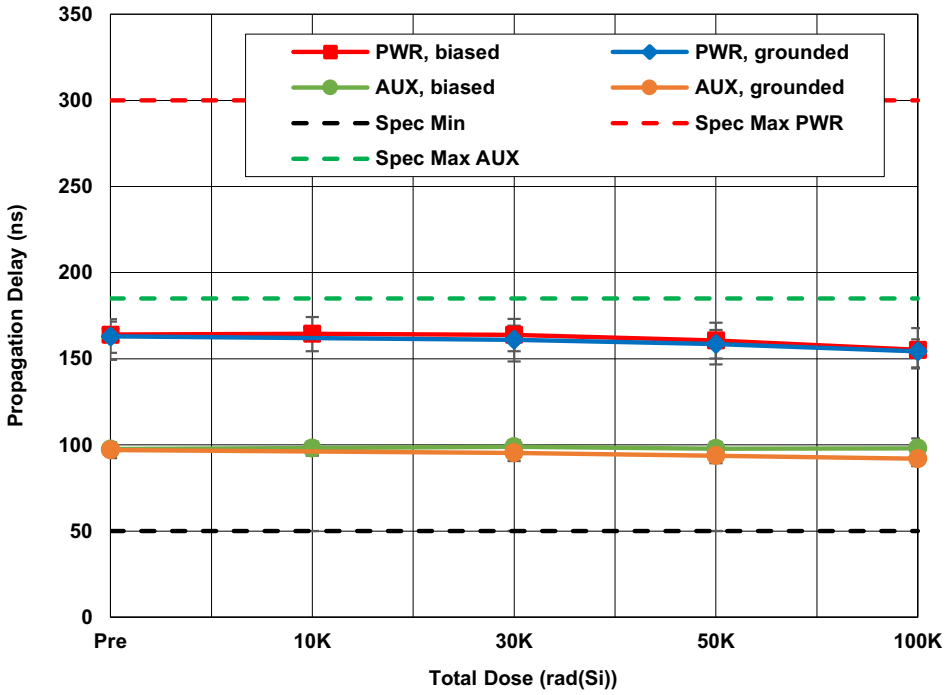

Figure 17. IS-1715AEH average propagation delay for PWR (T_{DP}) and AUX (T_{DA}), with INPUT falling/rising edges at 50% points, respectively, as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limits are 50ns minimum and 300ns maximum for PWR and 50ns minimum and 185ns maximum for AUX.

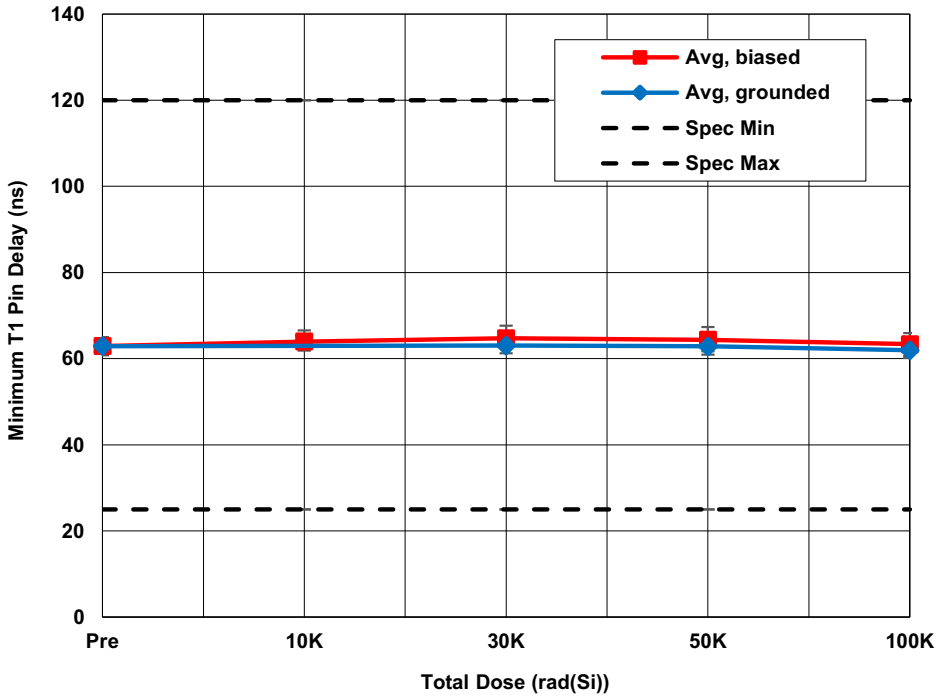

Figure 18. IS-1715AEH average minimum T1 pin delay (T_{1DM}) with T1 pin = 2.5V as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limits are 25ns minimum and 120ns maximum.

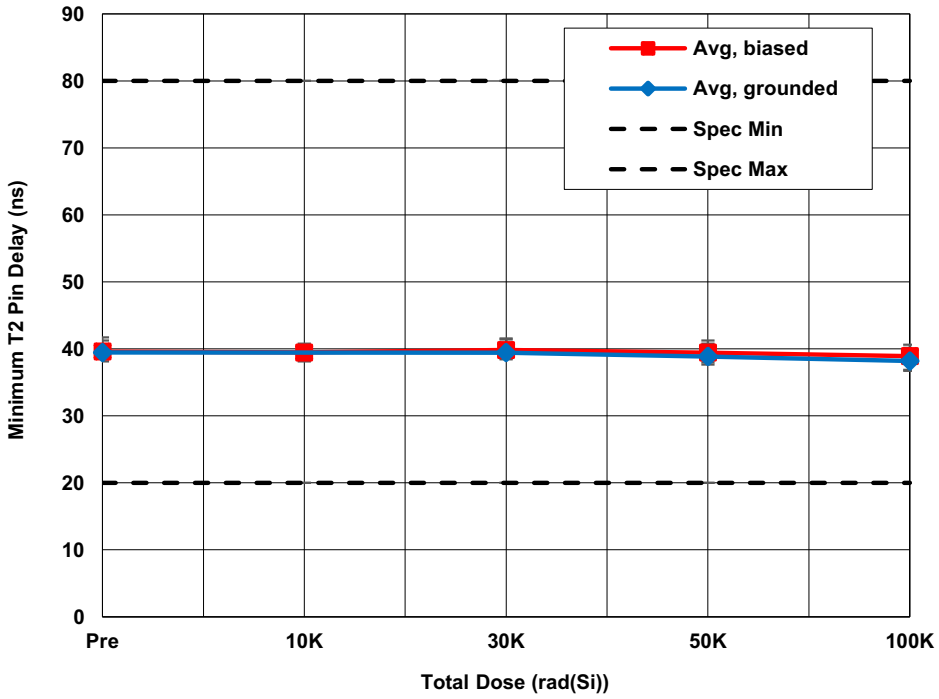

Figure 19. IS-1715AEH average minimum T2 pin delay (T_{2DM}) with T2 pin = 2.5V as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limits are 20ns minimum and 80ns maximum.

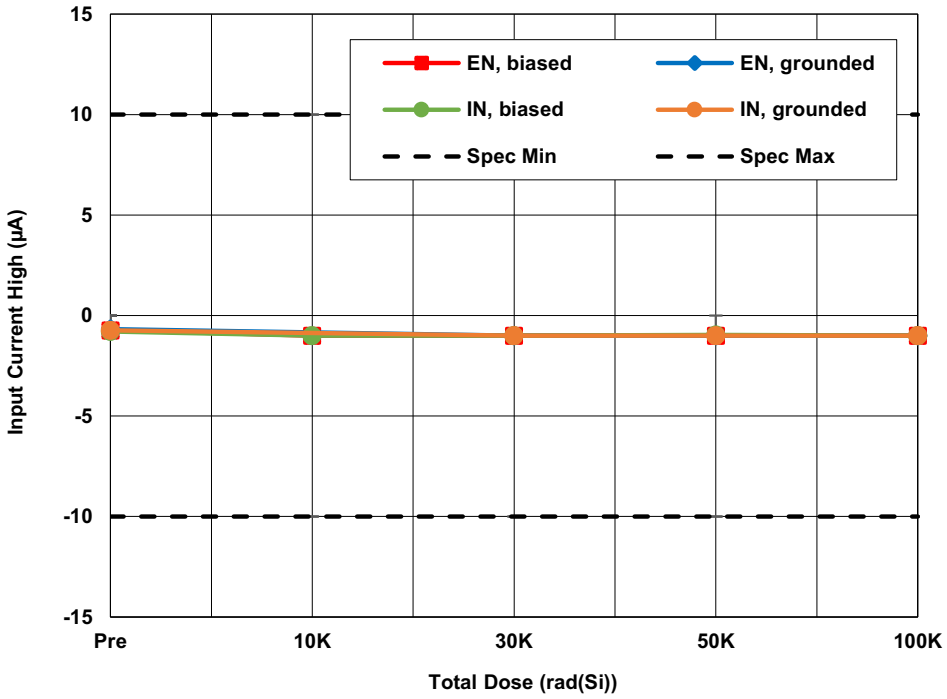

Figure 20. IS-1715AEH average input current high (I_{IH}) with of ENABLE and INPUT with ENABLE and INPUT = 15V as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limits are -10µA minimum and 10µA maximum.

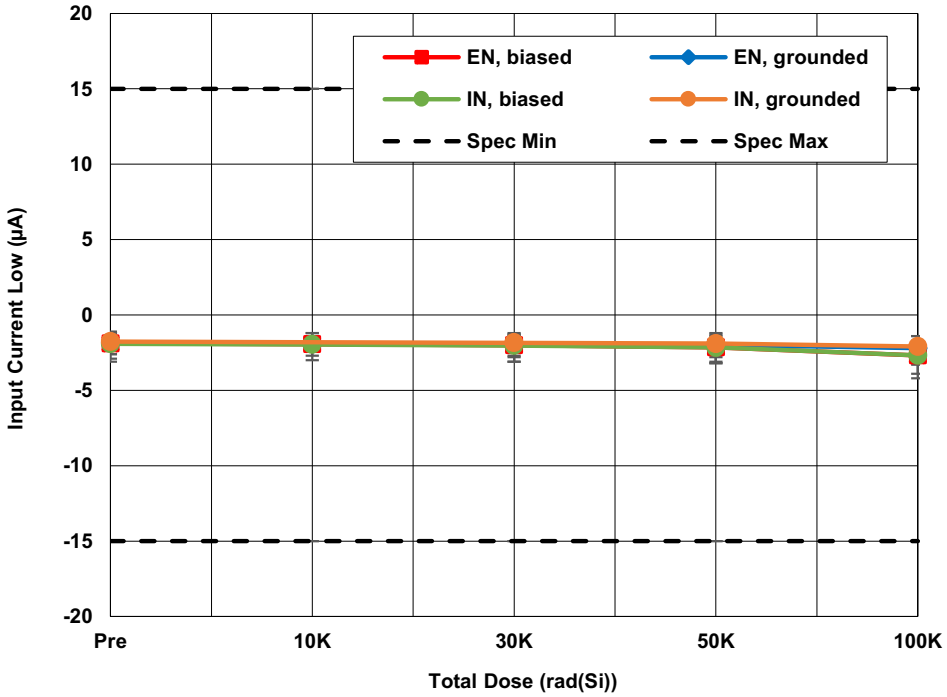

Figure 21. IS-1715AEH average input current low (I_{IL}) of ENABLE and INPUT with ENABLE and INPUT = 0V as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The SMD limits are -15µA minimum and 15µA maximum.

3. Discussion and Conclusion

The results of the LDR total dose test of the IS-1715AEH radiation hardened complementary switch FET driver have been reported. The irradiation of biased and grounded samples to 100krad(Si). All SMD parameters passed at all downpoints, however, the 10krad(Si) results for the grounded samples were missing from the recorded data and were unable to be plotted. However, all parts passed the 30krad(Si) downpoint. No evidence of bias dependence was observed.

Appendix

Reported Parameters

Table 3 lists the key parameters that are considered indicative of part performance. These parameters are plotted in Figure 4 through Figure 21. All limits are taken from the IS-1715AEH SMD (5962-00521).

Table 3. IS-1715AEH Key Total Dose Parameters (T_A = 25°C)

Figure	Parameter	Symbol	Conditions	Low Limit	High Limit	Unit
4	Input Current, Nominal	I_{CC}	V_{CC} = 18V and ENBL = 3V	1	6	mA
5	Input Current, Sleep Mode	I_{CCS}	V_{CC} = 18V and ENBL = 0.8V	300	900	µA
6	Undervoltage, Rising Threshold	UV+		8.5	9.5	V
7	Undervoltage, Falling Threshold	UV-		7.7	8.8	V
8	Undervoltage, Delta	UVD		0	2	V
9	Pre Turn-On Voltage, PWR Output, Low	V_{PPWR}	V_{CC} = 0V, ENBL = 0.8V, I_{OUT} = 10mA	-	2	V
10	PWR Pin Output Low, Saturation	V_{PWR}	INPUT = 0.8V, I_{OUT} = 40mA	-	1	V
11			INPUT = 0.8V, I_{OUT} = 100mA	-	1.5	
12	PWR Pin Output High, Saturation	V_{CC} - V_{PWR}	INPUT = 3.0V, I_{OUT} = -40mA	-	1	V
13			INPUT = 3.0V, I_{OUT} = -100mA	1	1.5	
14	Output Rise Time	T_{RP}	V_{CC} = 10V and C_L = 2200pF	15	50	ns
	Output Fall Time	T_{RF}				
15	T1 Input Pin Delay, AUX to PWR	t_{T1}	R_{T1} = 10kΩ	45	200	ns
			R_{T1} = 100kΩ	250	1300	
16	T2 Input Pin Delay, PWR to AUX	t_{T2}	R_{T1} = 10kΩ	50	130	ns
			R_{T1} = 100kΩ	200	700	
17	Propagation Delay For PWR	T_{DP}	INPUT falling/rising edges at 50% points	50	300	ns
	Propagation Delay For AUX	T_{DA}		50	185	
18	Minimum T1 Pin Delay	t_{1DM}	T1 pin = 2.5V	25	120	ns
19	Minimum T2 Pin Delay	t_{2DM}	T2 pin = 2.5V	20	80	ns
20	Input Current High	I_{IH}	ENABLE and INPUT = 15V	-10	10	µA
21	Input Current Low	I_{IL}	ENABLE and INPUT = 0V	-15	15	µA

4. Revision History

Revision	Date	Description
1.0	Apr 6, 2021	Initial release

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