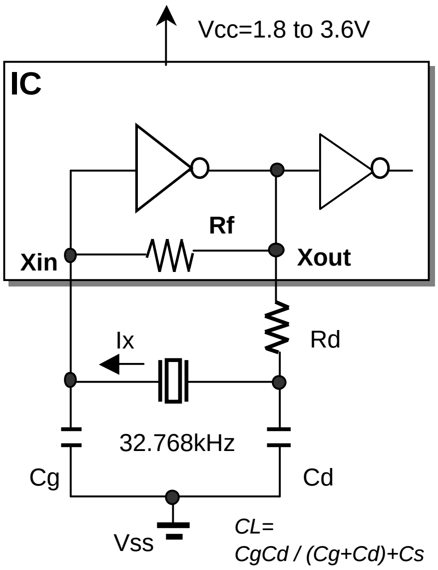
Evaluation of Subsystem Clock Oscillation Circuit

[HD64338024SWJB-80C] TQFP(12x12) 0.50mm pitch

Measurement conditions : 3.3V , 2.4V

Model	:VT-200
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10^{6}
Load capacitance	:CL=6.0pF
Equivalent series resistance	:R1=50kohm max
Max. Drive level	:DL=1x10^{6}W max
Recommended drive level	:DL=0.1x10^{6}W typ

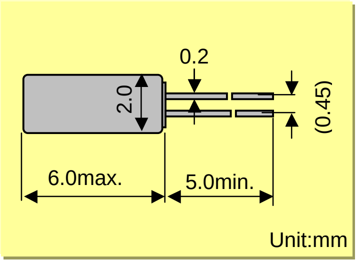


Remark) Ix : current through crystal

FEATURES

1.Compact tubular package
2.Photolithographic process
3.Excellent shock resistance and environmental characteristics.
4.Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



MODEL:VT-200 6.0pF with HD64338024S at 25°C

Key specifications	Vcc=2.4V	Vcc=3.3V	Remarks
Current control resistance : Rd (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	4	6	Optimal capacity in response to CL
Capacitance at drain : Cd (pF)	4	6	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vcc=2.4V	Vcc=3.3V	Remarks
Matching Accuracy : df / f (x10^{-6})	0.3	-1.2	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10^{-6})	6.1	6.4	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (x10^{-6}W)	0.02	0.02	DL=Ix^{2} Re < 1x10^{-6}W,Re=R1(1 + Co / CL)^{2}
Negative resistance : | - RL | (kohm)	717	717	5 times larger than R_{1MAX}
Oscillation allowance : M (times)	14.3	14.3	Judgemental standard of oscillation stability
Oscillation start up time : Ts (sec)	0.85	0.80	Time to reach 90% of output level

Temperature characteristics of circuit		Vcc=2.4V	Vcc=3.3V	Remarks
at -40°C	Variation : df / T (x10^{-6})	-139	-139	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^{2})
at +85°C	Variation : df / T (x10^{-6})	-134	-134	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^{2})

The mention value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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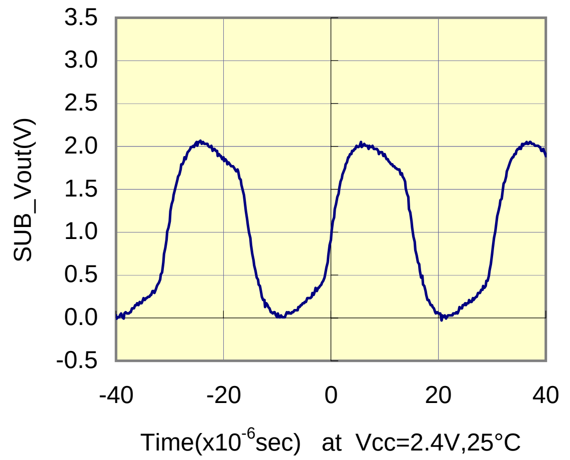
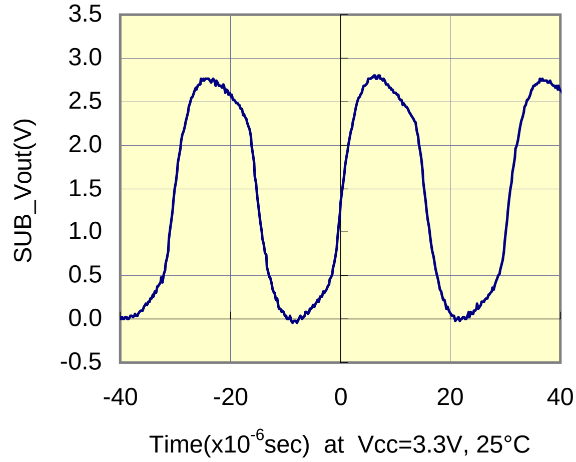
Measurement conditions : 3.3V , 2.4V

Test Data

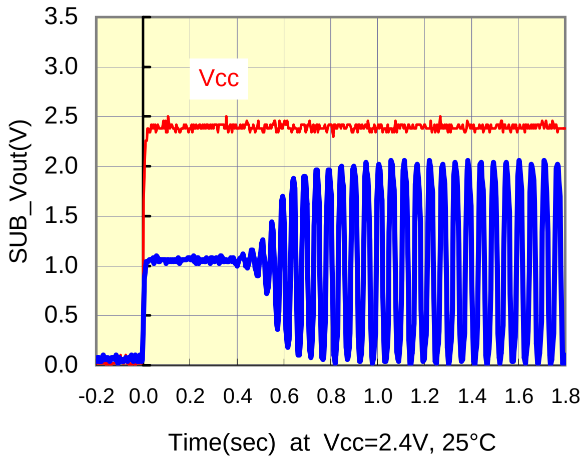
Output signal wave from the oscillator
MODEL : VT-200 6.0pF with HD64338024S



Output signal wave from the oscillator
MODEL : VT-200 6.0pF with HD64338024S



Start up time of SUB_Vout
MODEL : VT-200 6.0pF with HD64338024S



Start up time of SUB_Vout
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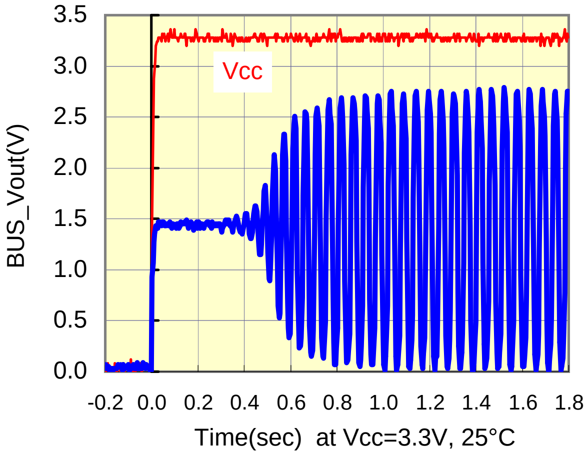
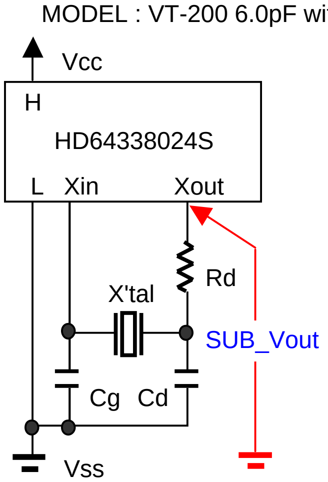


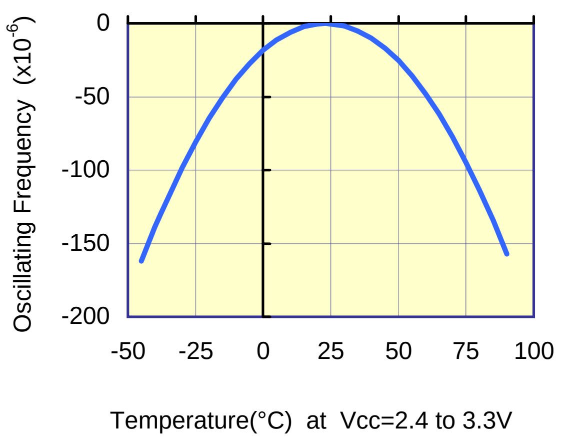
Test Circuit
MODEL : VT-200 6.0pF with HD64338024S



H : 1,52
L : 8,11,53
Xin : 6
Xout : 7

Recommended Values
X'tal :
VT-200 +/-20/6.0pF
Vcc=2.4V and 3.3V
Rd=0 ohm
Cg=4 to 6pF typ
Cd=4 to 6pF typ
Ta=-40 to 85°C

Temperature characteristics of oscillating frequency
MODEL : VT-200 6.0pF with HD64338024S



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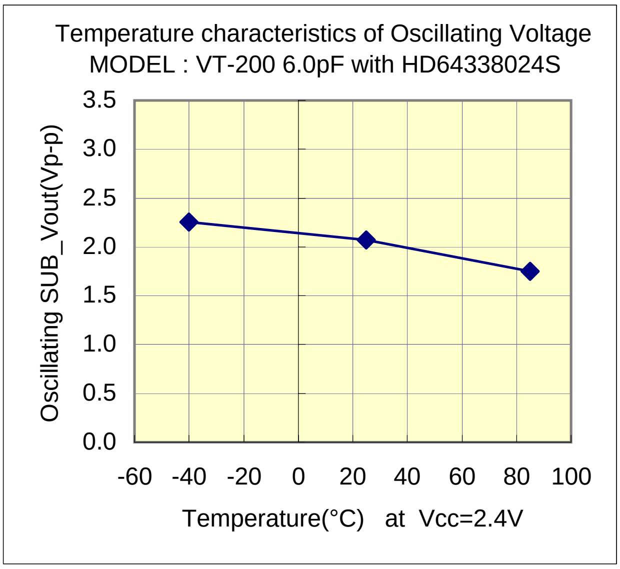
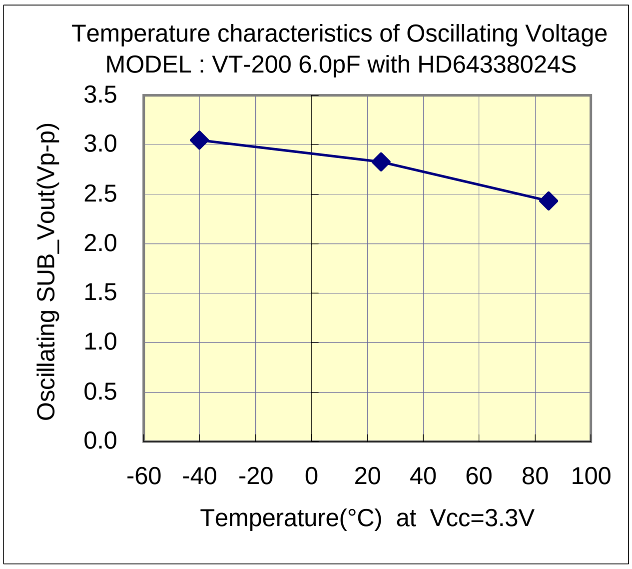
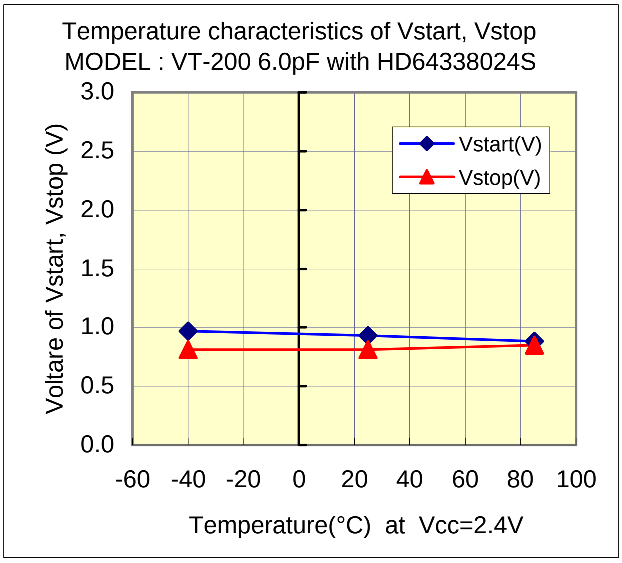
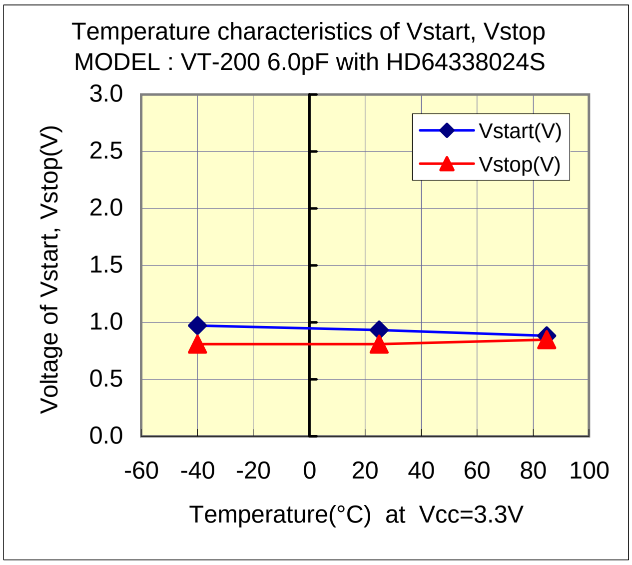
Measurement conditions : 3.3V , 2.4V

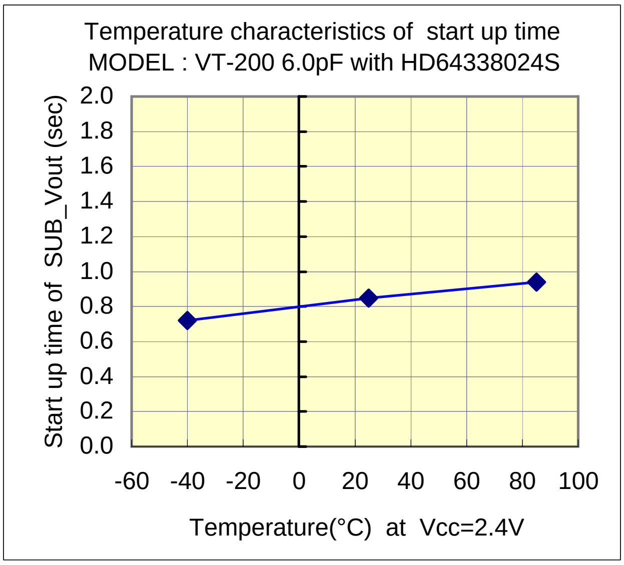
Test Data : Temperature characteristics

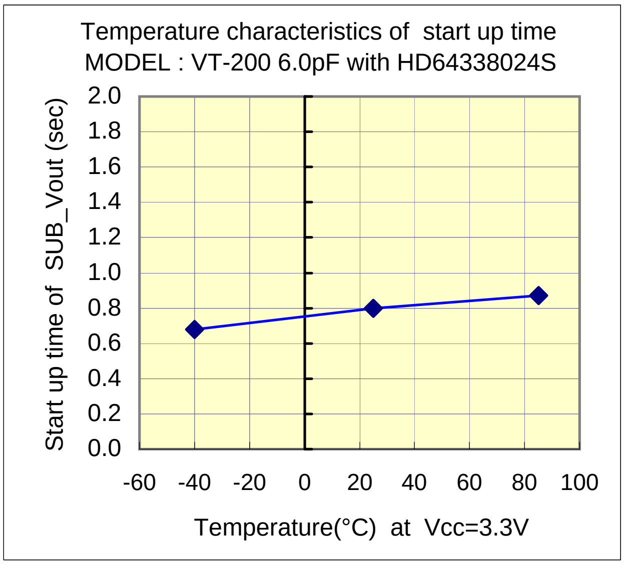












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Evaluation of Subsystem Clock Oscillation Circuit

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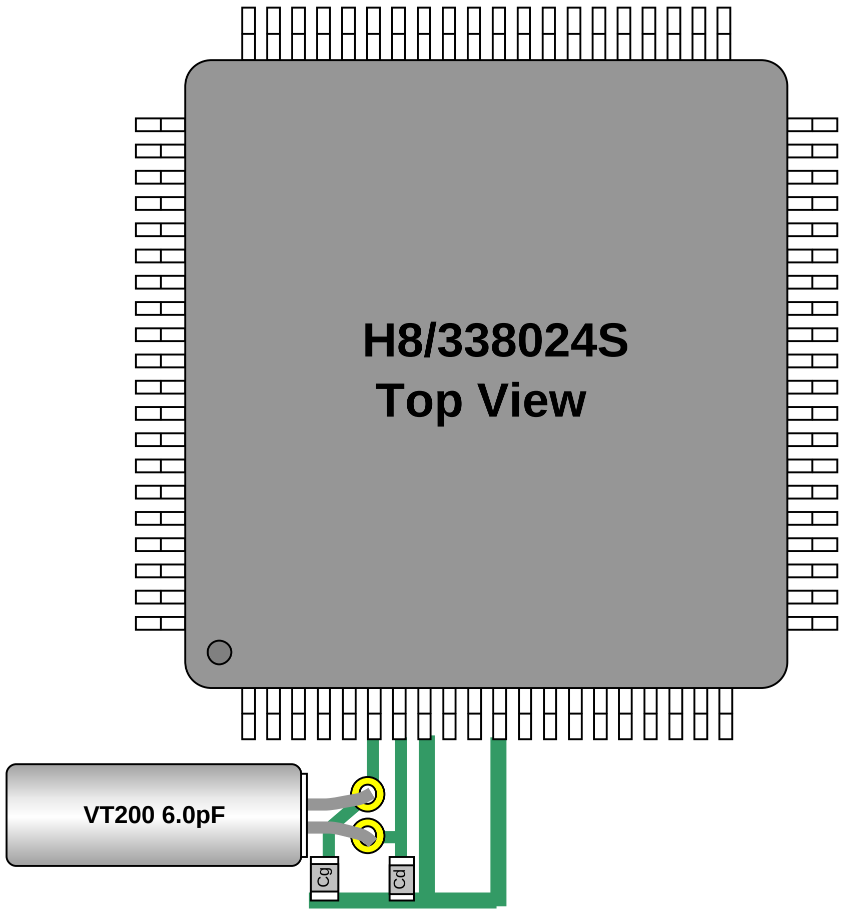
Measurement conditions : 3.3V , 2.4V

Referenicial components layout(see Figure 1)



Avcc:1 (H)
Vcc:52 (H)
AVss:8 (L)
Vss:53(L)
TEST:11(L)
X1:6 (SUB_in)
X2:7 (SUB_out)
RES:12

Figure 1 Referenicial components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.
Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

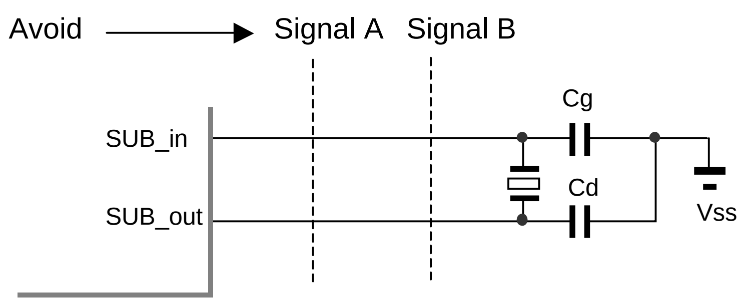


Figure 2 Example of Incorrect Board Design

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Measurement conditions : 3.3V , 2.4V

[Evaluation Sample : VT-200 6.0pF at 25°C]

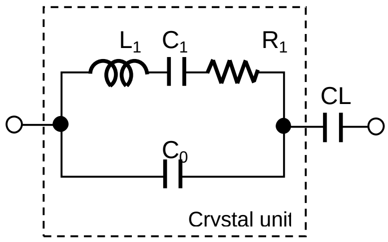
SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
VT-200 6.0pF	1	6	32768.18	32762.98	28.7	0.91	2.193	77.2
	2	6	32768.18	32763.04	27.8	0.89	2.161	80.9
	3	6	32768.19	32763.00	27.2	0.90	2.187	81.7

[IC Test Data : IC samples Rd=0 ohm,Cg=4 to 6pF,Cd=4 to 6pF at 25°C]

Vcc(V)	IC samples	Fosc(Hz)	df / f($x10^{-6}$)	DL($x10^{-6}$W)	| -RL |(kohm)	Vstart(V)	Ts(sec)
3.3	BE07620-01	32768.14	-1.23	0.02	717	0.93	0.80
	BE07620-02	32768.14	-1.23	0.02	717	0.93	0.81
	BE07620-03	32768.13	-1.41	0.02	717	0.92	0.80
2.4	BE07620-01	32768.14	0.30	0.02	717	0.89	0.85
	BE07620-02	32768.14	0.60	0.02	717	0.88	0.90
	BE07620-03	32768.13	0.30	0.02	717	0.92	0.87

Remak (see figure 3)

$$Fo = fr \times \{ C1 / (2 \times (Co + CL) + 1 \} \quad (Hz)$$



Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

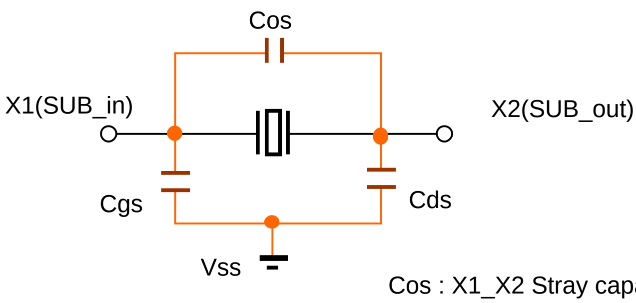
Figure 3 Equivalent circuit of crystal unit, and CL

Remak (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$CL = Cg \times Cd / (Cg + Cd) + Cs \quad (pF)$$

Where Cs Stands for stray capacity of the circuit.



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

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