

8A34001/02/03/04/05 (ClockMatrix™)

ITU-T G.8262 and G.8262.1 Compliance

Overview

This report describes the results for the compliance testing of Renesas' ClockMatrix™ PLL as per the standard ITU-T G.8262 and G.8262.1 for wander generation, wander transfer, phase transient tolerance, phase transient due to synchronization rearrangement operations, and holdover.

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1. Description of Tests and Setup

The synchronization rearrangement of the network is introduced through automatic reference switching between two clock inputs or through disconnecting the qualified reference clock input. Calnex Paragon-X is used to introduce and measure wander to and from the system while an Agilent frequency generator introduces phase transients. The measurement of phase transients is handled by a Keysight frequency counter.

The test setup is illustrated in the following diagram.

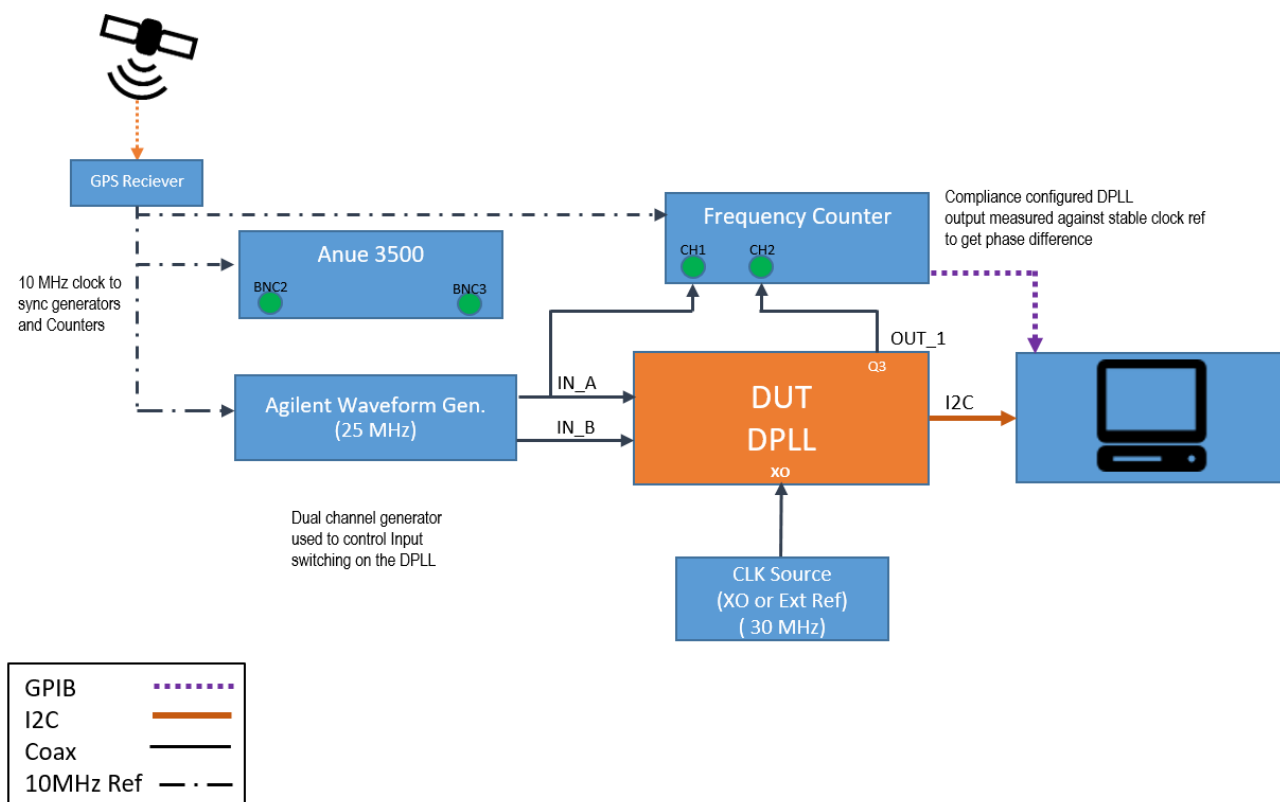


Figure 1. Complete Test Setup

The Symmetricom TimeProvider acts as a stable and accurate clock source locked to GPS. Its 10MHz clock output serves as the 10MHz reference clock for the Agilent 33250A function generator, 53230A frequency counter, and Paragon-X. The DUT will lock to the reference clock input generated either through 33250A Function Generator or Paragon-X. The Renesas PLL can lock to virtually any frequency from 1MHz to 1GHz and produce virtually any output frequency from 1MHz to 1GHz. The Renesas PLL supports digital Low-pass filter whose bandwidth and Phase slope limit is set based on the standard ITU-T G.8262 Opt1/Opt2 or ITU-T G.8262.1 to test their compliances. Fractional Frequency Offset (FFO) and Maximum Time Interval Error (MTIE) plots are calculated from the measurements taken from 53230A frequency counter. The objective maximum FFO and the MTIE plots throughout each test have the mask specified in the standard.

2. PLL Settings Information

Table 1. PLL Settings based on Compliance Standard Table

Compliance Standard No.	Input/Output Frequency (MHz)	PLL Bandwidth (Hz)	Phase Slope Limit (us/s)	Max Phase Lock Error (ns)	Phase Monitor Duration (s)	Gain Peaking Control
ITU-T G.8262 Option 1	25.00	1.2/3.0/10.0	7.500	250	10	< 0.2 dB
ITU-T G.8262 Option 2	25.00	0.1	0.885	250	10	< 0.2 dB
ITU-T G.8262.1 eEEEC	25.00	1.2/3.0	7.500	250	10	< 0.2 dB

3. Frequency Accuracy

Frequency accuracy at free-run is determined by the system oscillator used. For more information, see [AN-807 Recommended Crystal Oscillator for Network Synchronization](#).

3.1 Option 1

Refer to section G.813 Option 1 / G.8262 Option 1 (see Table 8 in [AN-807](#)).

3.2 Option 2

Refer to section GR-1244-CORE and GR-253-CORE Stratum 3 / G.812 Type IV / G.8262 Option 2 (see Table 7 in [AN-807](#)).

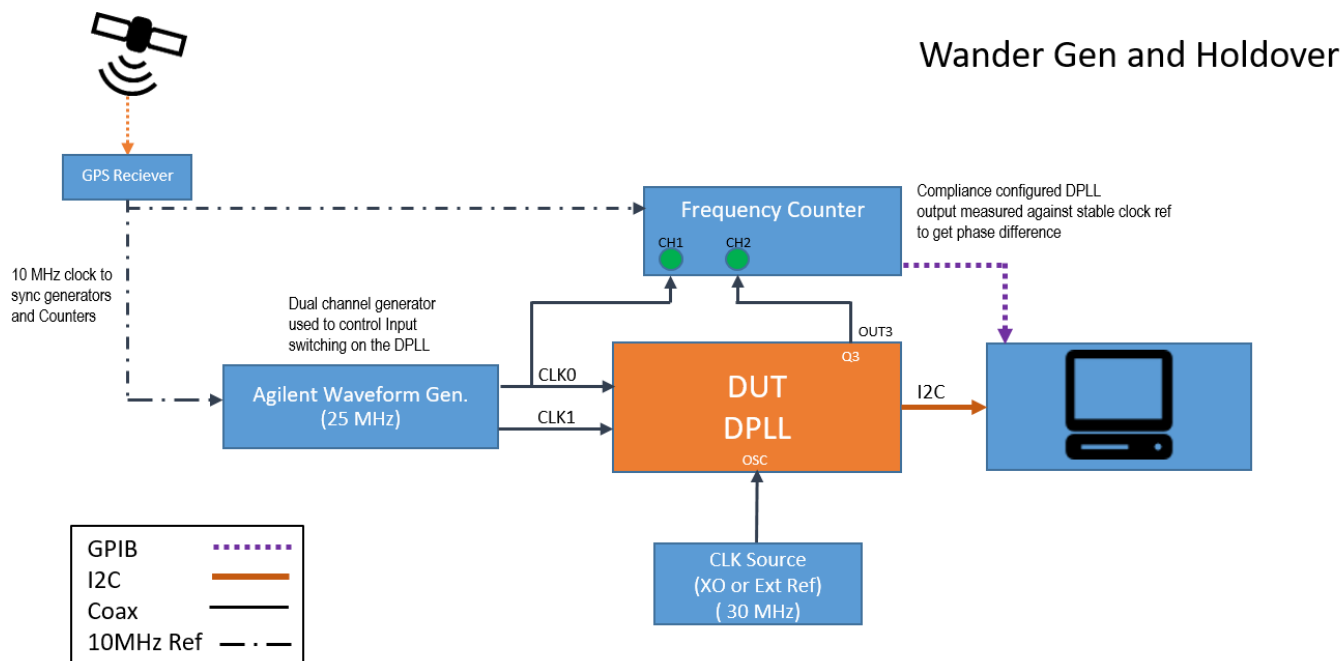
3.3 Enhanced or for Both Options 1/2

Refer to section G.8262.1 Enhanced Synchronous Ethernet/OTN Equipment Clock (see Table 6 in [AN-807](#)).

4. Pull-in, Hold-in, and Pull-out Ranges

The ClockMatrix™ PLL supports a pull-range of ± 244 ppm. Per-input activity monitors can be used to define a pull-in/hold-in range with ppb accuracy. Thus, to support a ± 4.6 ppm pull-in/hold-in with a standard 4.6ppm XO, you can set the frequency monitor to 9.2ppm (A), 12PPM (R).

5. Noise (Wander) Generation and Holdover Performance



The wander generation requirement checks for the noise generated by the DUT, while the PLL is locked to an input clock signal that is wander free, it should not generate any wander that exceeds the MTIE mask as given by the standard being tested.

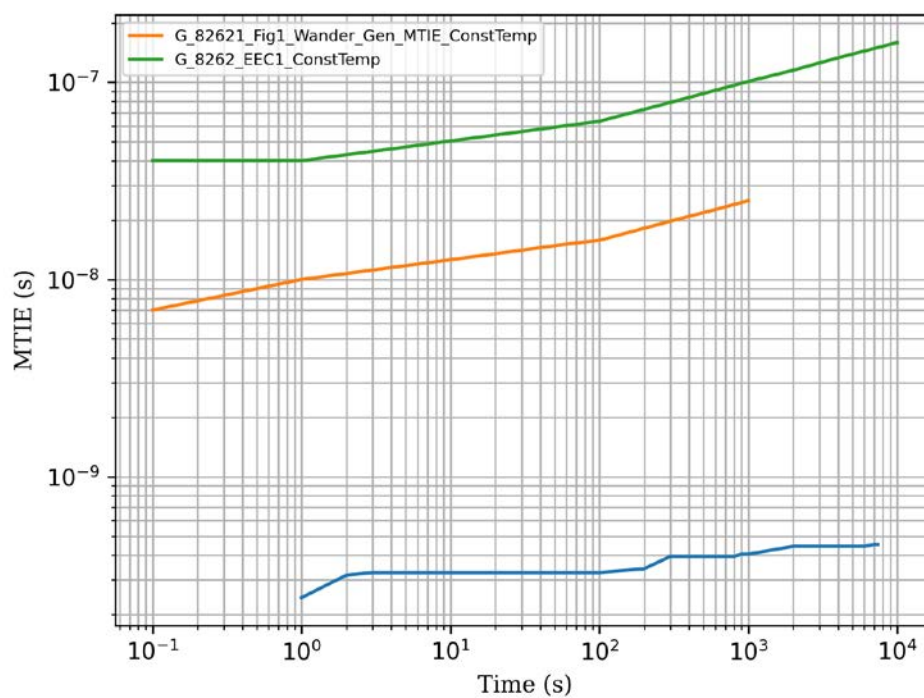
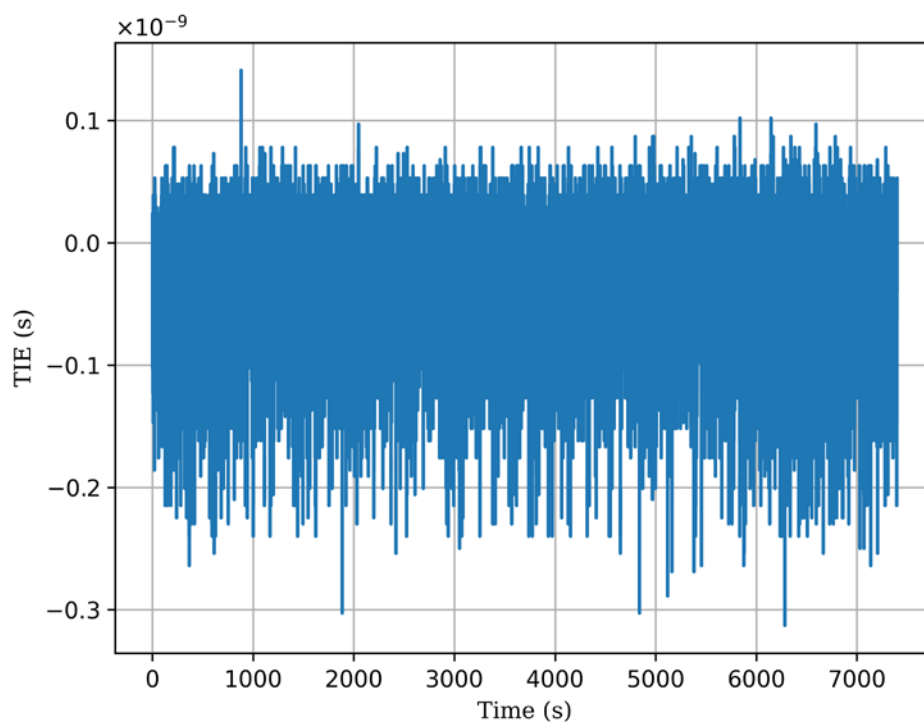
The wander generation and holdover test is carried out by providing a reference clock from the Agilent waveform generator on CLK0. The PLL should not produce/add any wander to the output beyond the standard allowed value. The test is run for 3 hours with a stable no wander input, and the output from OUT_3 is monitored for phase error on the frequency counter. The generator connected to CLK0 is then turned OFF for a duration of time and the PLL goes into holdover state once the input is removed. The phase error between the output OUT_3 and a second signal (reference signal from same source) is measured on the counter. The TIE and MTIE plots show the response of DUT in these conditions.

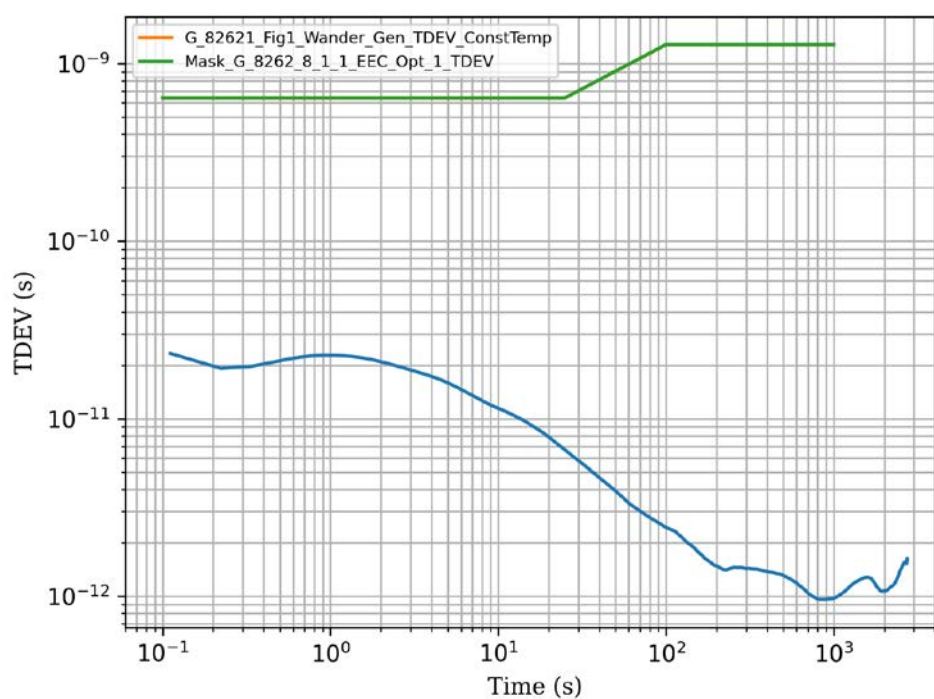
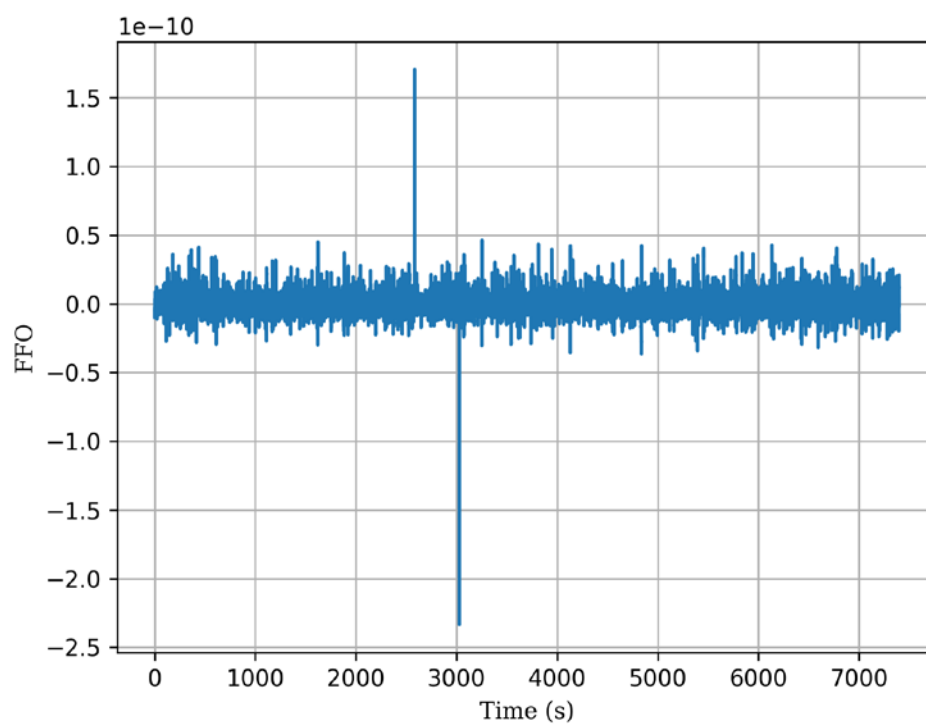
The holdover portion of this test is carried out with "Advanced Holdover".

Advanced holdover bandwidth is set to 1.5mHz.

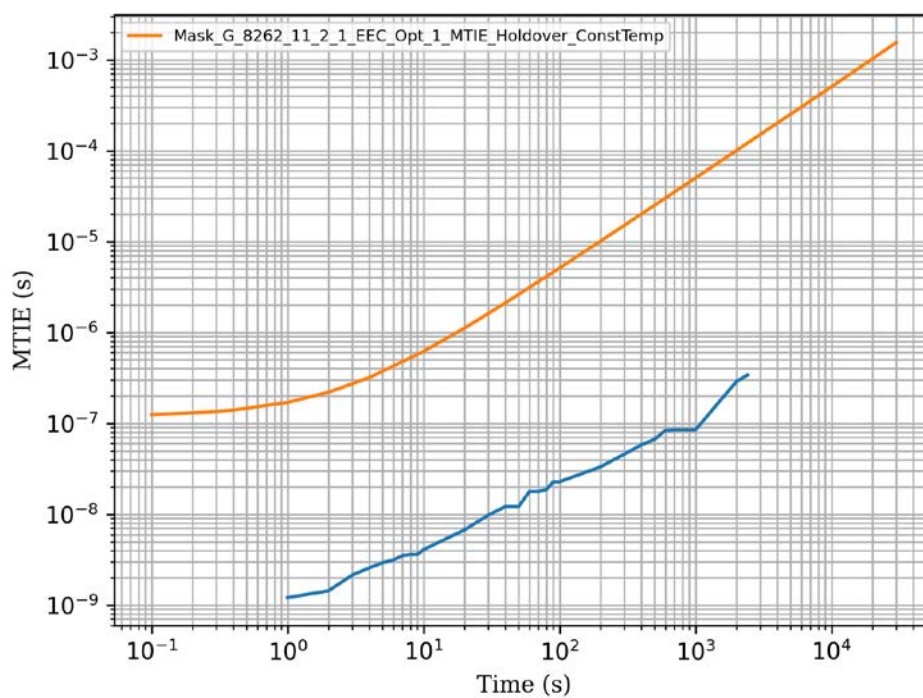
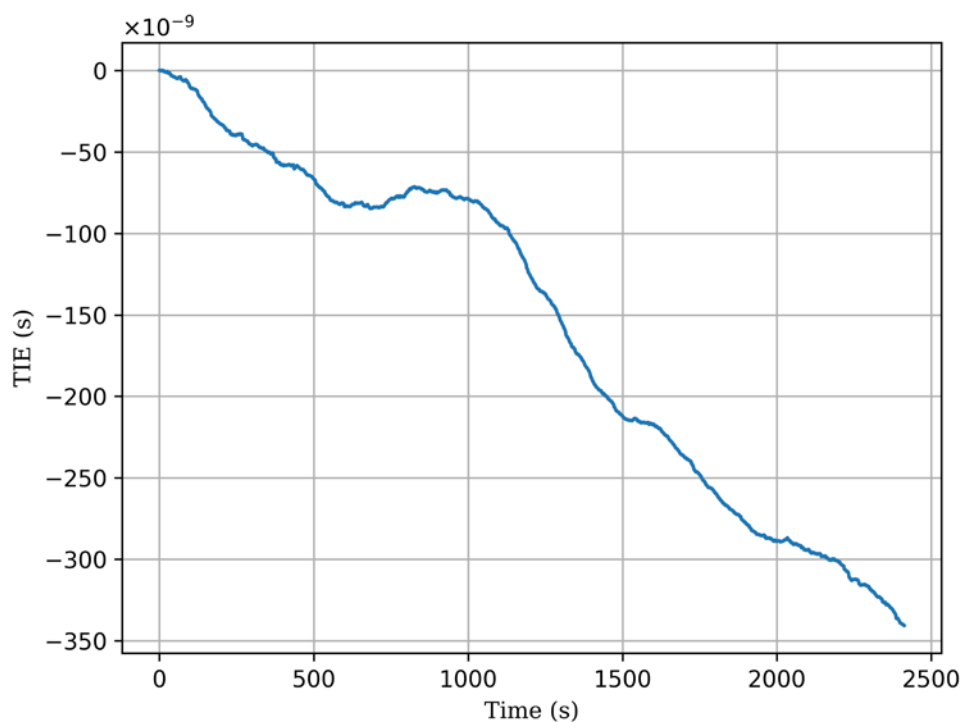
Advanced holdover history is set to 30 seconds.

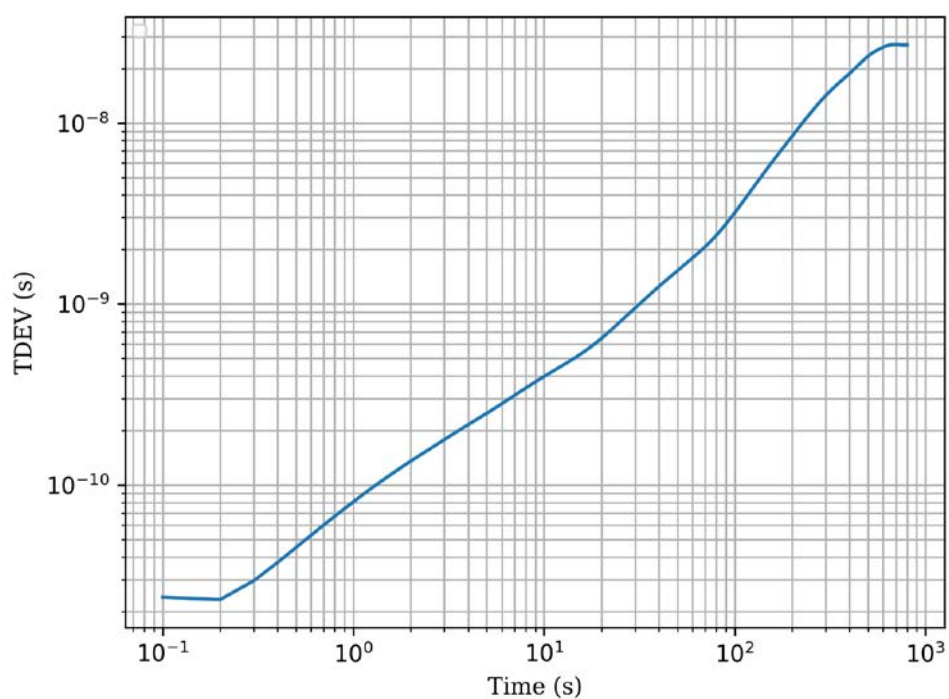
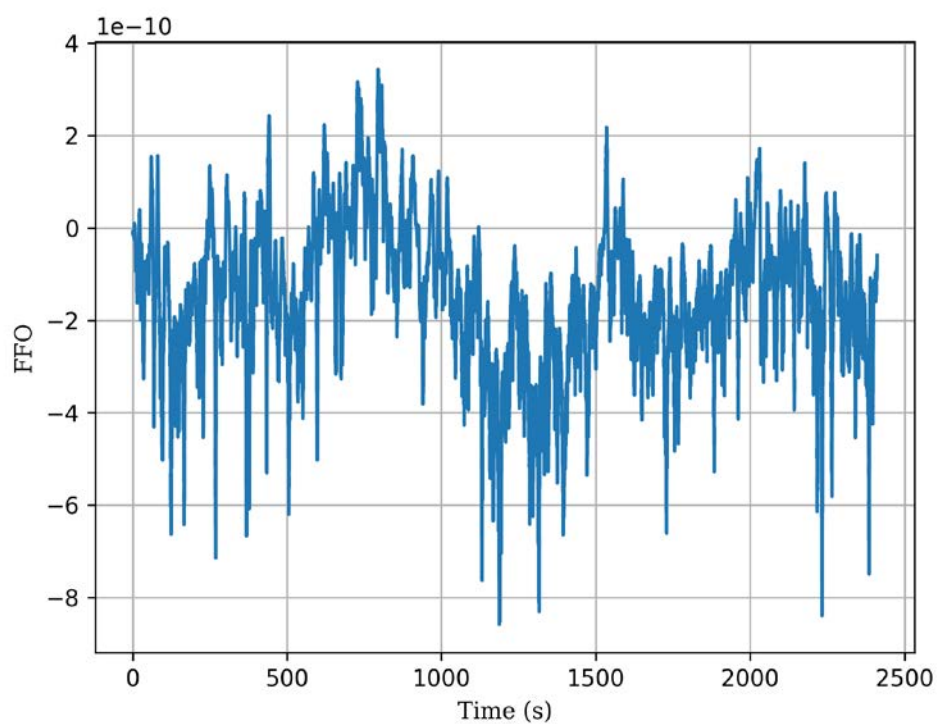
5.1 Wander in Locked Mode – G8262_EEC1_1Hz



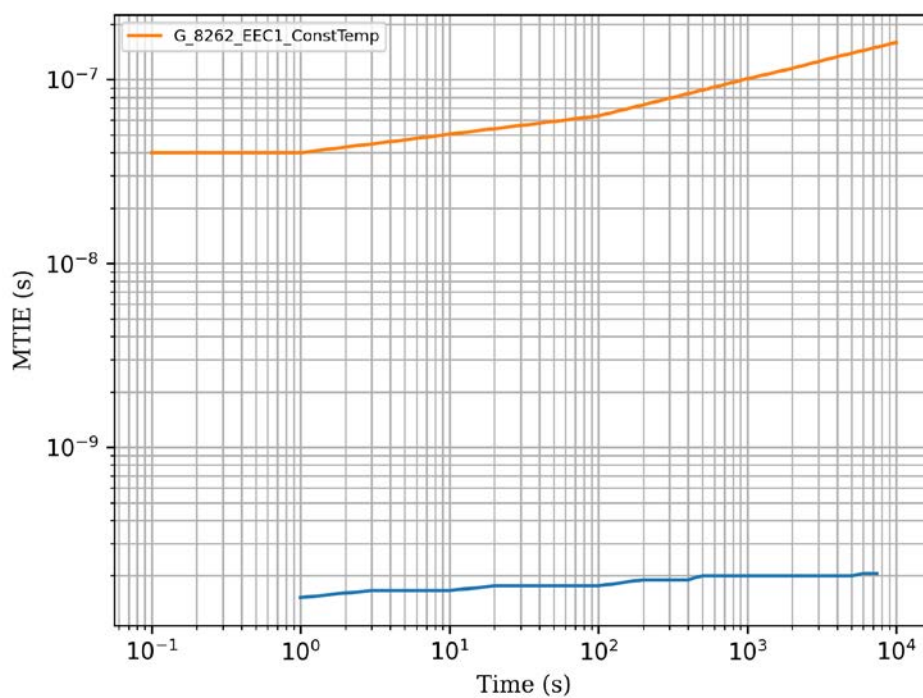
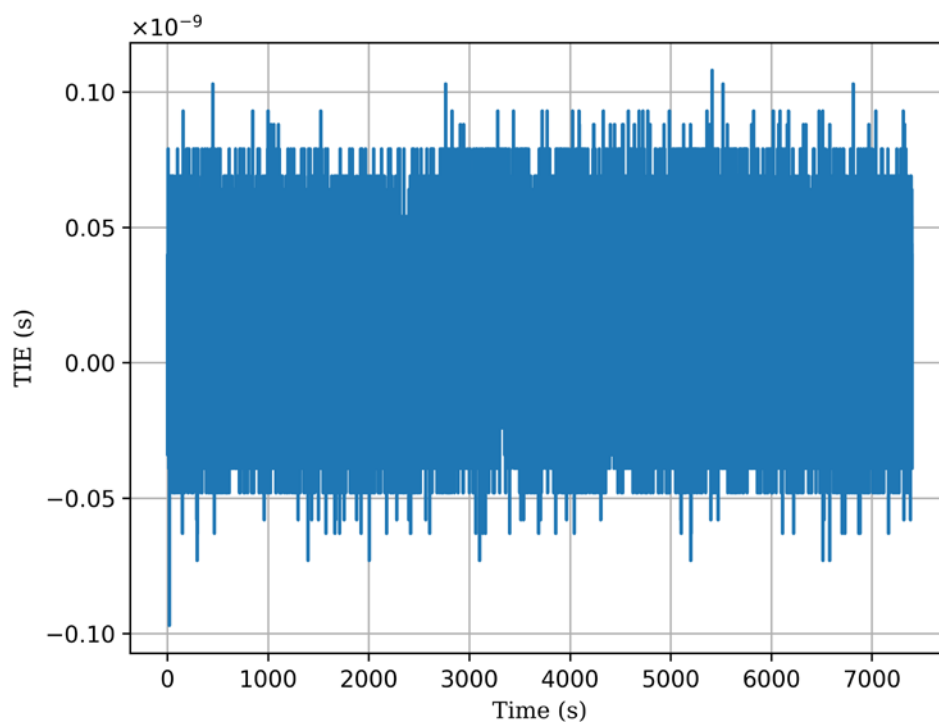


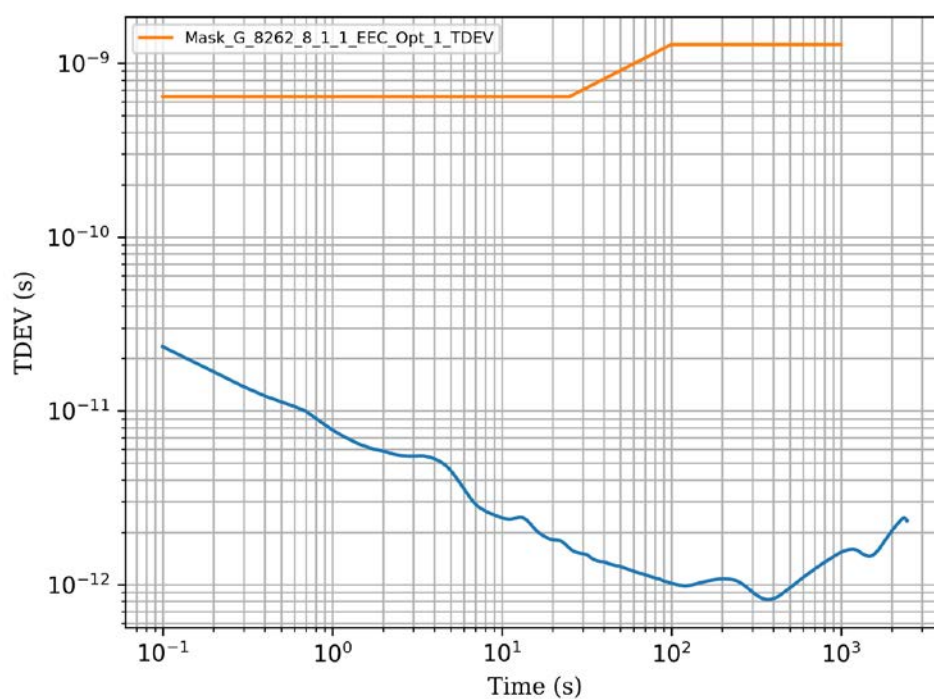
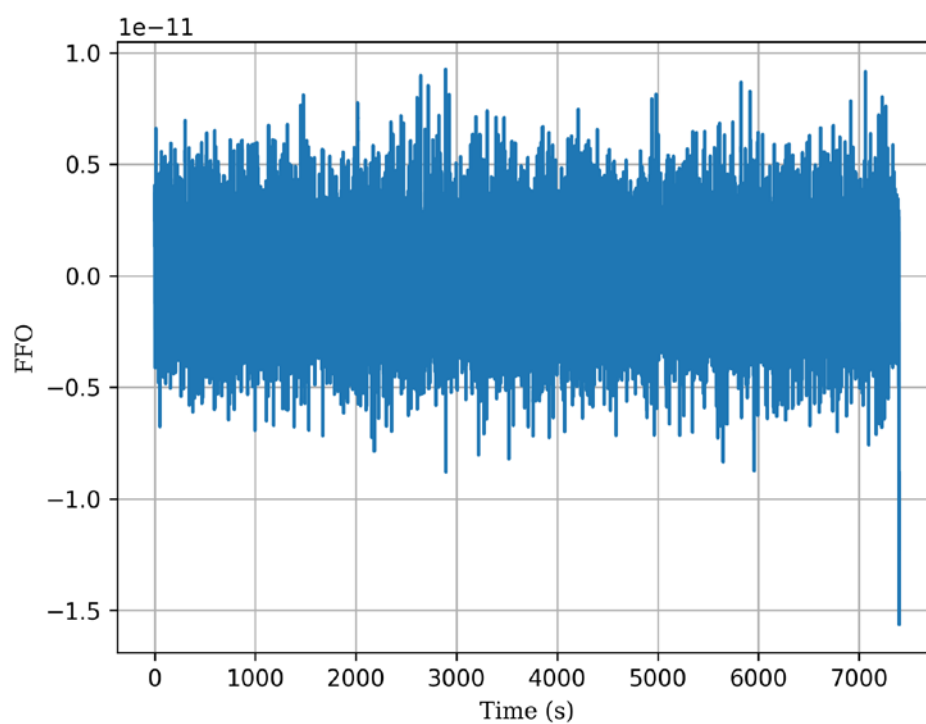
5.2 Long-term Phase Transient Response – G8262_EEC1_1Hz



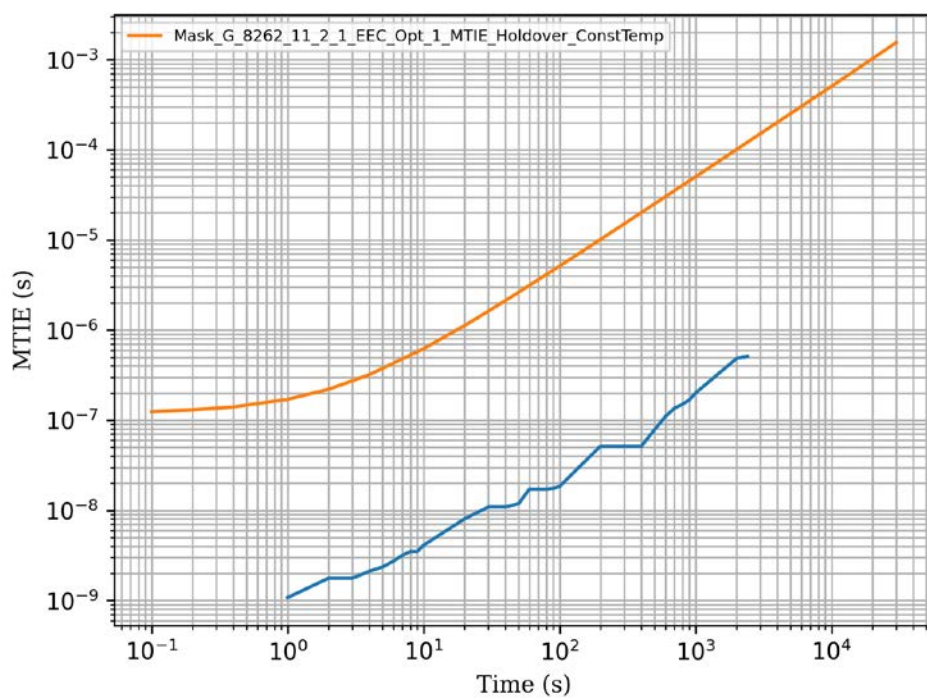
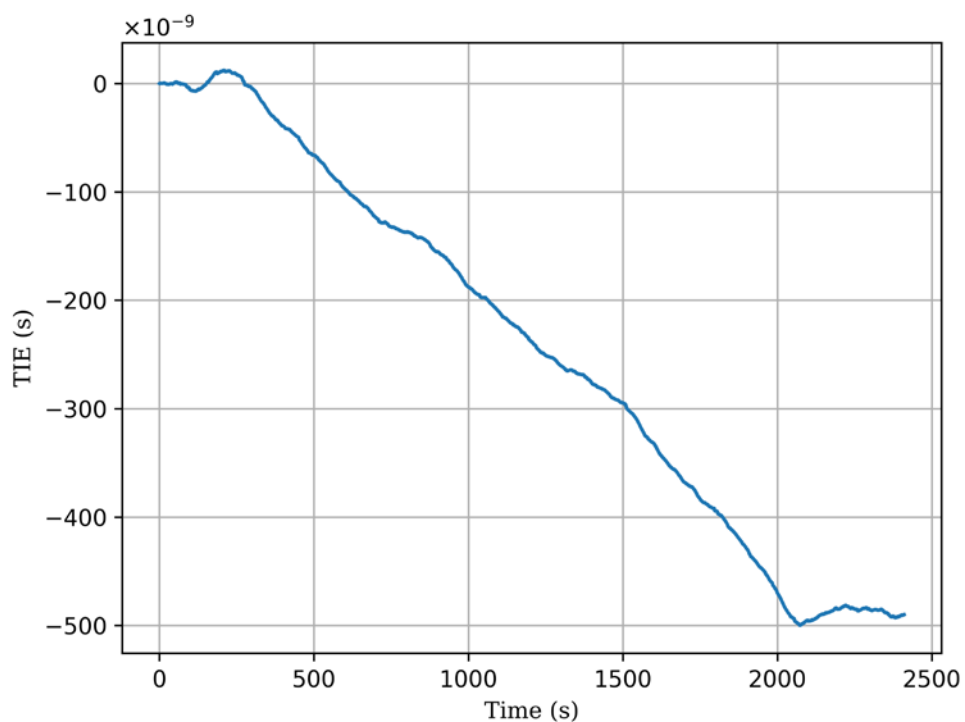


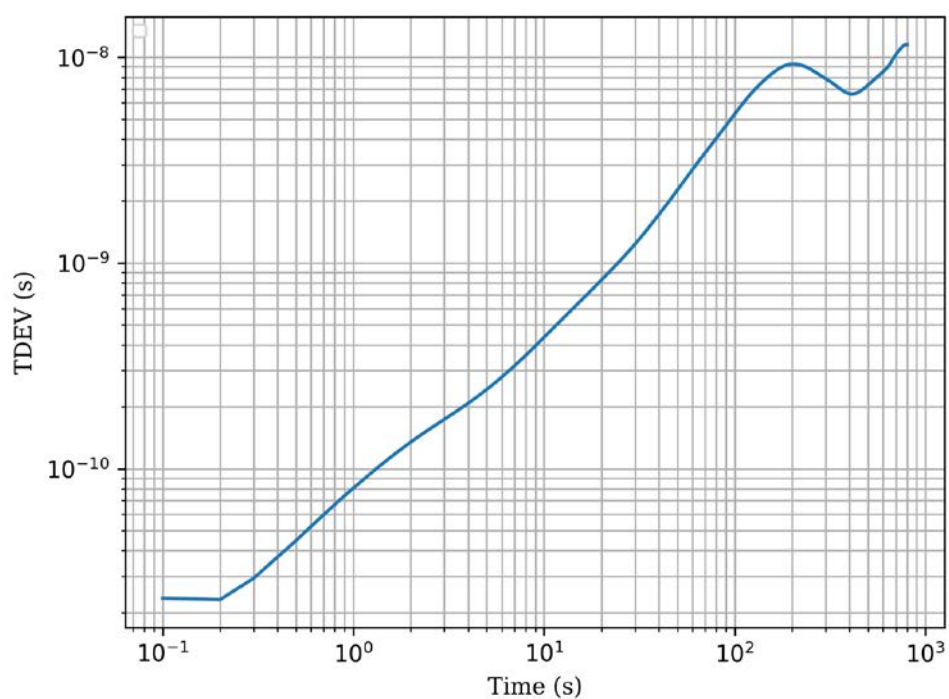
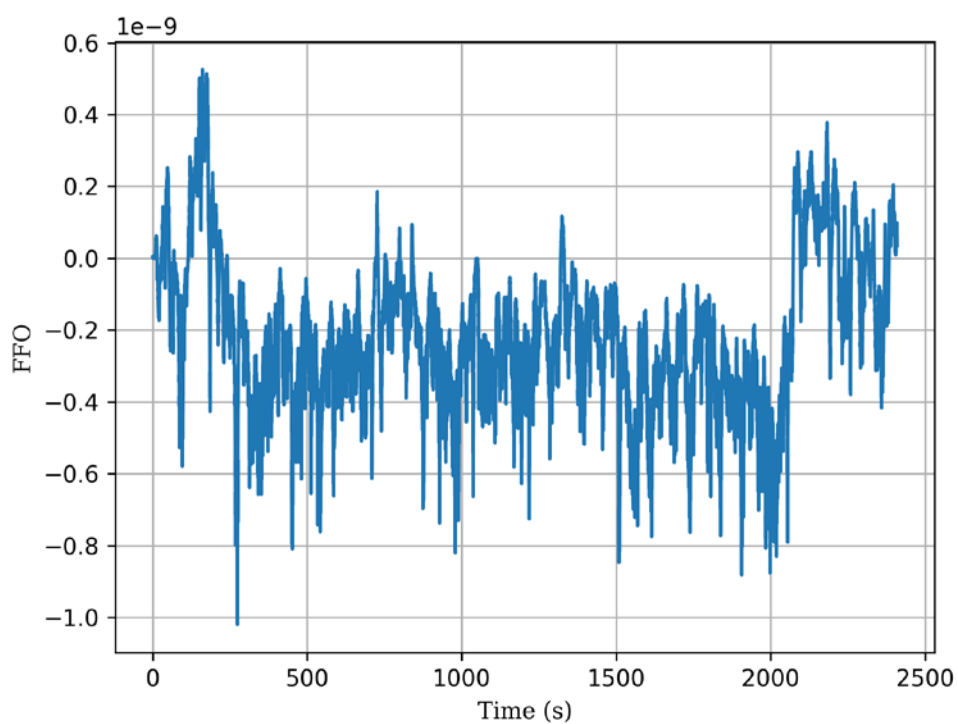
5.3 Wander in Locked Mode – G8262_EEC1_10Hz



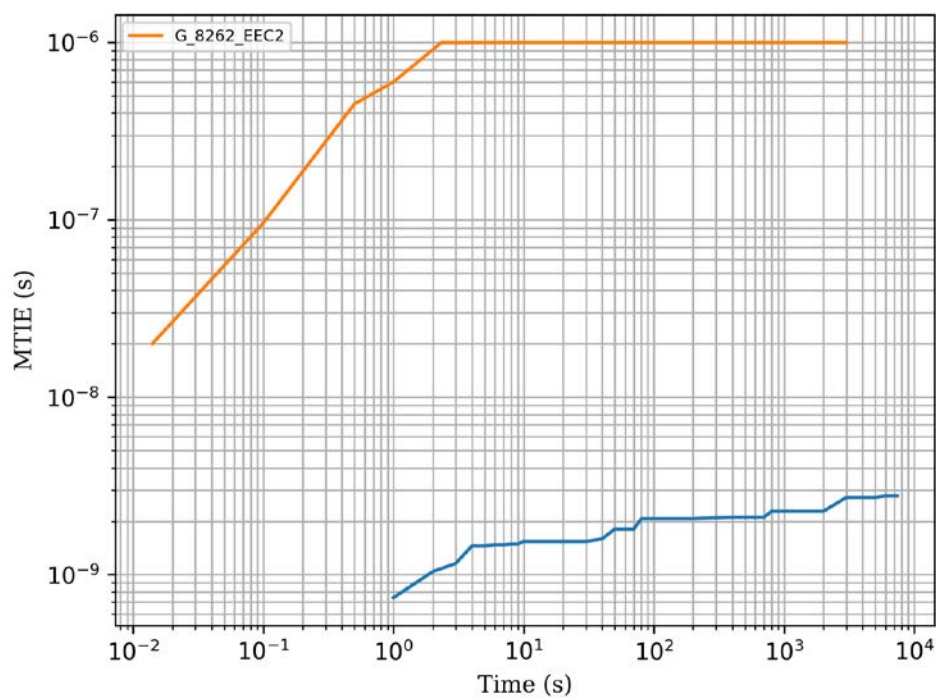
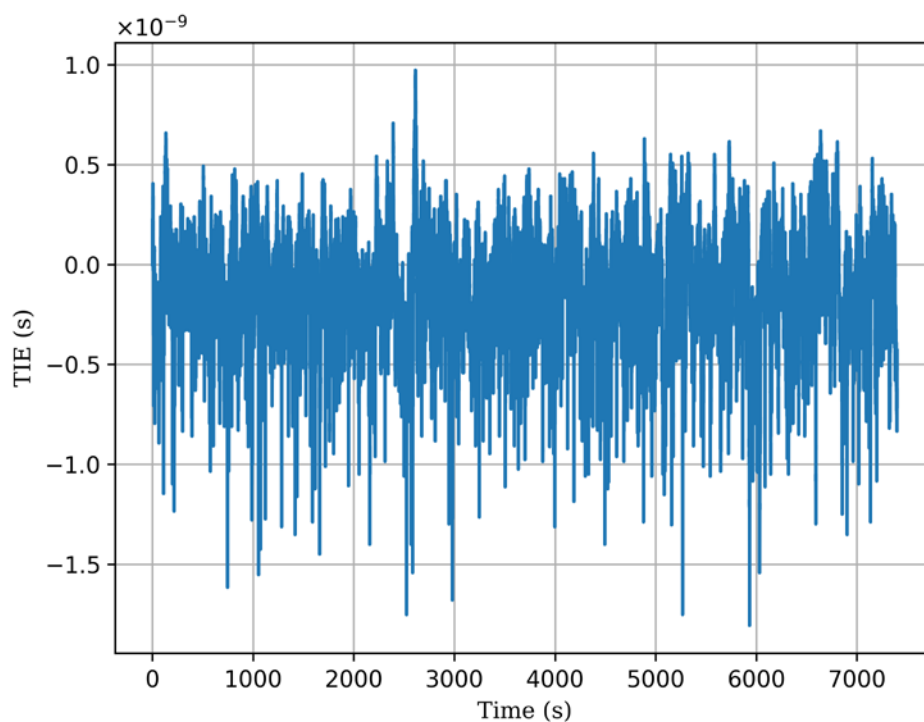


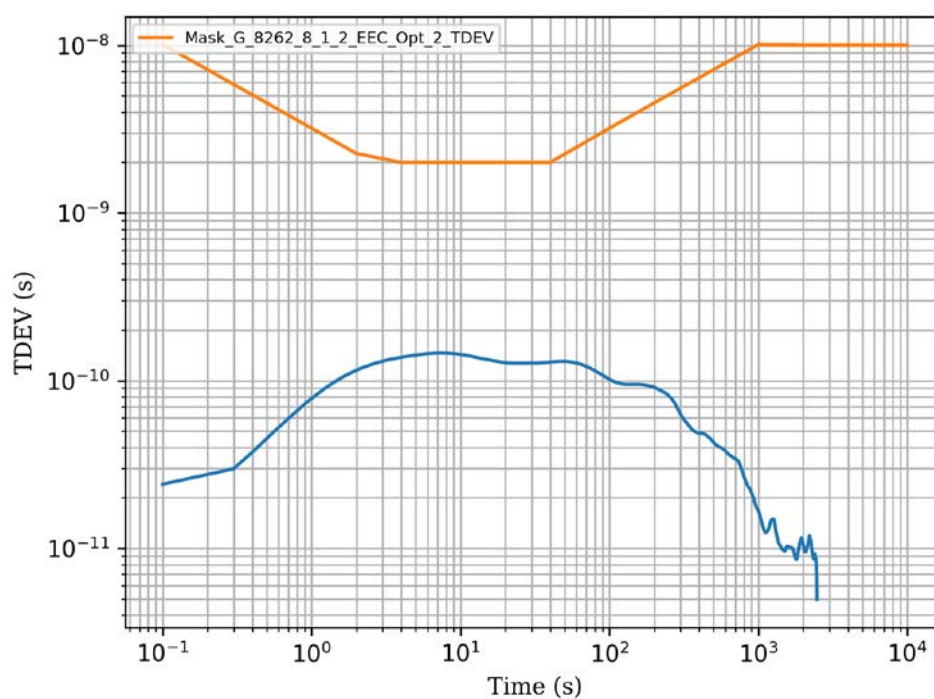
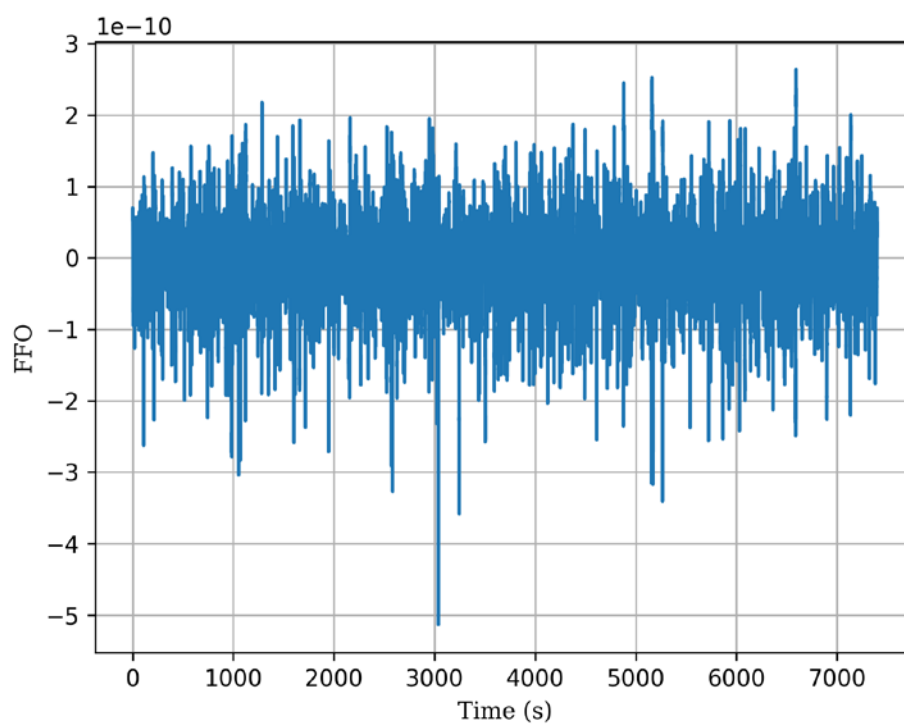
5.4 Long-term Phase Transient Response – G8262_EEC1_10Hz



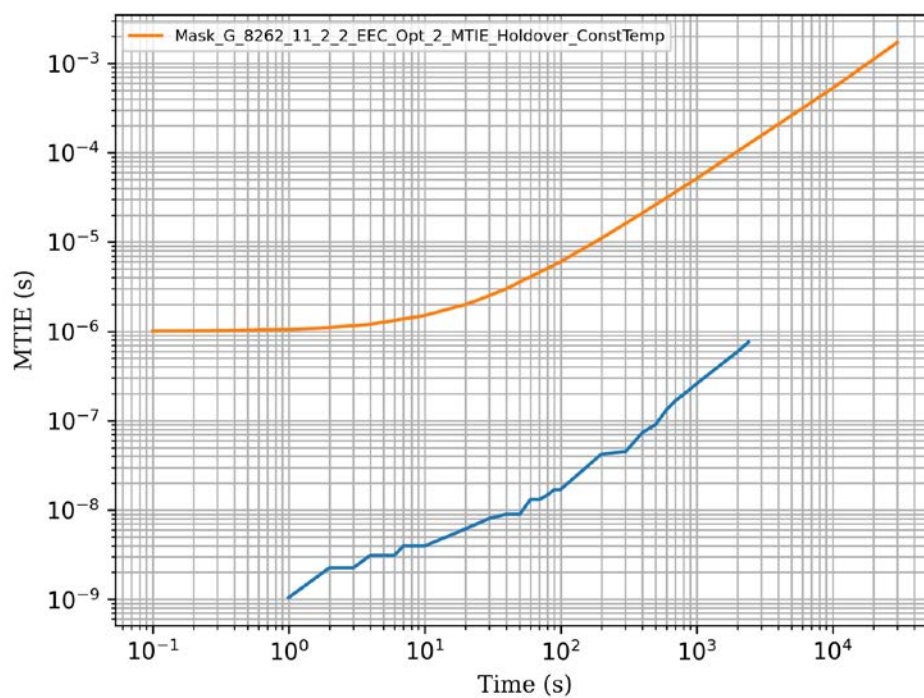
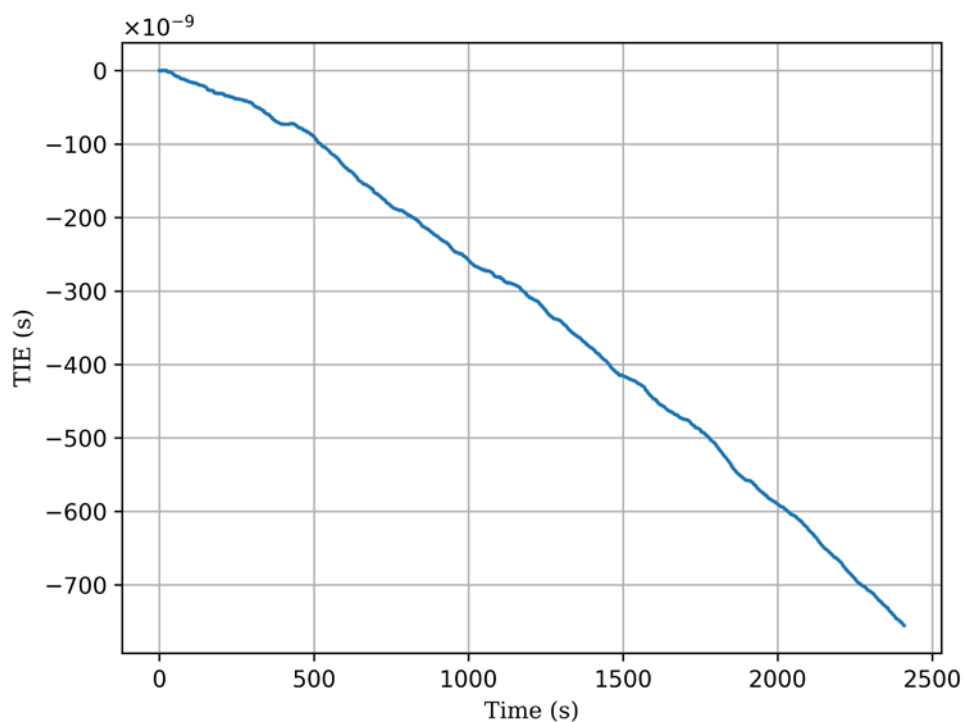


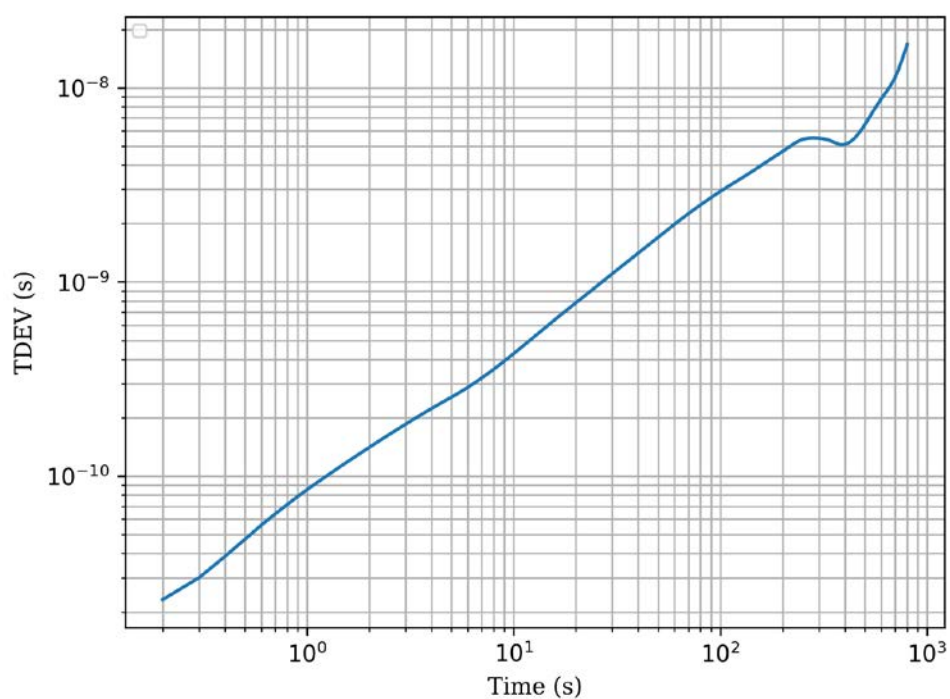
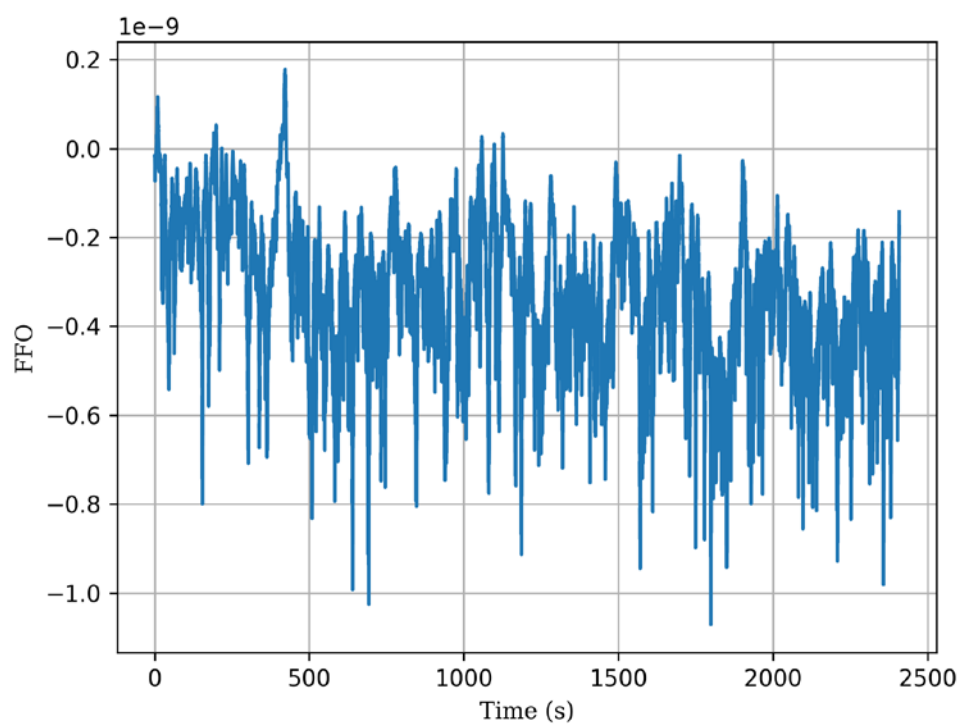
5.5 Wander in Locked Mode – G8262_EEC2



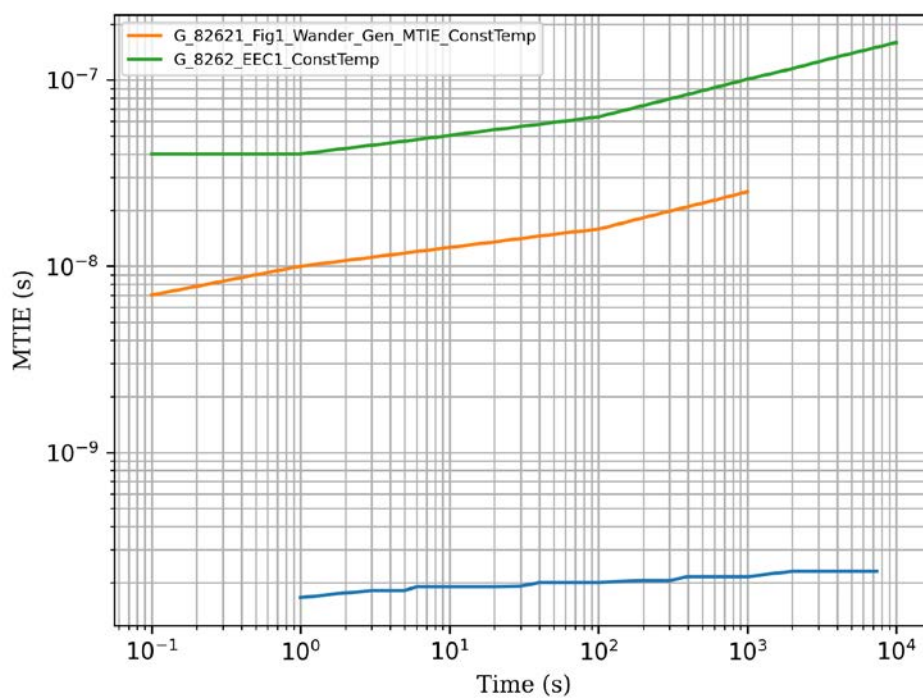
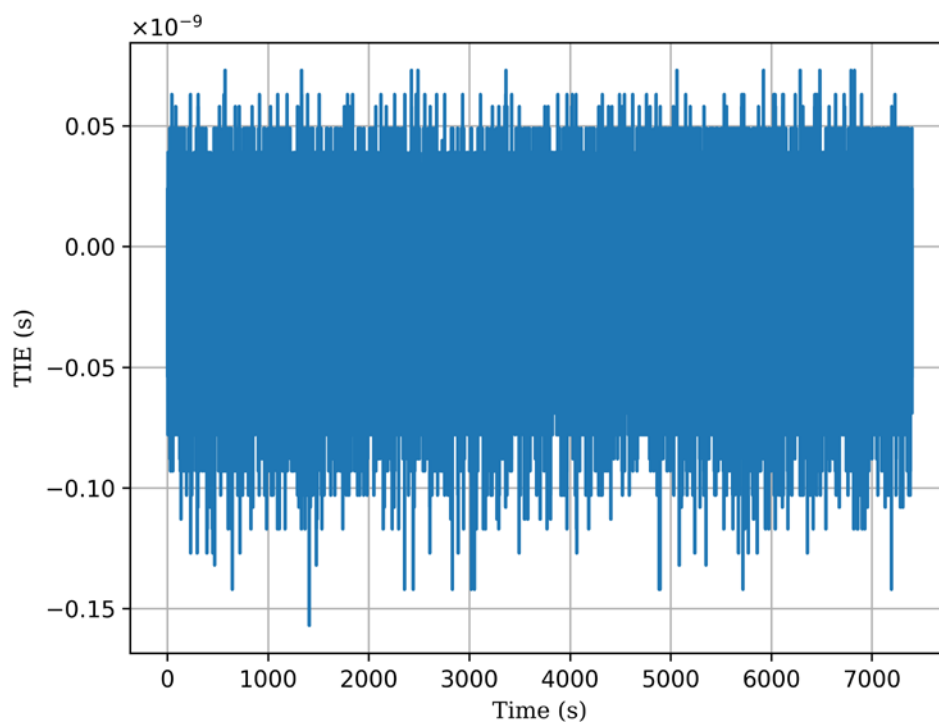


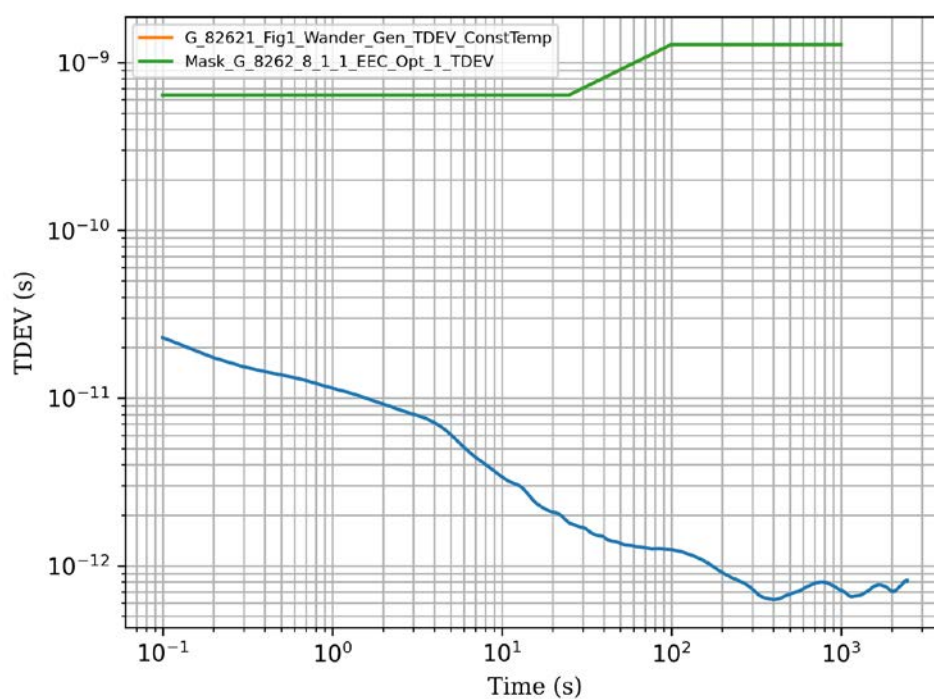
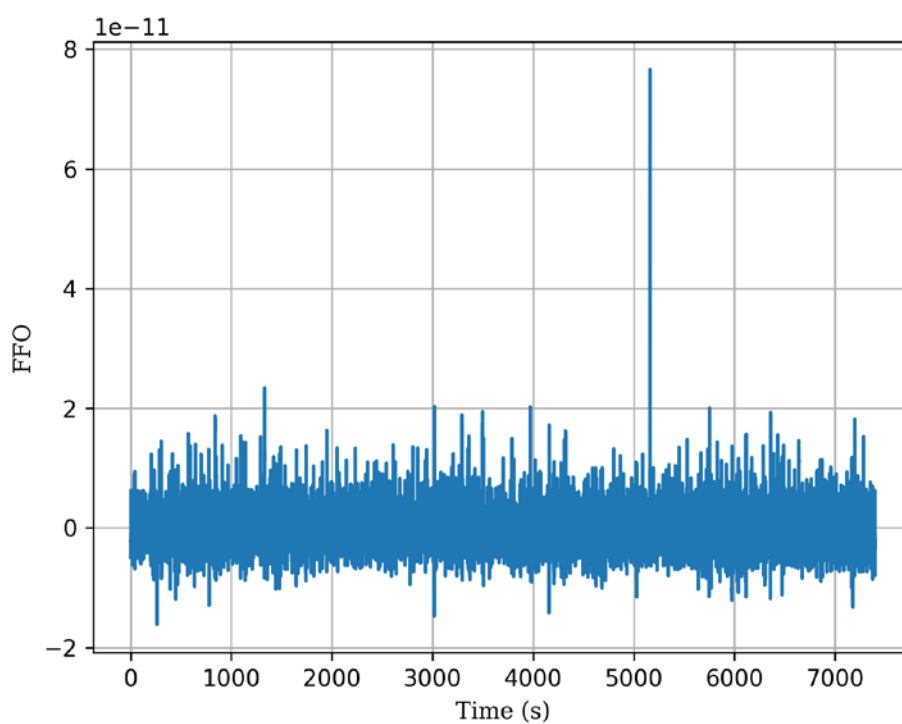
5.6 Long-term Phase Transient Response – G8262_EEC2



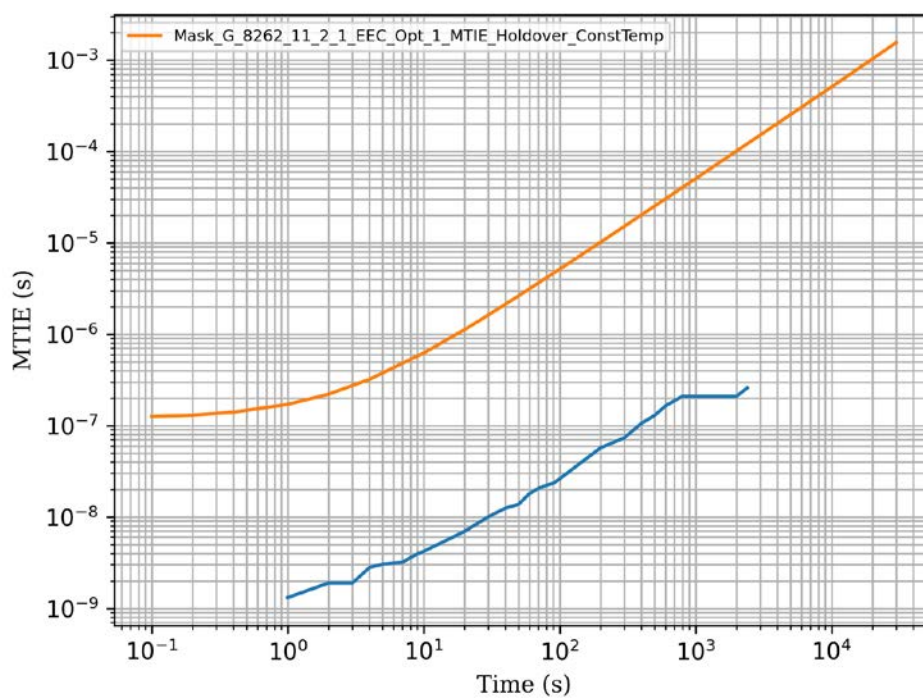
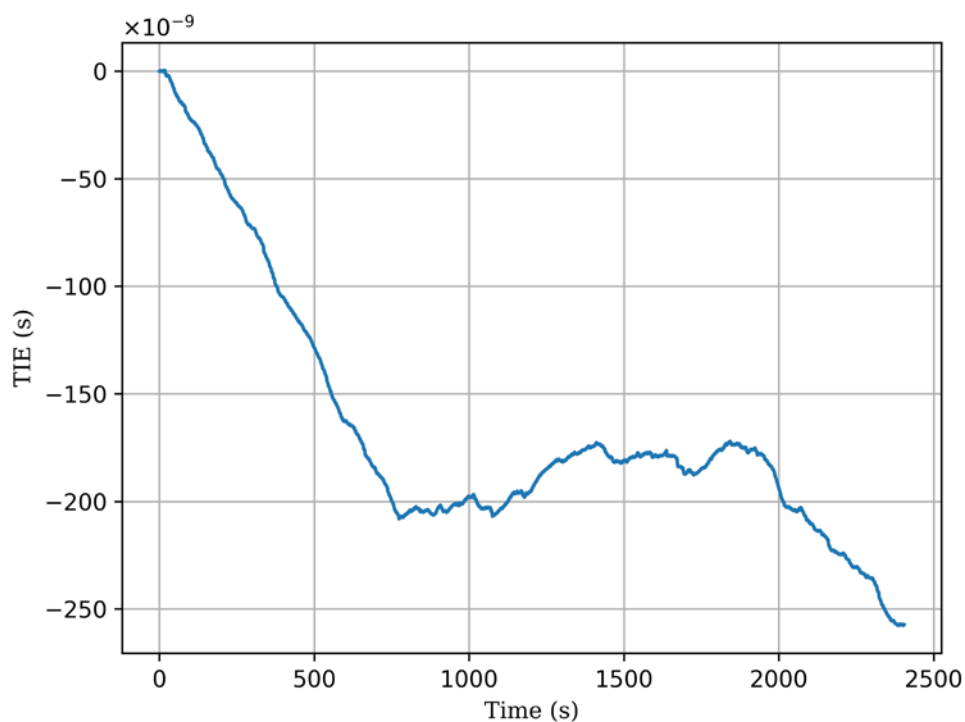


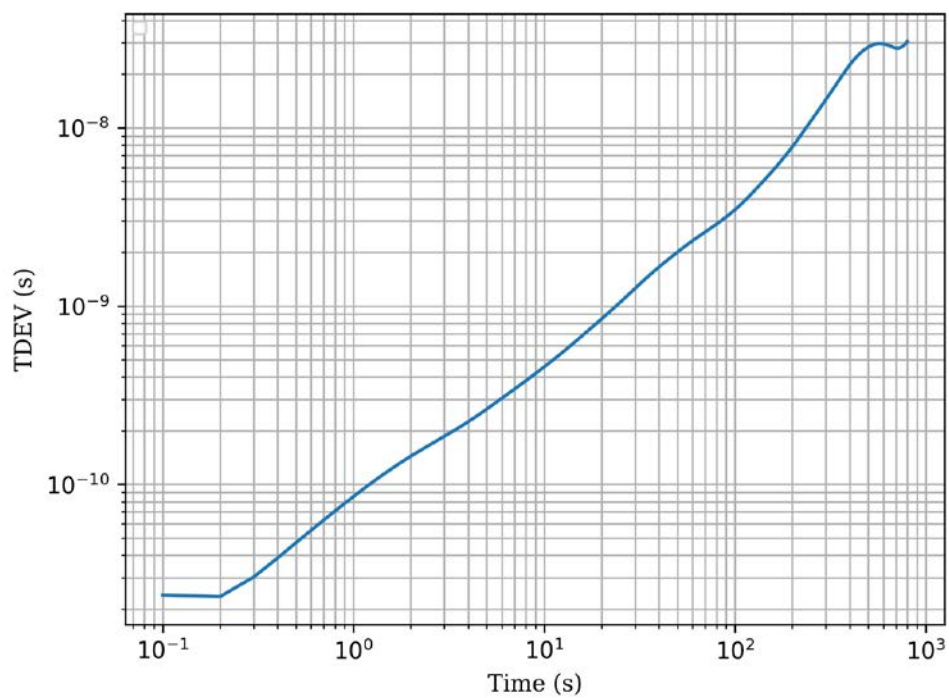
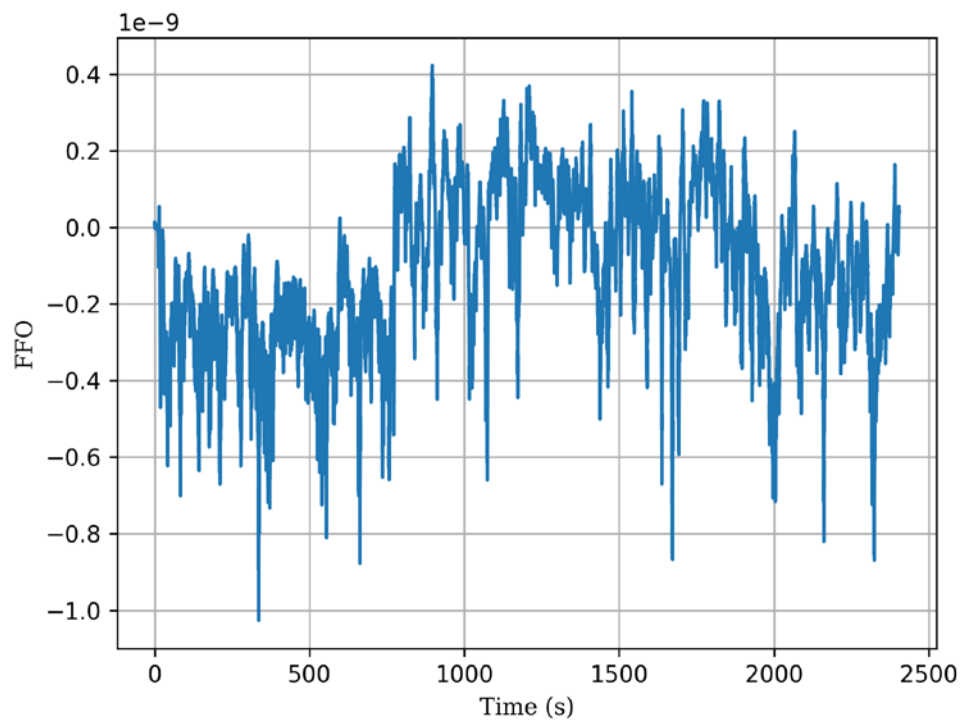
5.7 Wander in Locked Mode – G8262_eEEC_3Hz





5.8 Long-term Phase Transient Response - G8262_eEEC_3Hz





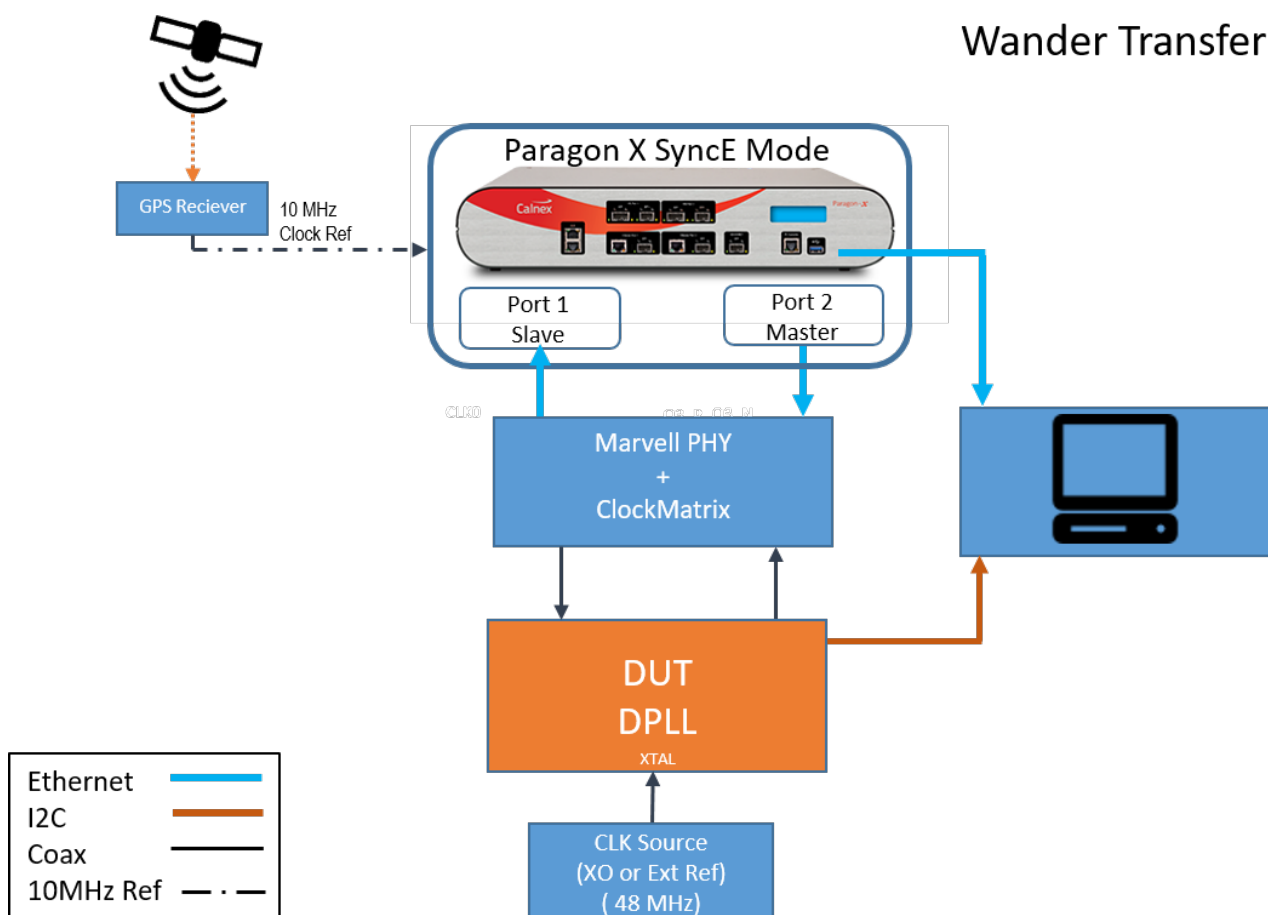
6. Noise Tolerance

This is part of noise transfer testing. The ClockMatrix™ PLL is monitored so that it does not leave the LOCK state during noise transfer testing.

7. Jitter Tolerance

The ClockMatrix™ PLL has a programmable lock threshold to tolerate large amounts of jitter at the input. To meet the jitter tolerance for EEC for any peak-peak jitter amplitude (UI), it is recommended to set the lock threshold to 250ns.

8. Noise (Wander) Transfer



Wander Transfer is a test that requires a PLL to receive a clock containing varying amounts of wander and suppressing that wander based on the damping factor of the PLL. Wander begins at Paragon-X, a device that can place sinusoidal wander at varying frequencies and amplitudes through an Ethernet port. A proprietary PHY recovers the clock on this Ethernet line and sends the signal to an external Renesas PLL. The PLL acts as a transparent device to pass the wander to the DUT at the frequency specified by the standard. The DUT then cleans up the signal and returns it through the PLL and the proprietary PHY where it is measured by Paragon-X to determine the phase gain present in the signal.

Note: Paragon-X does not natively create a Gain (dB) vs. Frequency (Hz) graph when running wander transfer with a table of sinusoidal frequencies. The graphs in this report requiring that type of test are created by parsing the data that Paragon-X calculates during the test and plotting it. Results for the TDEV style of wander transfer used for ITU-T G.8262 EEC Option 2, however, are generated and plotted by Paragon-X.

8.1 Noise Transfer – G8262_EEC1_1Hz

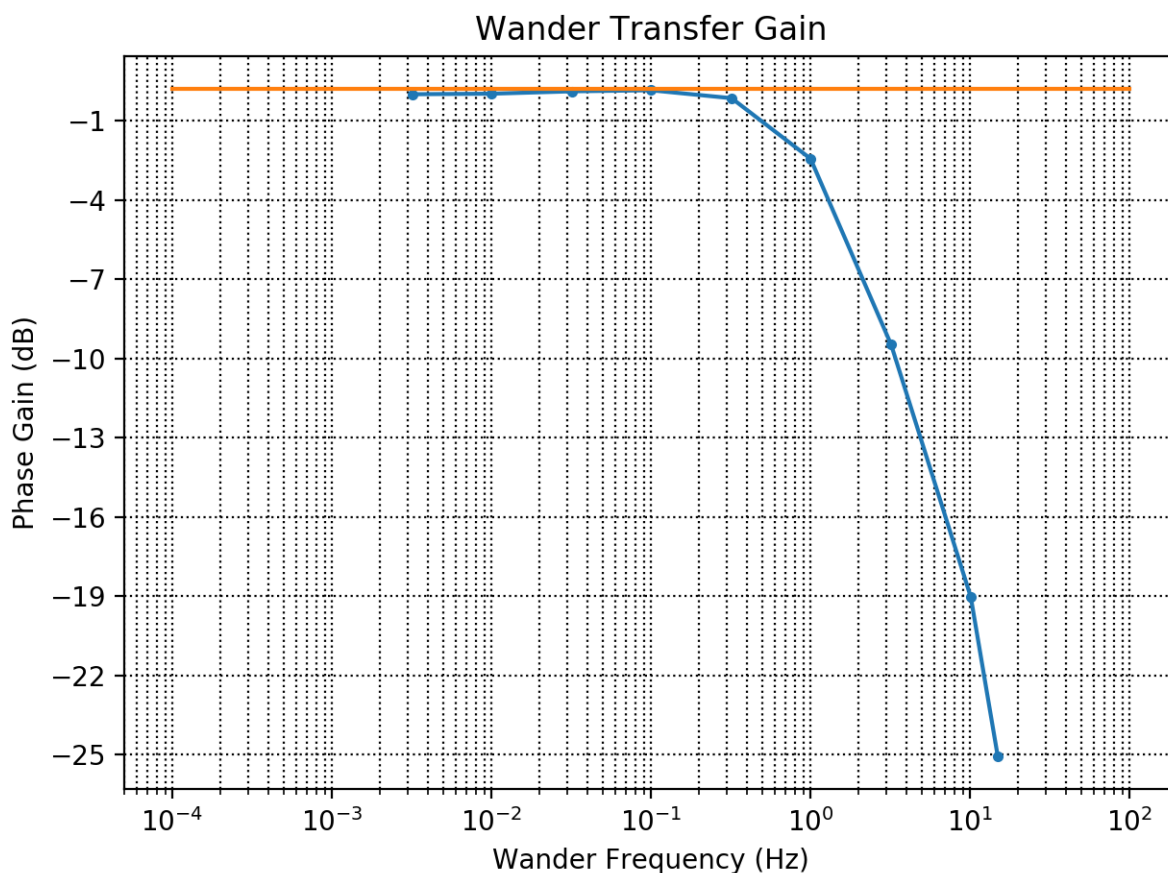


Table 2. Wander Transfer Gain Peaking for Standard – G8262_EEC1_1Hz

Frequency (Hz)	Gain Peaking (dB)
0.0032	0.01
0.01	0.03
0.032	0.12
0.1	0.16
0.32	-0.14
1.0	-2.43
3.2	-9.47
10.1	-19.02
14.9	-25.04

8.2 Noise Transfer – G8262_EEC1_10Hz

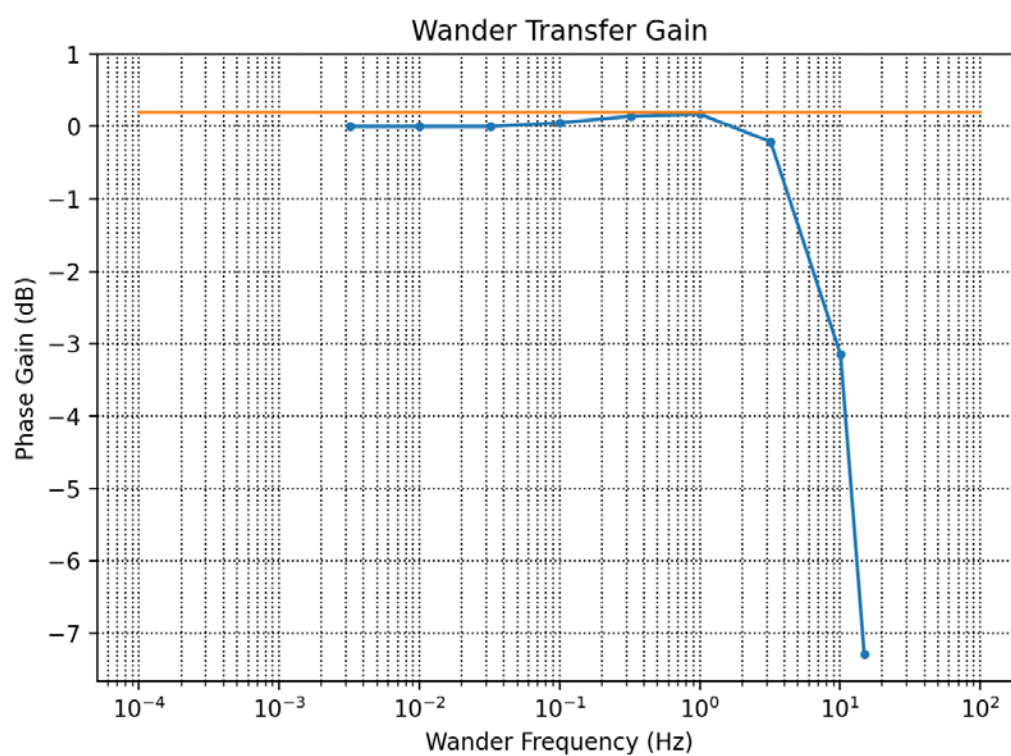
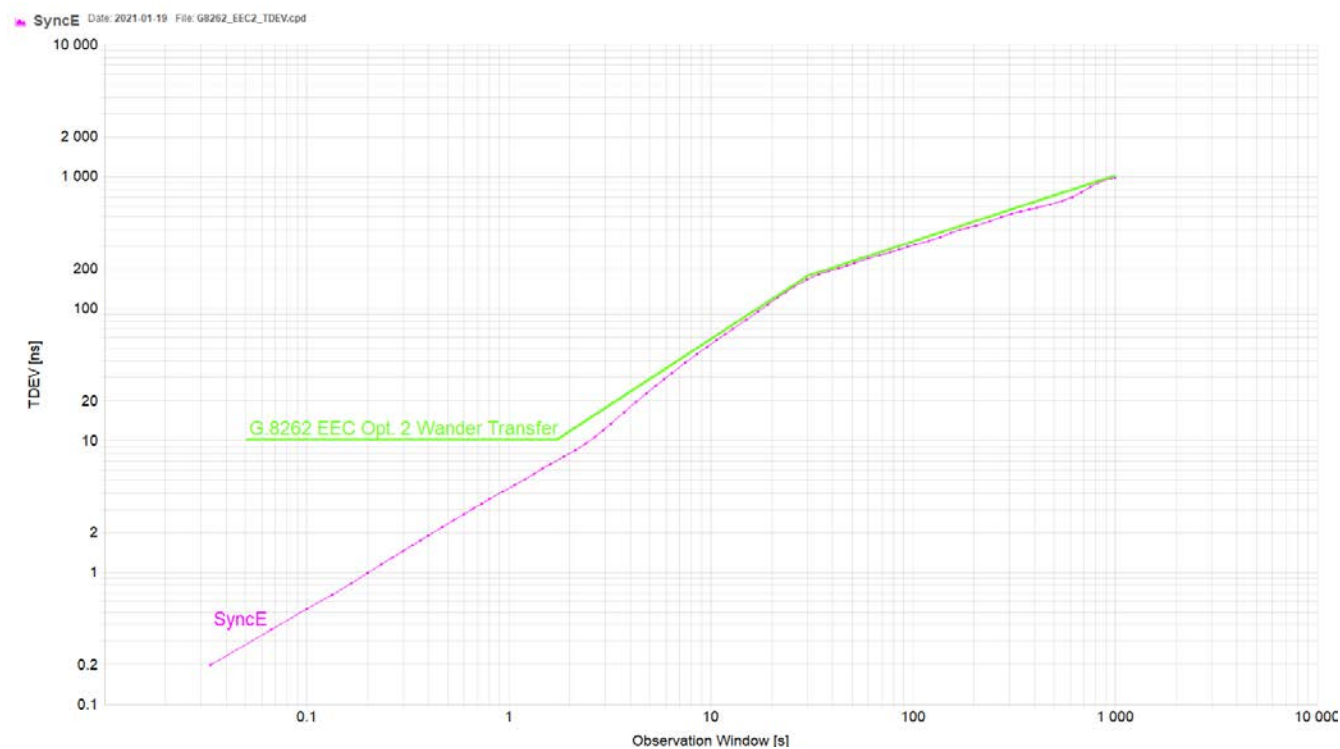


Table 3. Wander Transfer Gain Peaking for Standard - G8262_EEC1_10Hz

Frequency (Hz)	Gain Peaking (dB)
0.0032	0.00
0.01	0.00
0.032	0.00
0.1	0.05
0.32	0.14
1.0	0.17
3.2	-0.21
10.1	-3.15
14.9	-7.29

8.3 Noise Transfer – G8262_EEC2



8.4 Noise Transfer – G8262_eEEC_3Hz

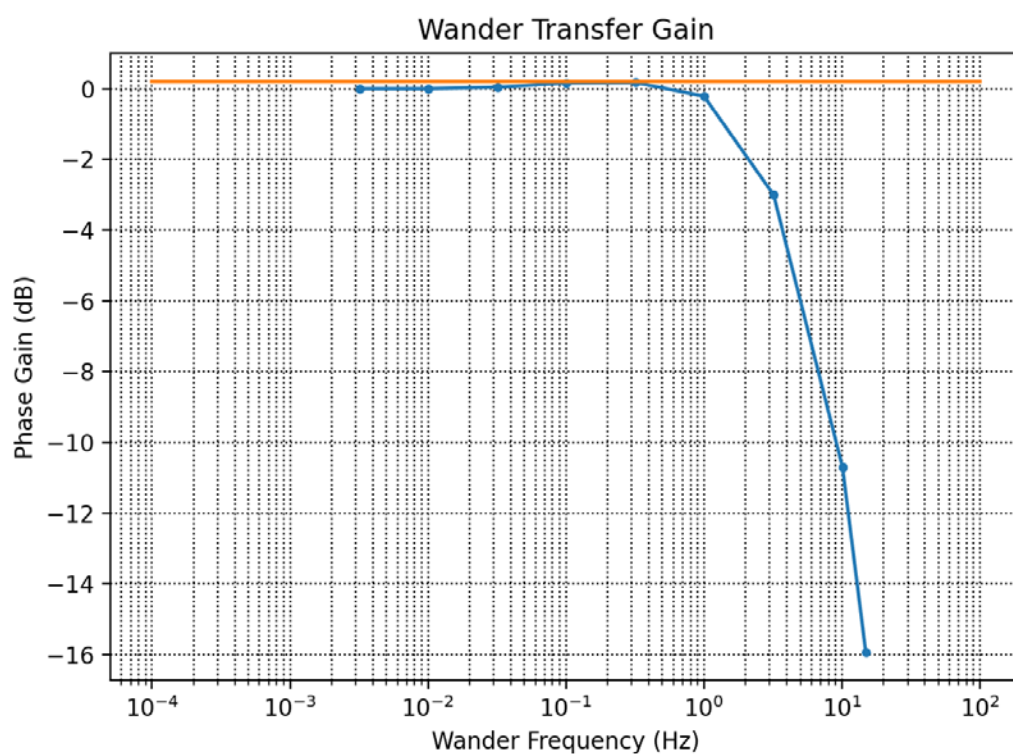
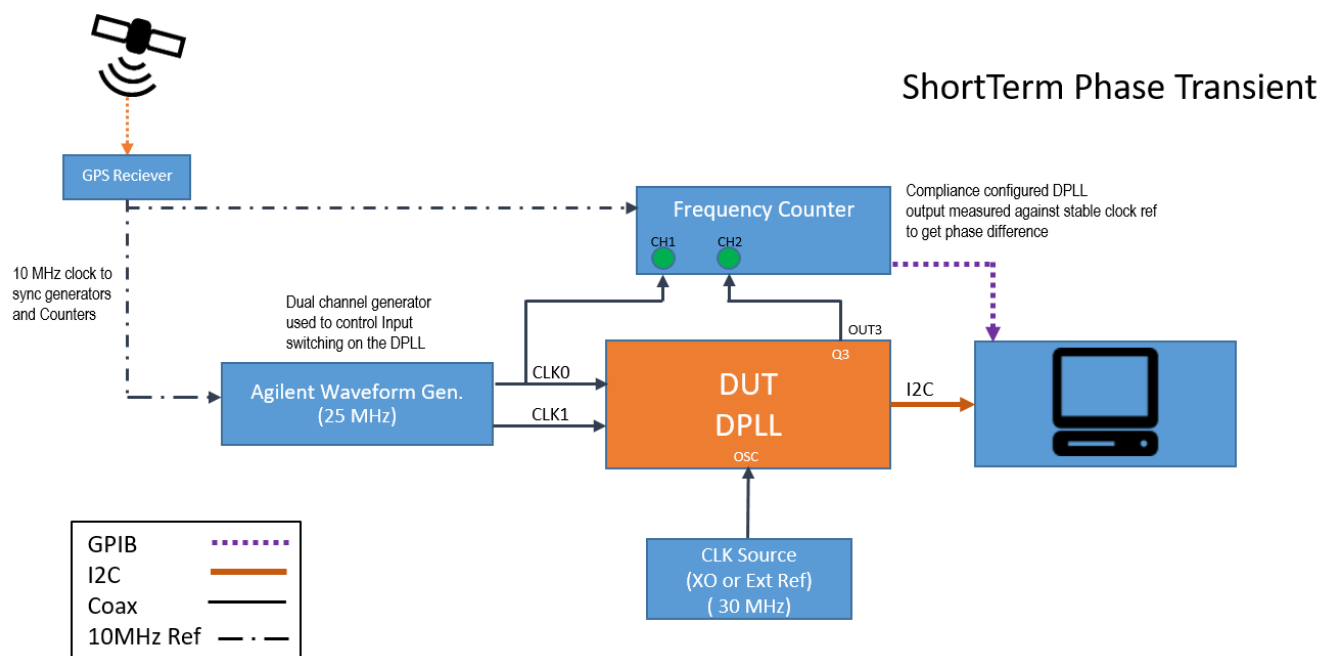


Table 4. Wander Transfer Gain Peaking for Standard - G8262_EEC1_10Hz

Frequency (Hz)	Gain Peaking (dB)
0.0032	0.00
0.01	0.00
0.032	0.04
0.1	0.16
0.32	0.17
1.0	-0.21
3.2	-3.00
10.1	-10.69
14.9	-15.92

9. (Phase) Transient Response – Short-term



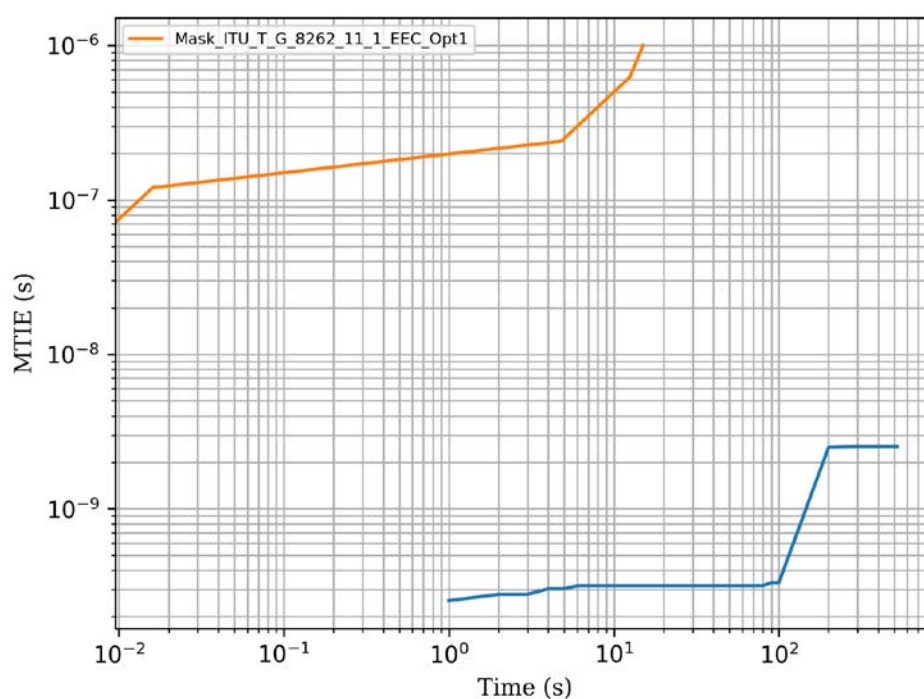
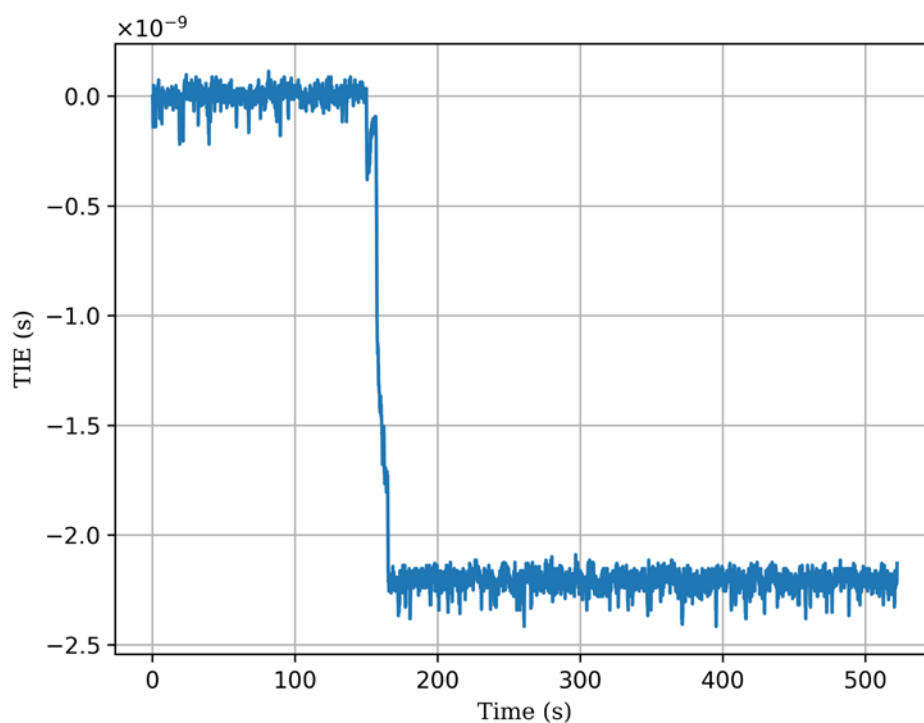
Short-term phase transient response requirement reflects the performance of the DUT in cases when the (selected) input reference is lost due to a failure in the reference path and a second reference input signal, traceable to the same reference clock, is available simultaneously, or shortly after the detection of the failure.

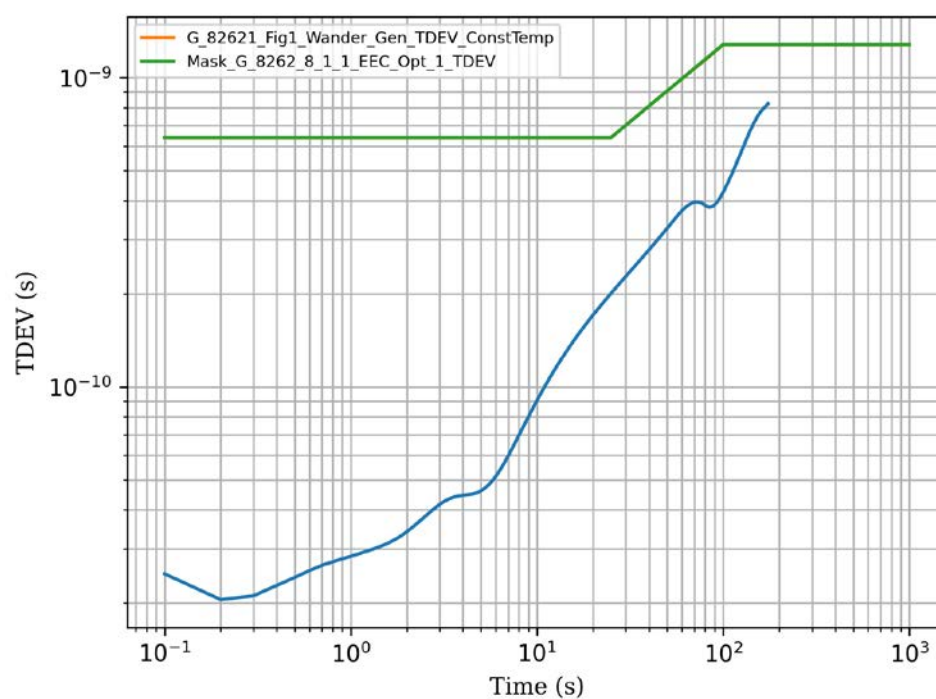
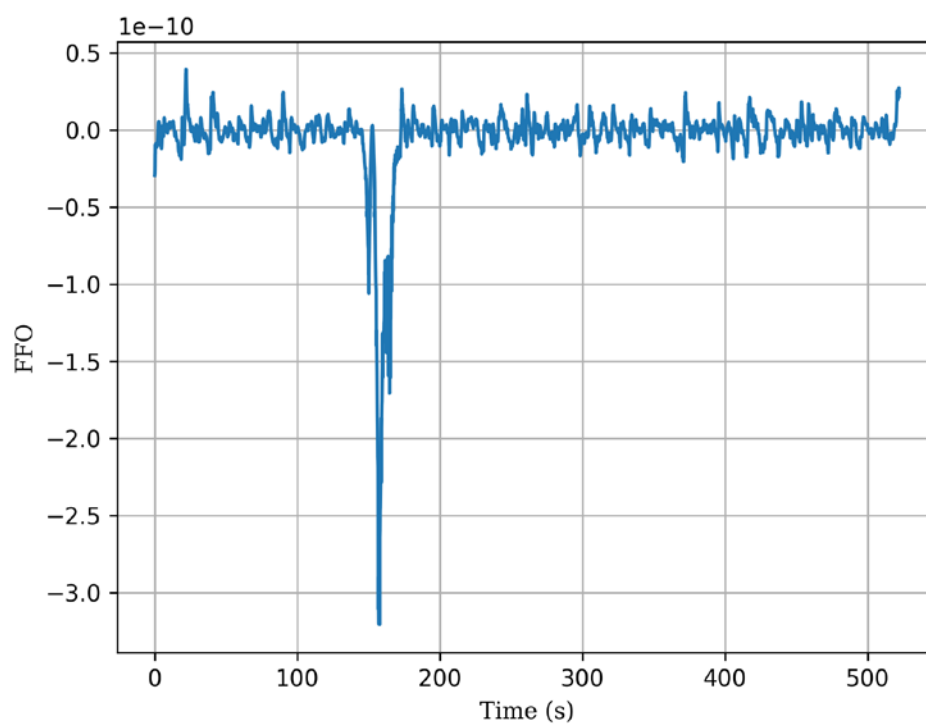
The test was carried out by providing reference clock inputs on CLK0 and CLK1 from the Agilent waveform generator, which are 180° out of phase from each other. The PLL is locked to the clock signal from CLK0 for a given period of time before producing a phase transient by turning off the input reference signal for 11 seconds, during this time the clock on CLK1 is unavailable. The DPLL goes into holdover during the 11 second period because no other reference is available. After 11 seconds the reference signal on CLK1 is turned ON and PLL locks to the newly available reference signal. The switching during the two transients Locked (CLK0) → holdover → Locked (CLK1) is carried out.

The output from the DUT is available on the OUT_3 and the phase time error is captured using the frequency counter. The results of the given transient are plotted against the mentioned standard profiles.

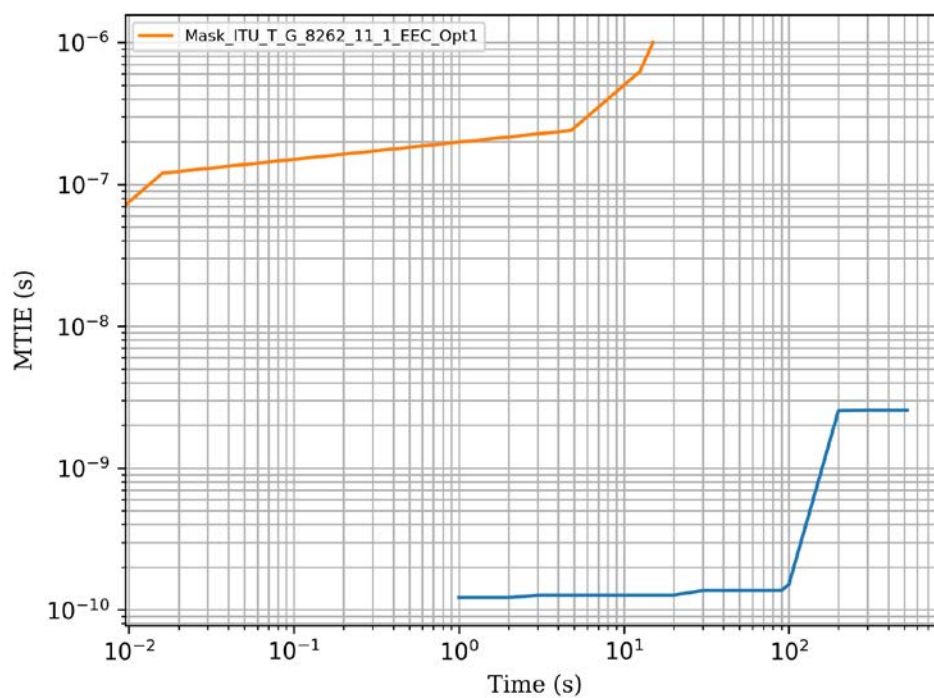
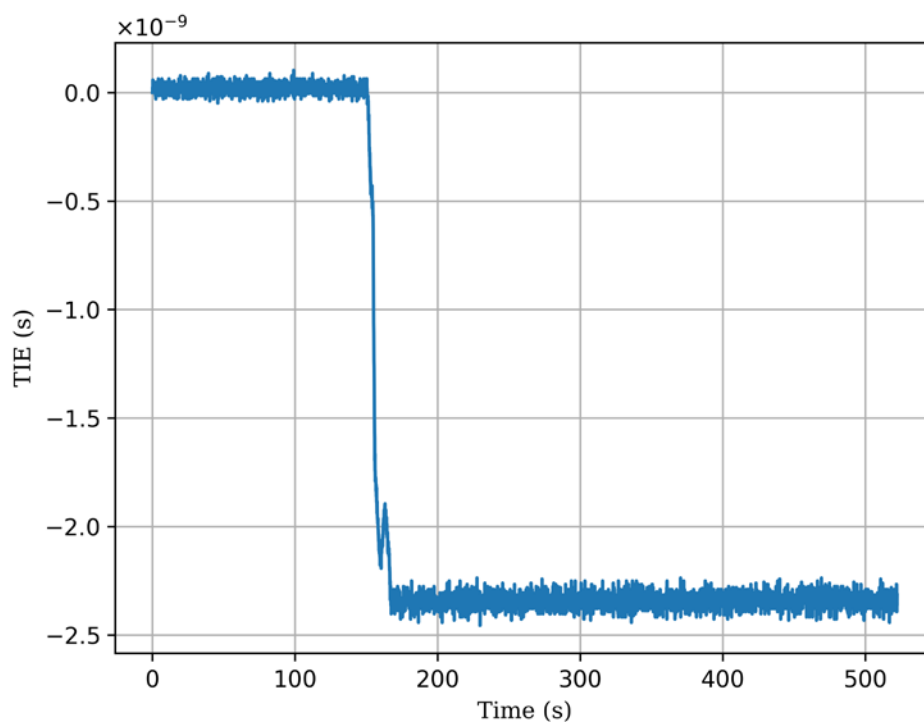
For reference clocks, < 1MHz it is recommended to enable Hitless switching to absorb phase offset.

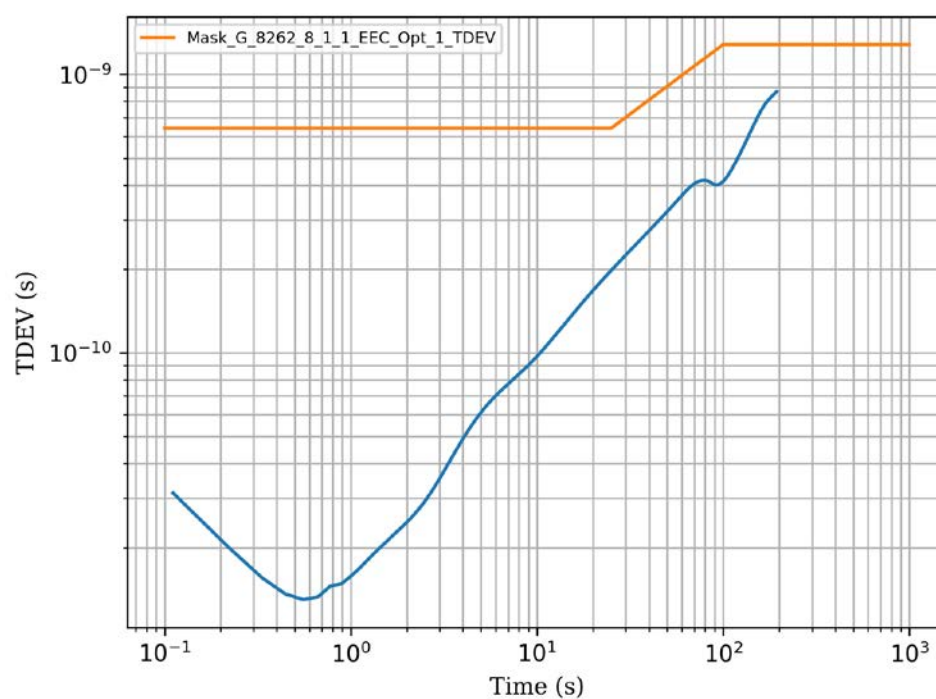
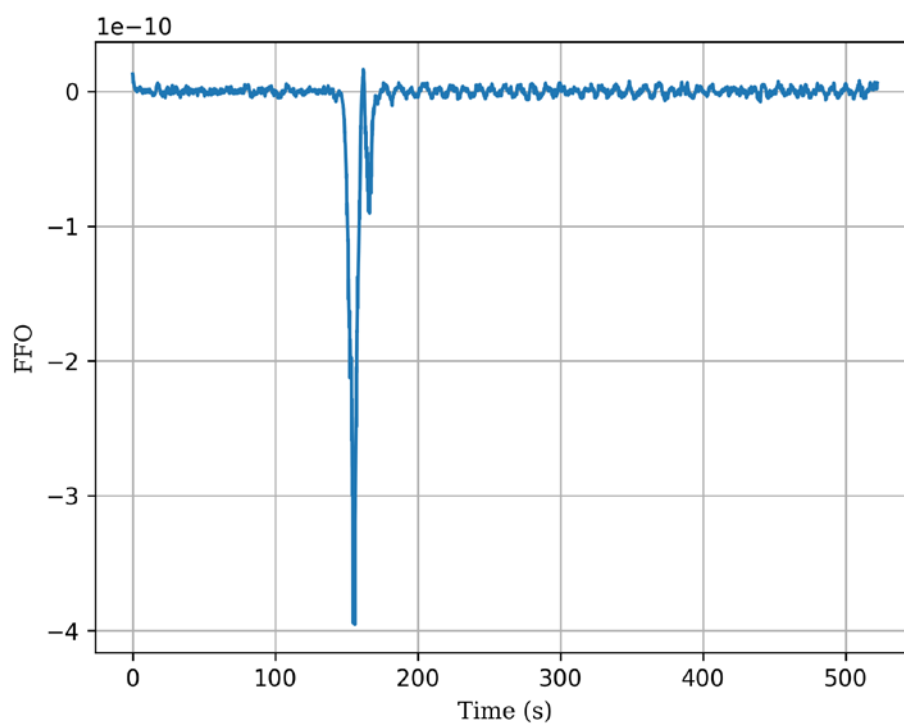
9.1 Short-term Phase Transient – G8262_EEC1_1Hz



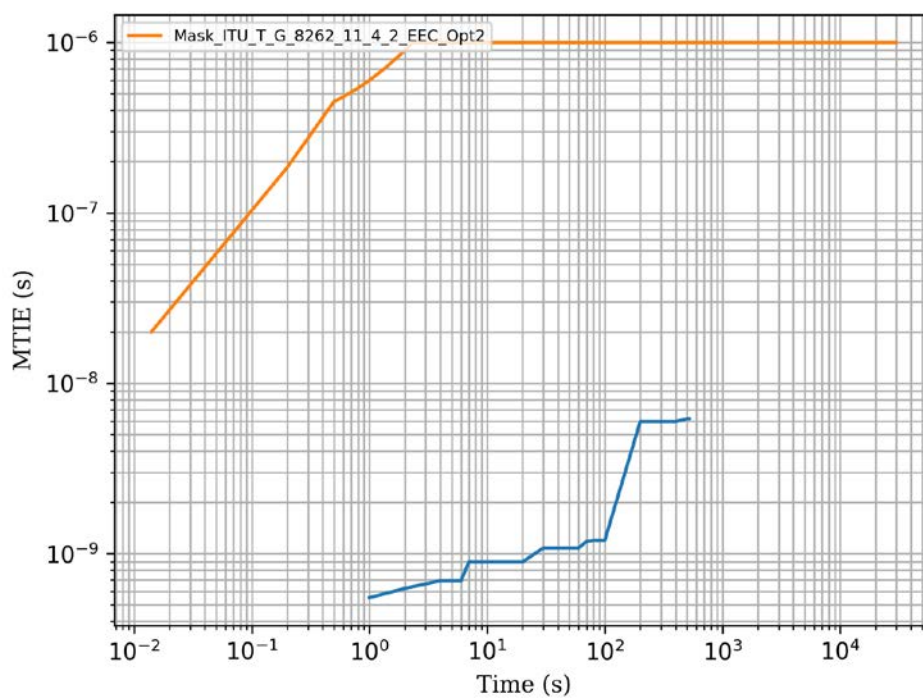
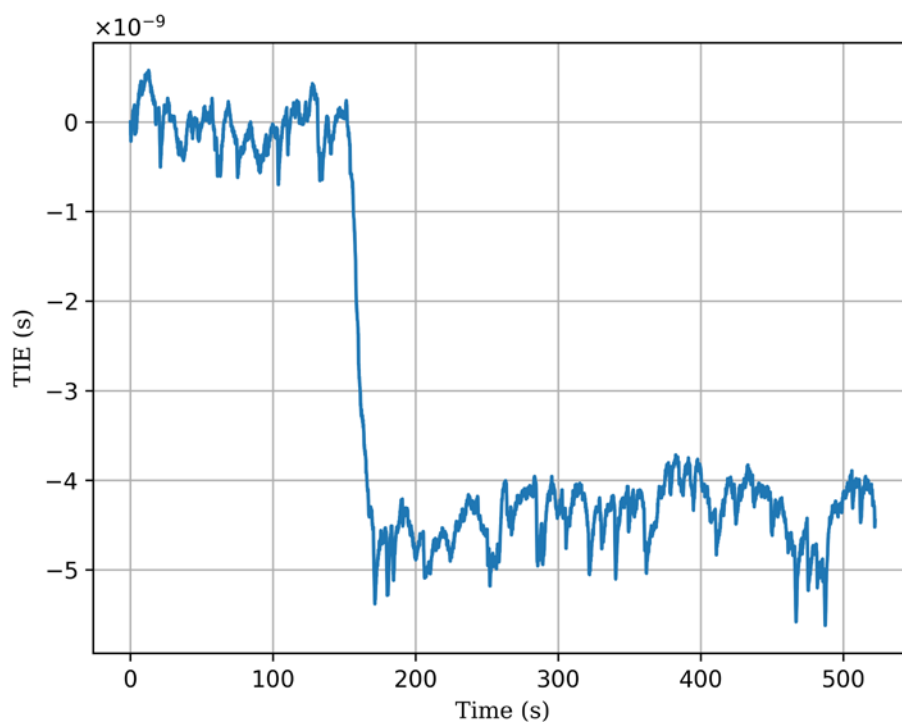


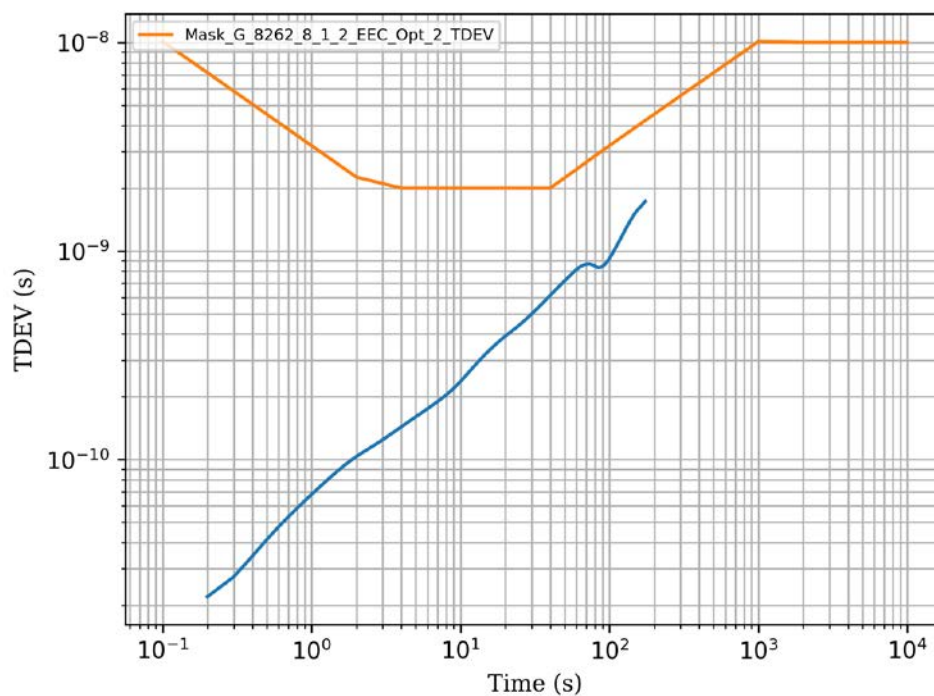
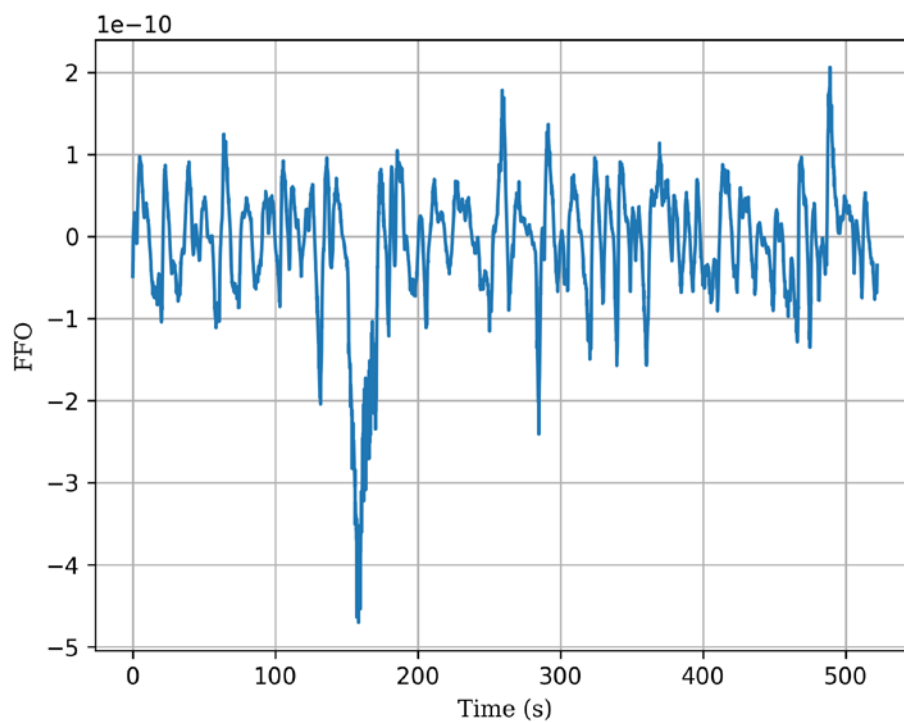
9.2 Short-term Phase Transient – G8262_EEC1_10Hz



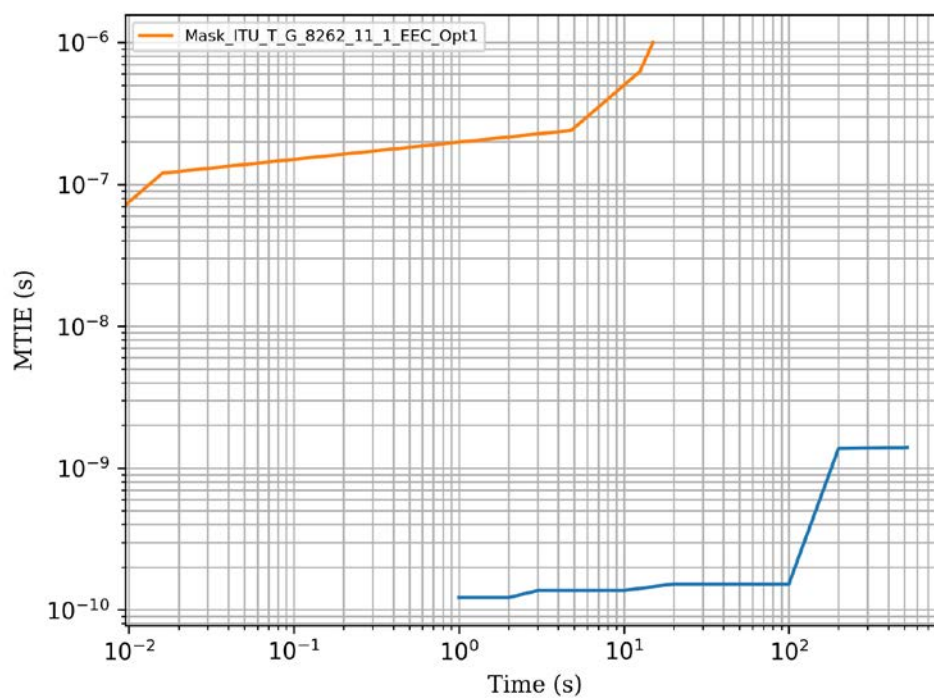
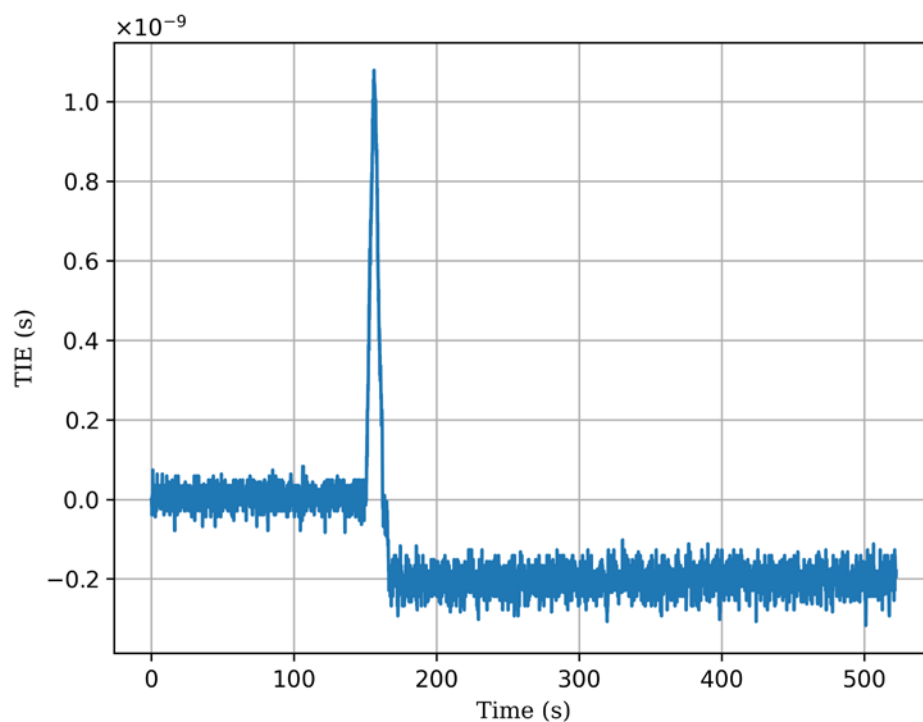


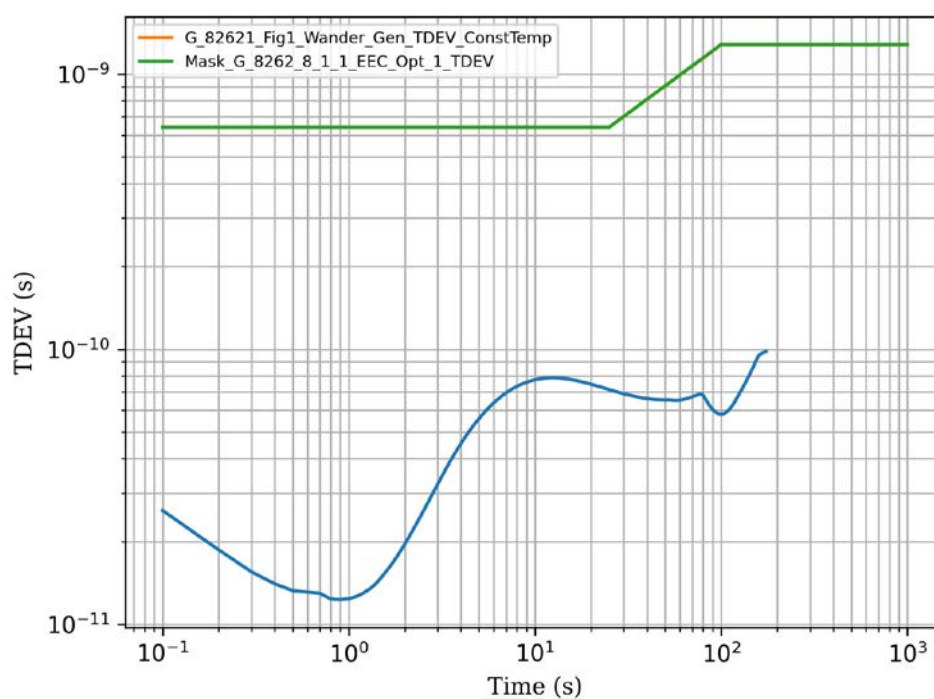
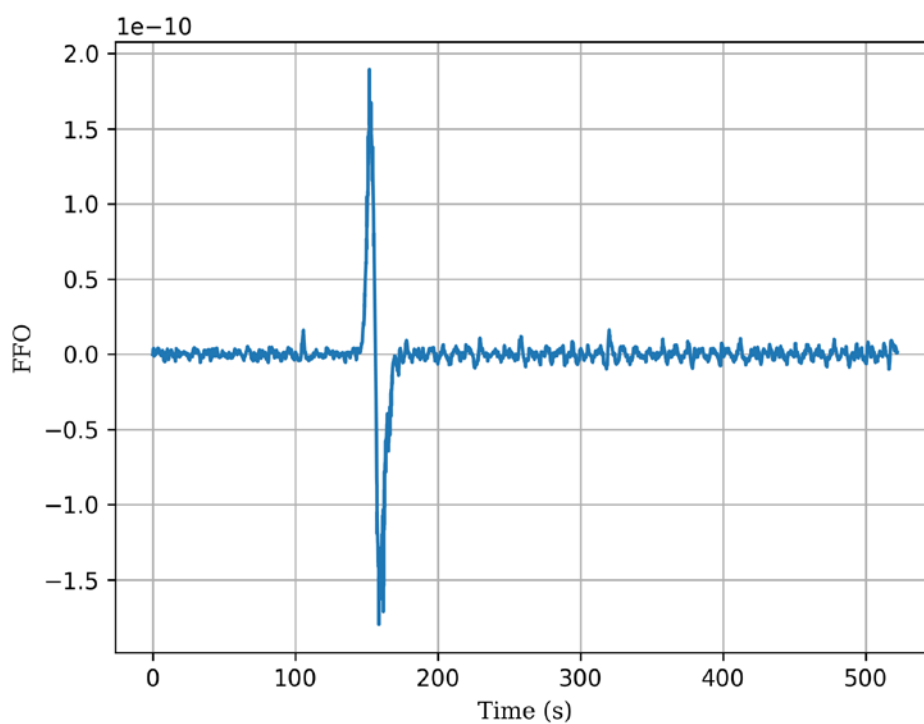
9.3 Short-term Phase Transient – G8262_EEC2



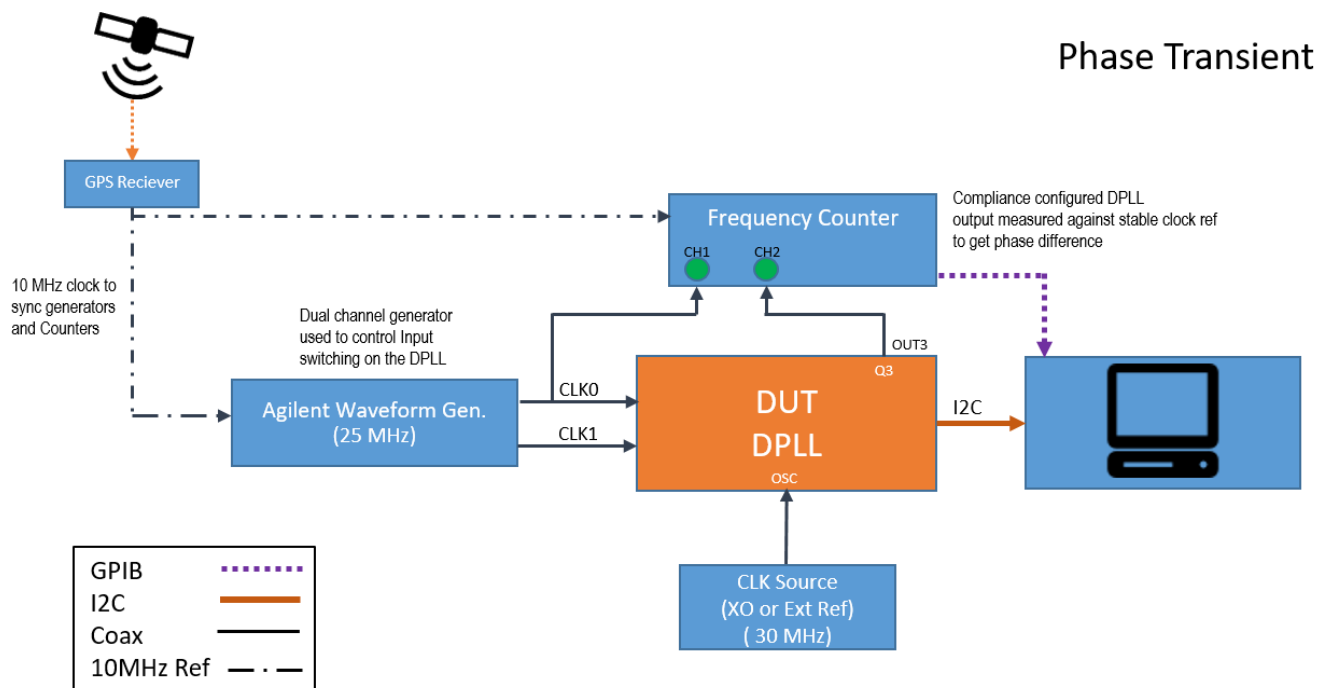


9.4 Short-term Phase Transient – G8262_eEEEC1_3Hz





10. (Phase) Transient Response – Input Signal Interruption

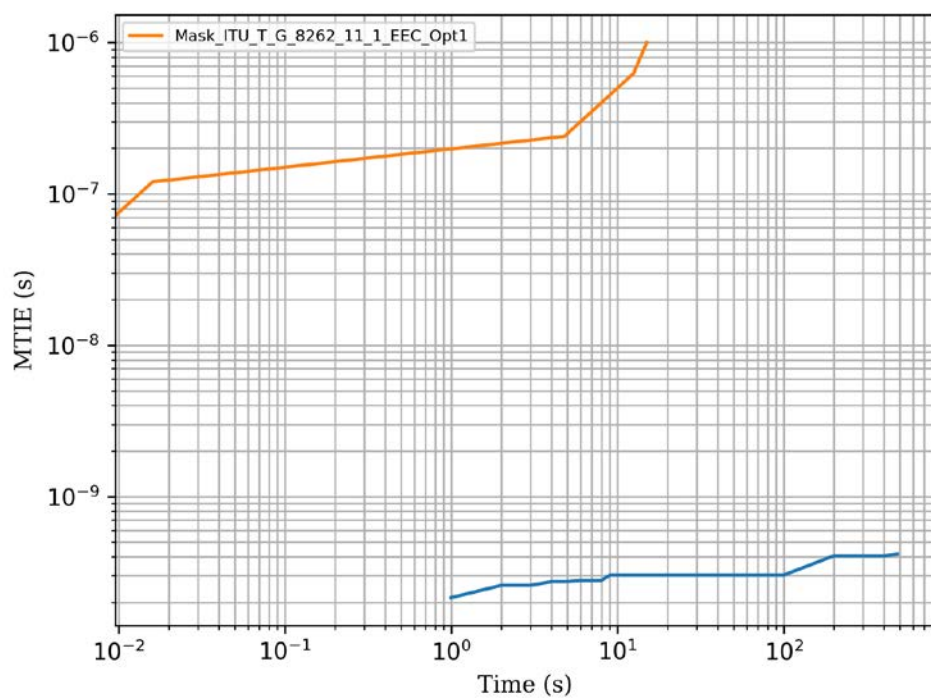
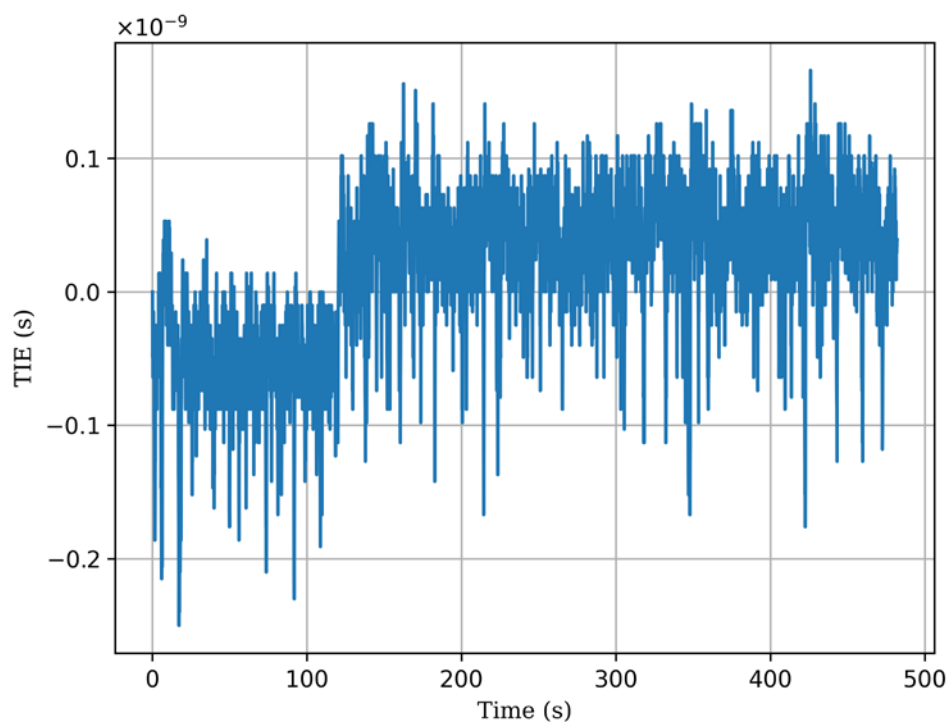


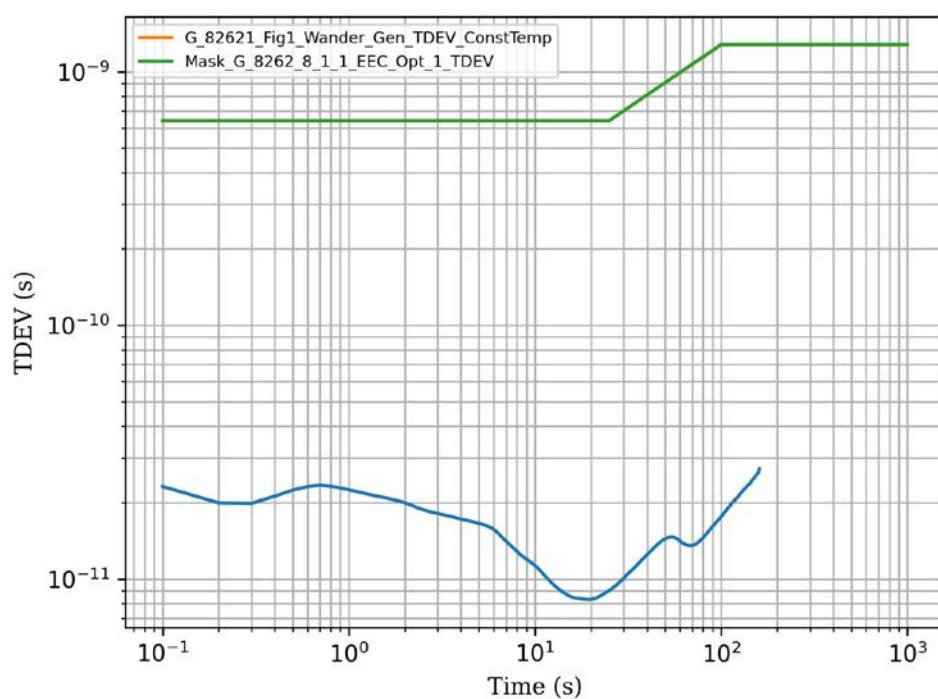
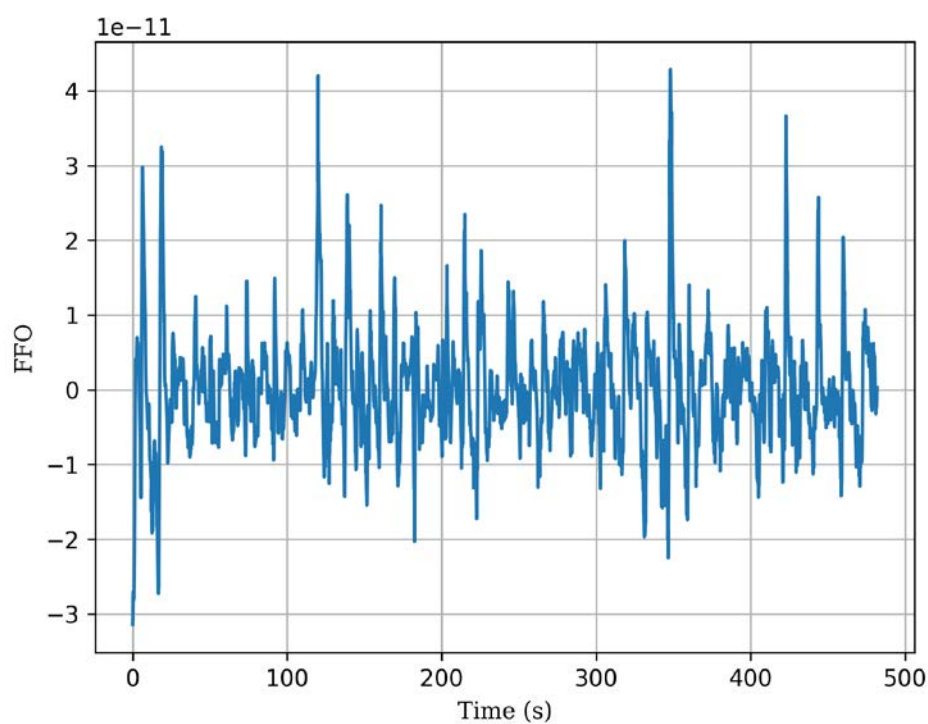
Transient response compliance checks the system response in situations where the input signal is affected by disturbances or transmission failures, which would result in phase transients at the synchronous EEC (Ethernet Equipment Clock) output. Short interruptions, switching between different reference clock signals, loss of reference etc., are categorized as transients, which would result in phase transients at the EEC output.

In this test the reference clock inputs are provided on CLK0 and CLK1 from the Agilent waveform generator, the PLL is locked to the clock signal from CLK0 for a given period of time before producing a phase transient by turning off the clock signal. The DPLL goes into holdover and tries to lock to any other qualified clocks. CLK1 is available from the Agilent waveform generator, and the DPLL switches to this clock which is very close in phase alignment to the original clock. The results of the given transient are plotted against the mentioned standard profiles.

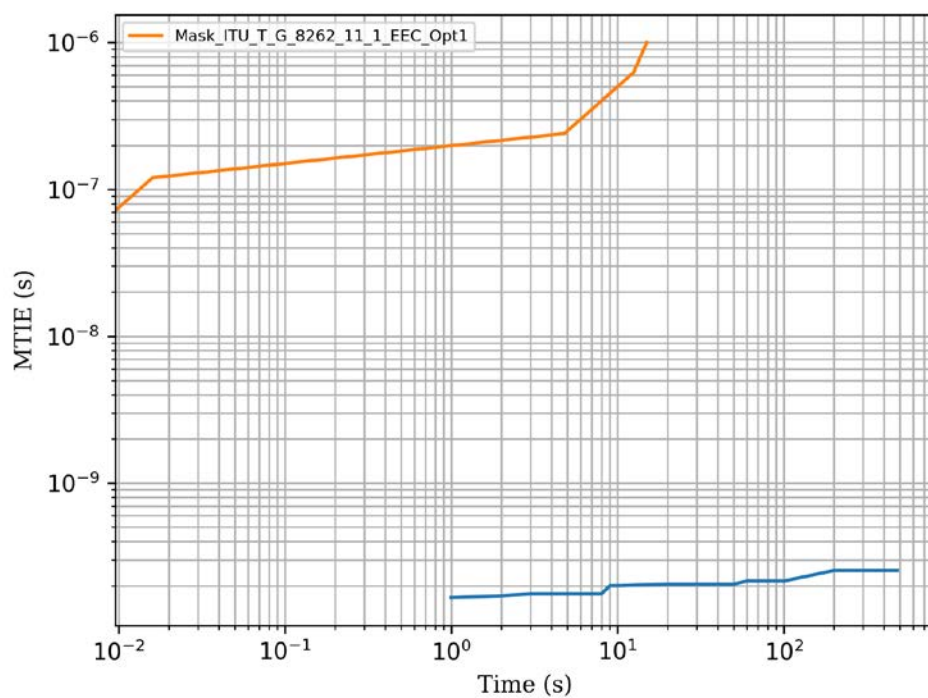
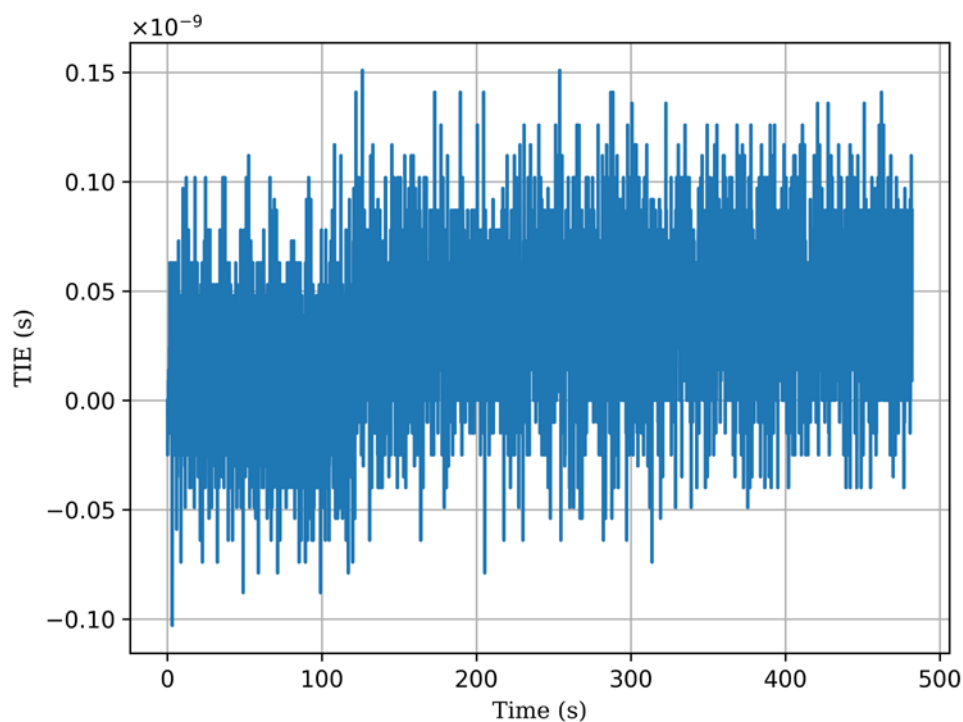
Hitless switching is disabled during this test.

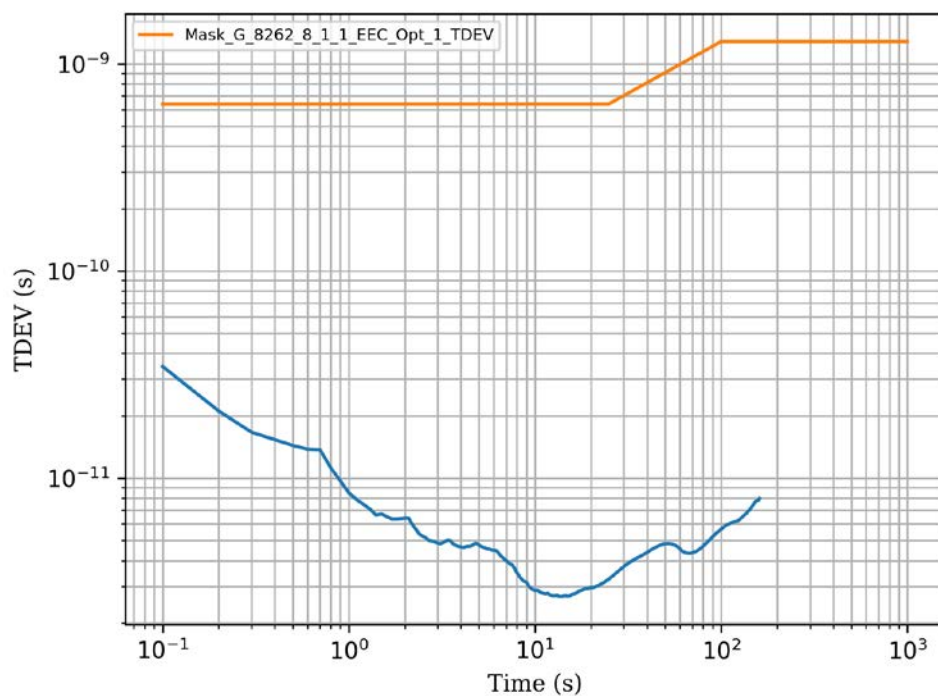
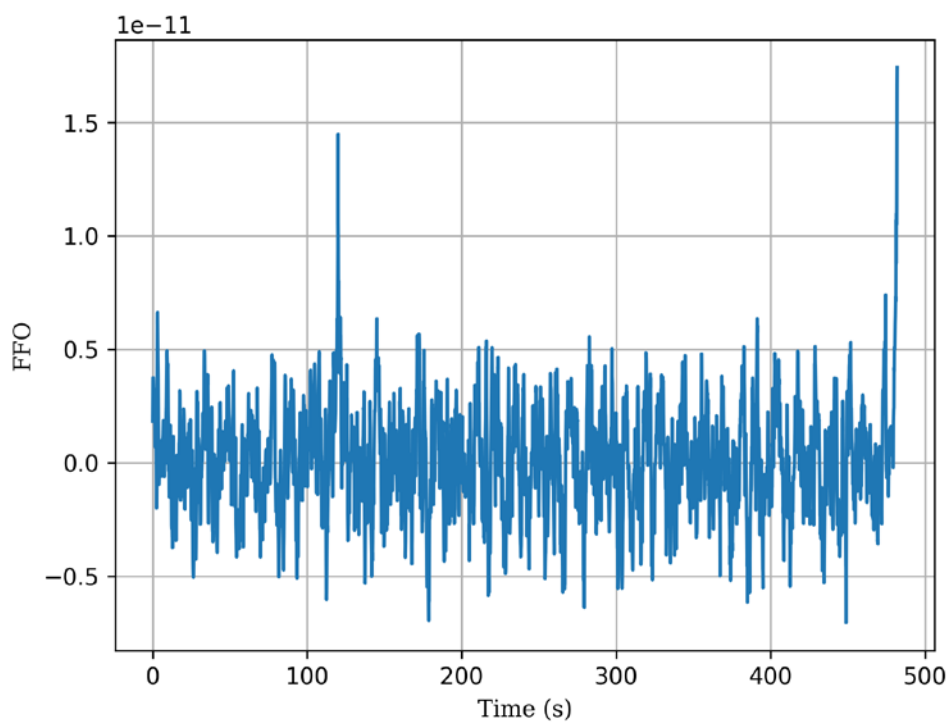
10.1 Phase Response to Input Signal Interruptions – G8262_EEC1_1Hz



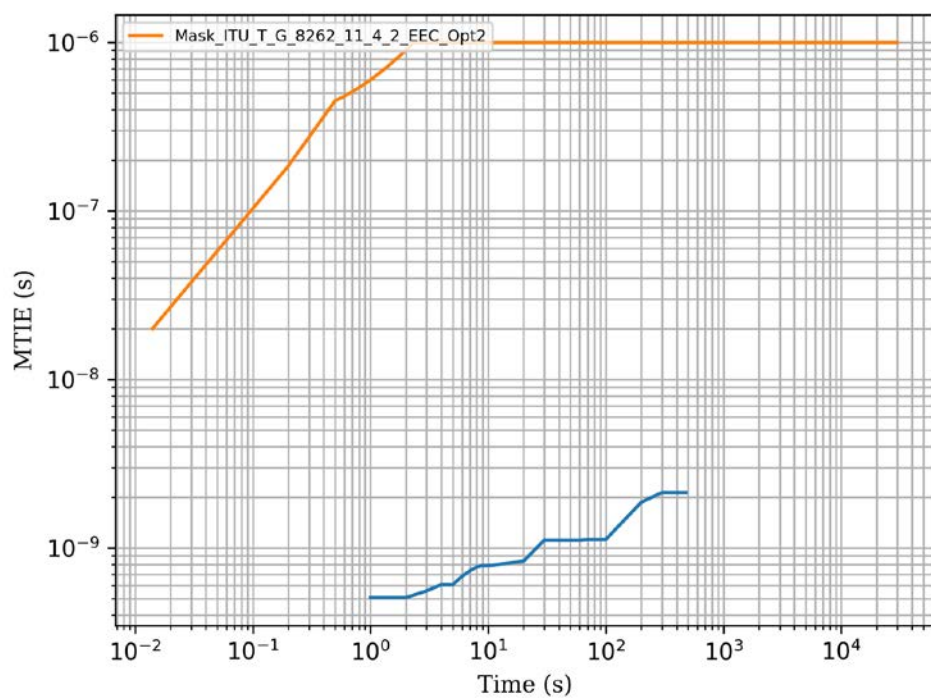
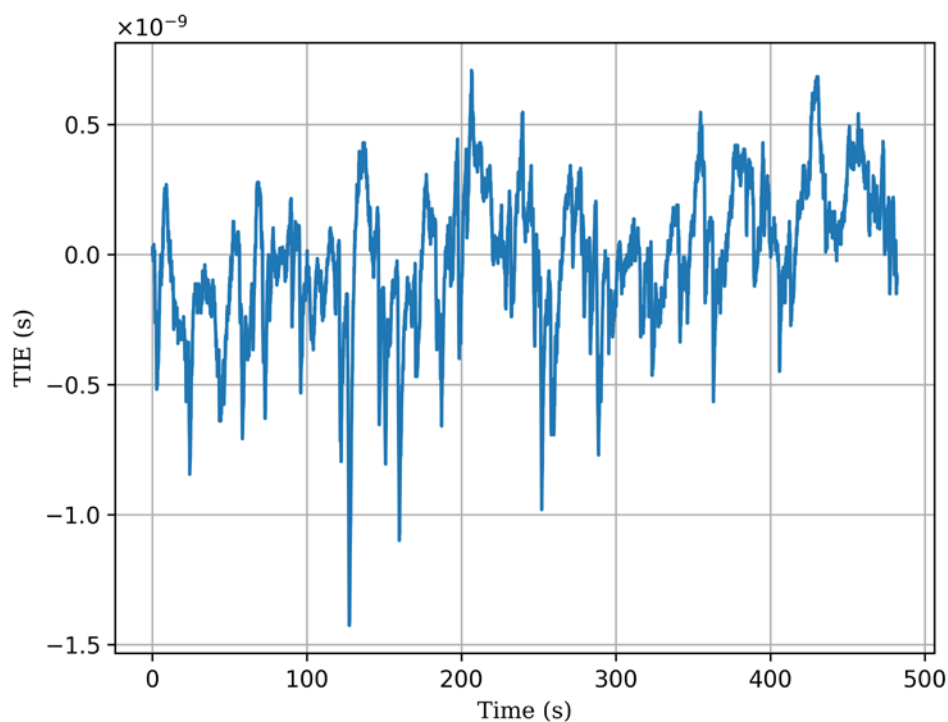


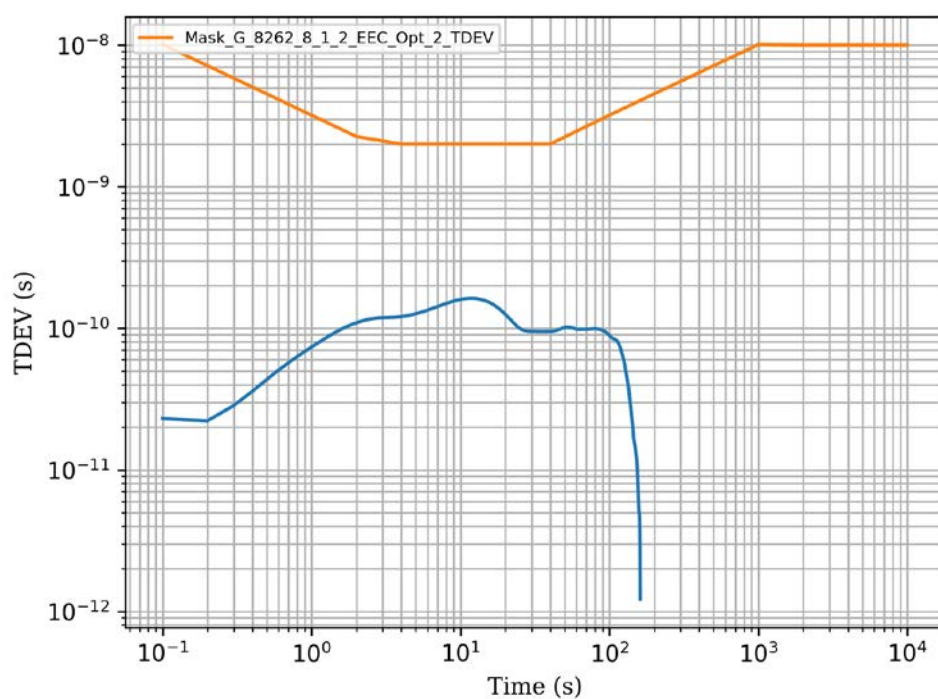
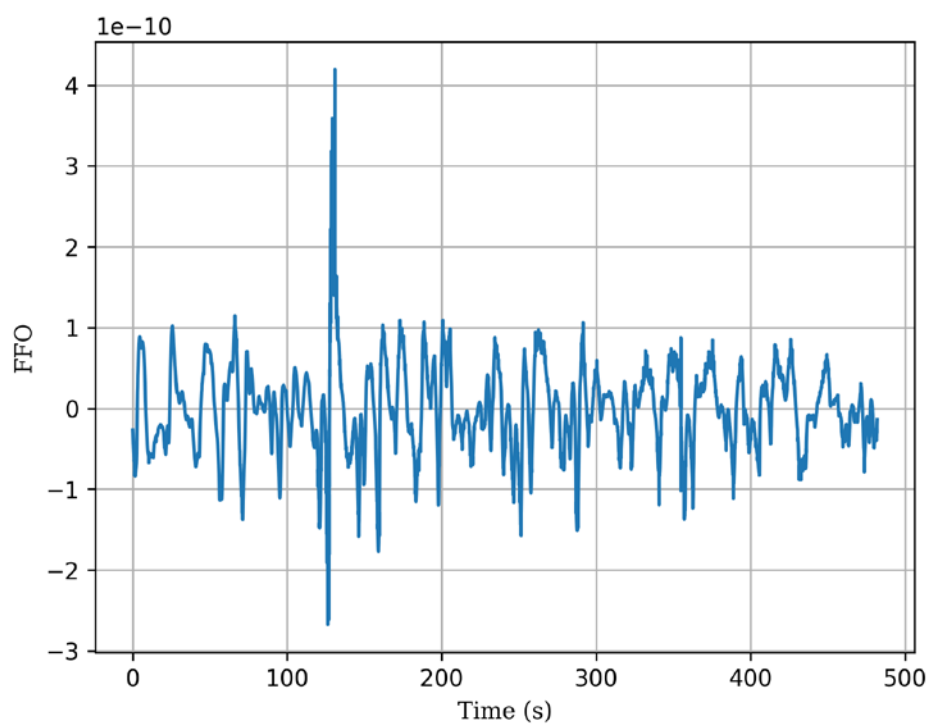
10.2 Phase Response to Input Signal Interruptions – G8262_EEC1_10Hz



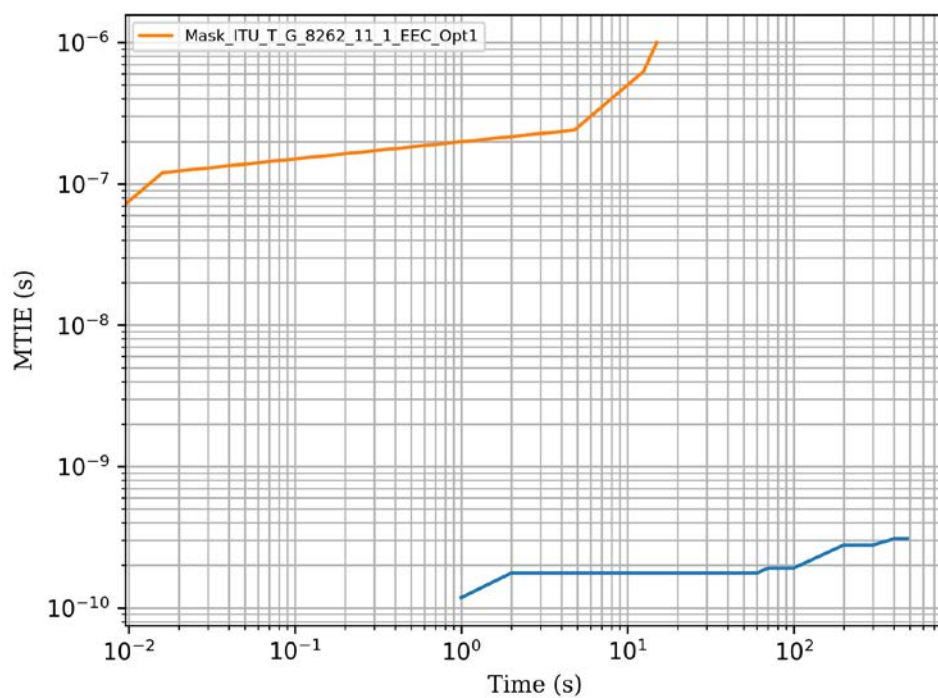
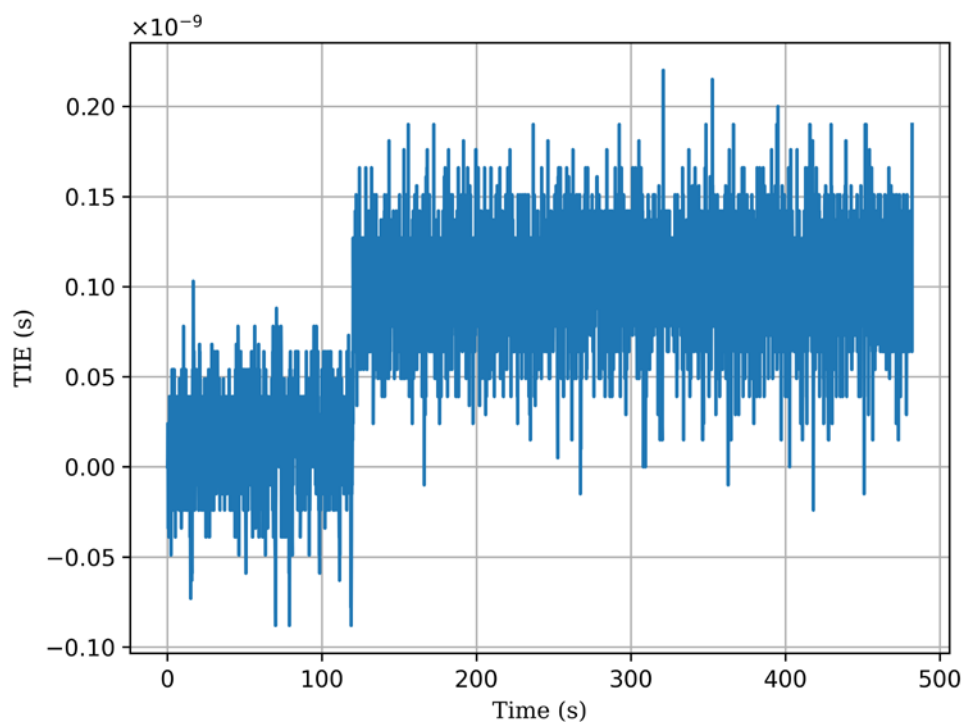


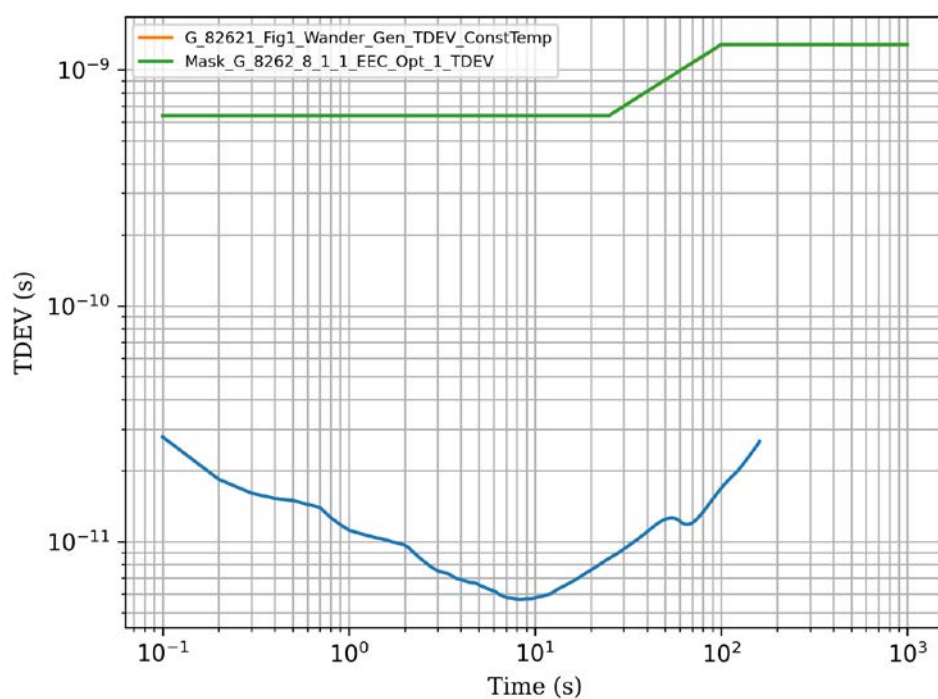
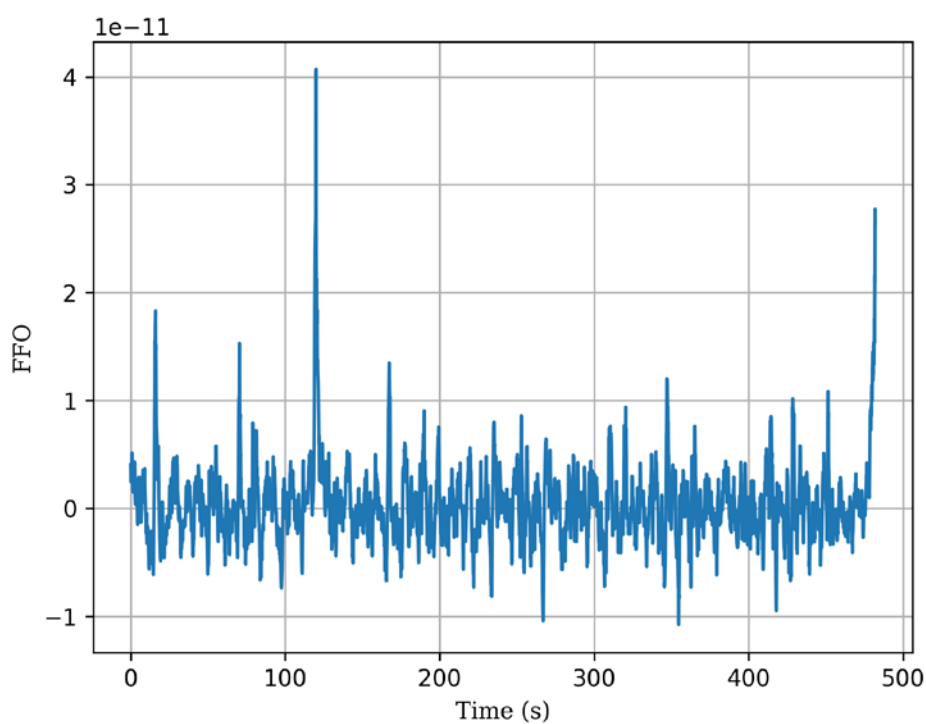
10.3 Phase Response to Input Signal Interruptions – G8262_EEC2





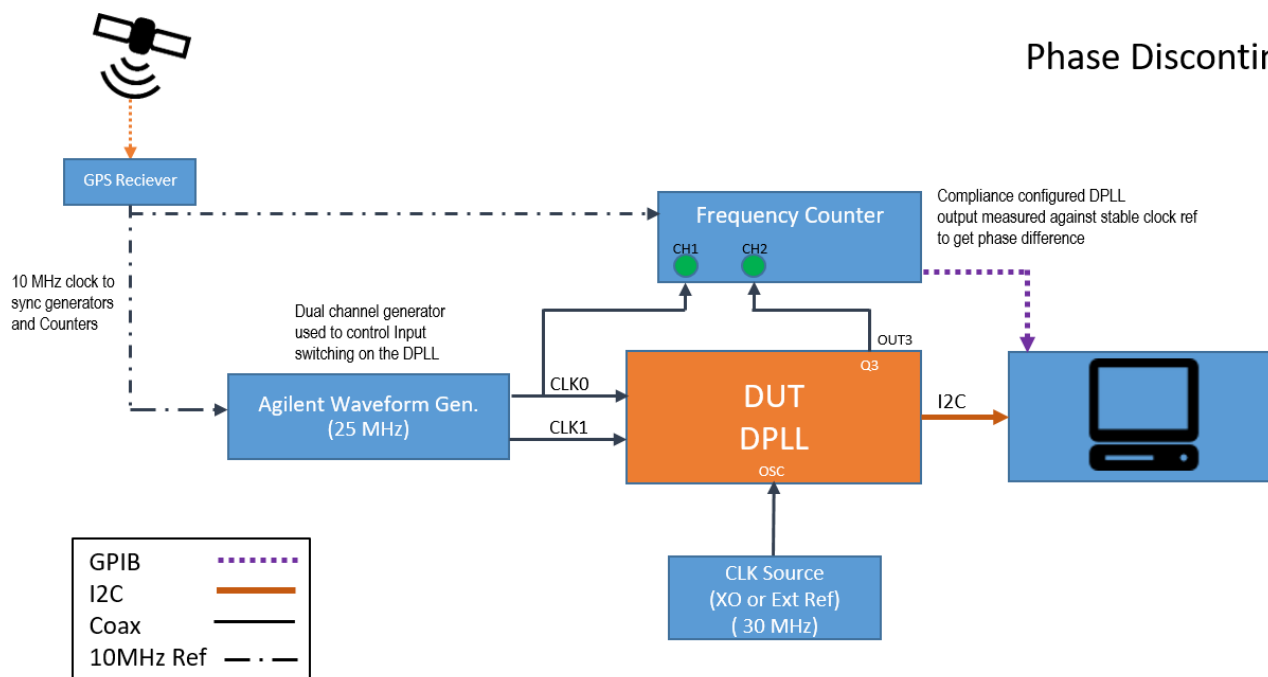
10.4 Phase Response to Input Signal Interruptions – G8262_eEEC1_3Hz





11. (Phase) Transient Response – Phase Discontinuity

Phase Discontinuity

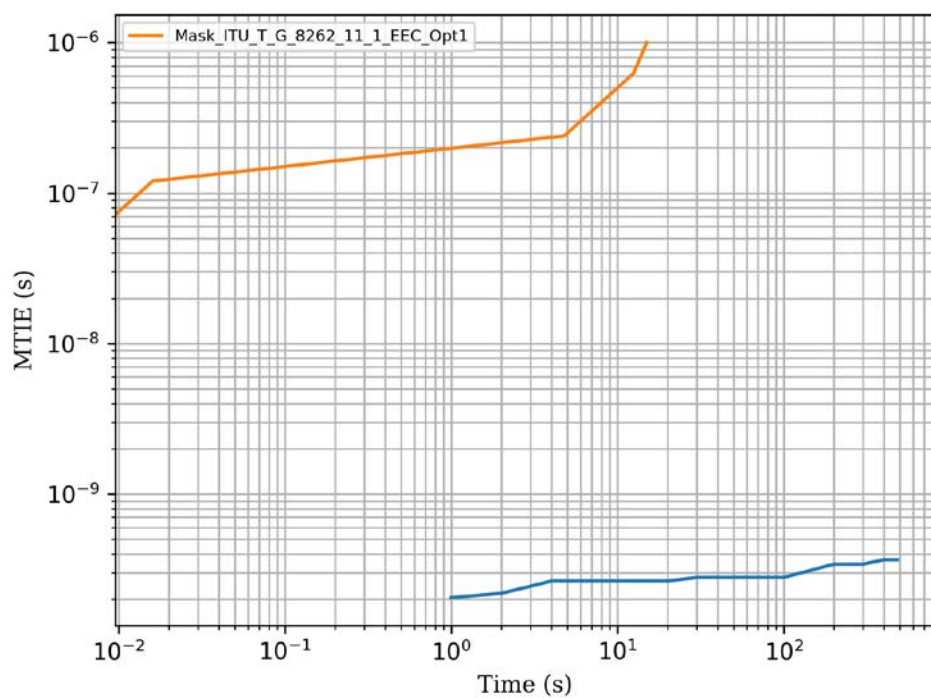
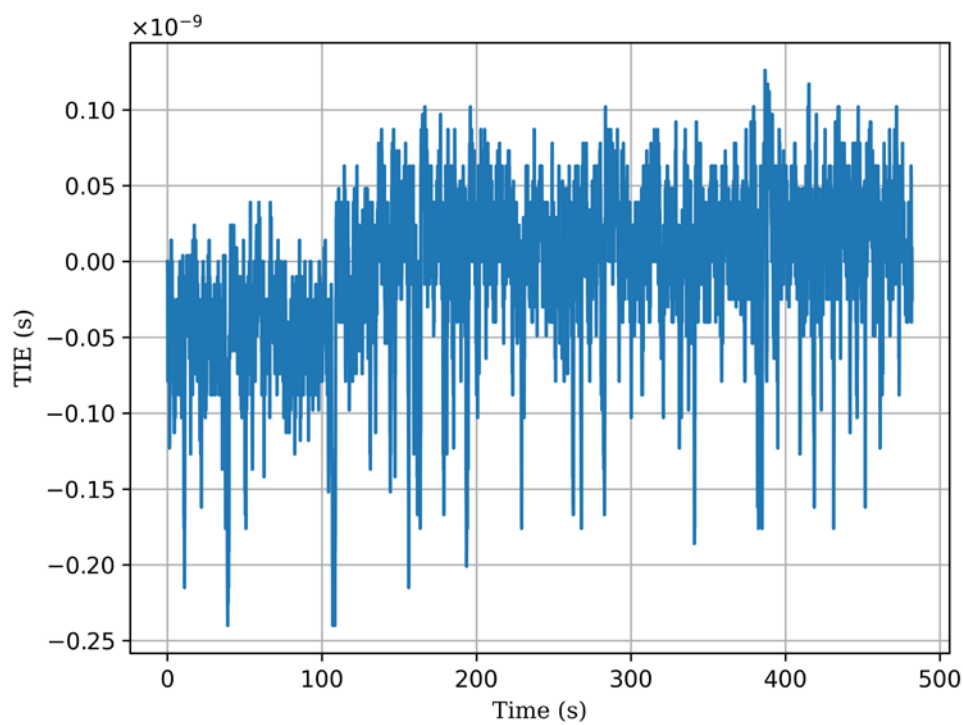


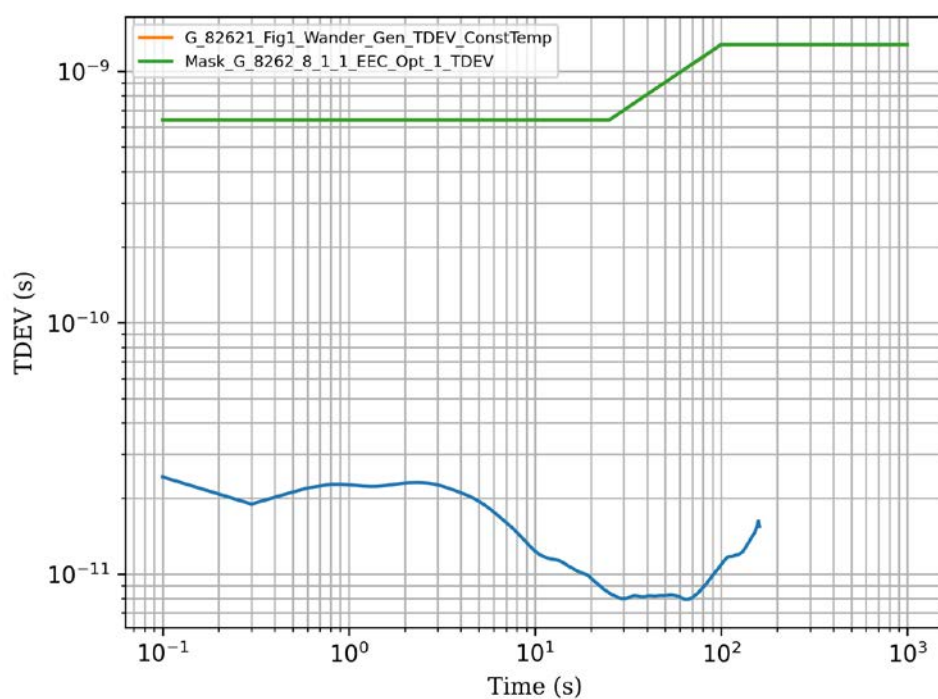
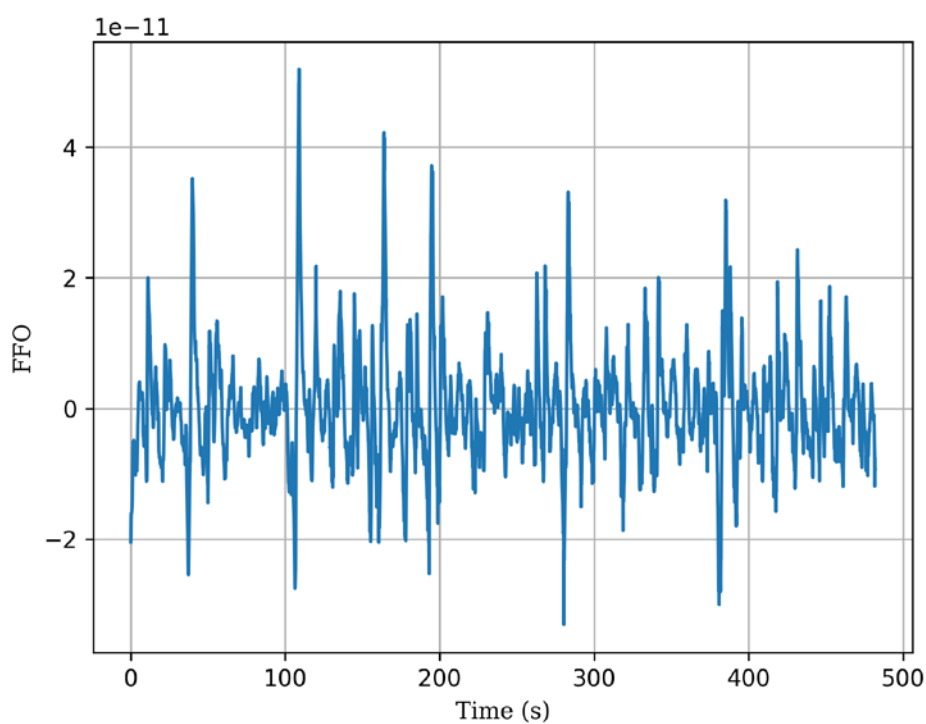
Phase discontinuity requirement reflects the performance of the DUT in cases when there are internal disturbances within the equipment clock.

The test was carried out by providing reference clock inputs on CLK0 and CLK1 from the Agilent waveform generator which are 180° out of phase from each other. The PLL is locked to the clock signal from CLK0 for a given period of time before producing a phase transient by turning off the signal to CLK0 from the waveform generator while the signal at CLK1 is simultaneously available to the DUT. The DPLL will try to lock to the reference signal on CLK1. The output from the DUT is made available on the OUT_3 output and the phase time error is captured using the frequency counter. The results of the given transient are plotted against the mentioned standard profiles.

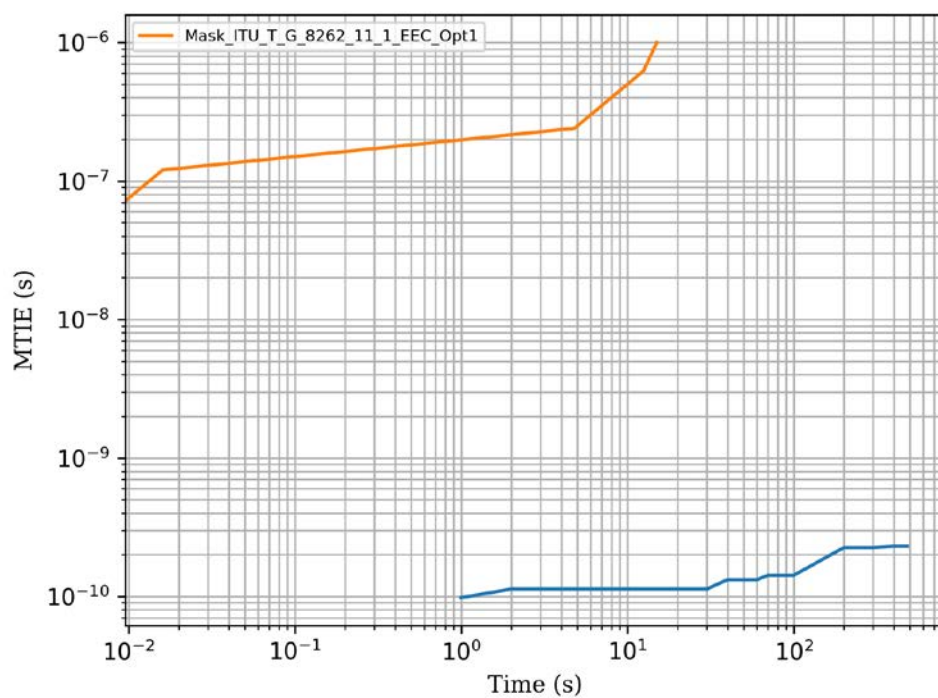
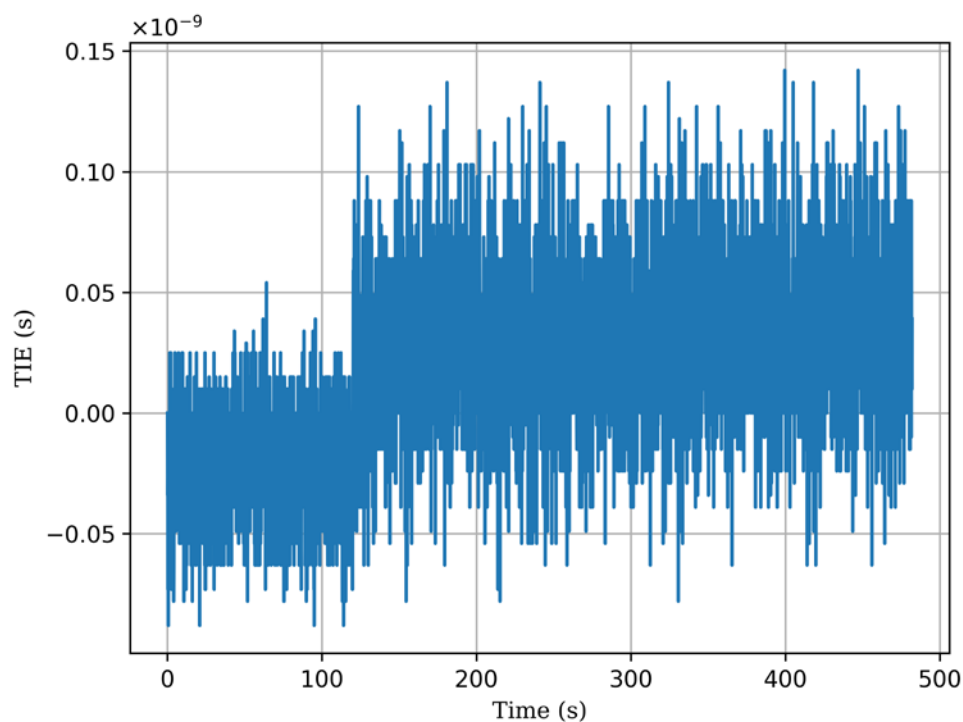
Hitless switching is enabled during this test.

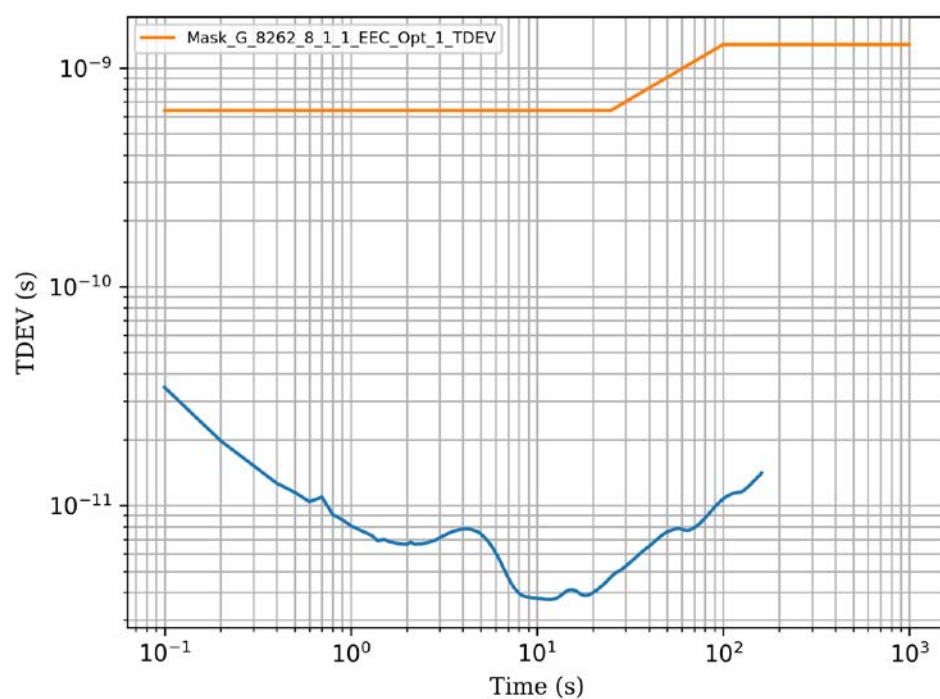
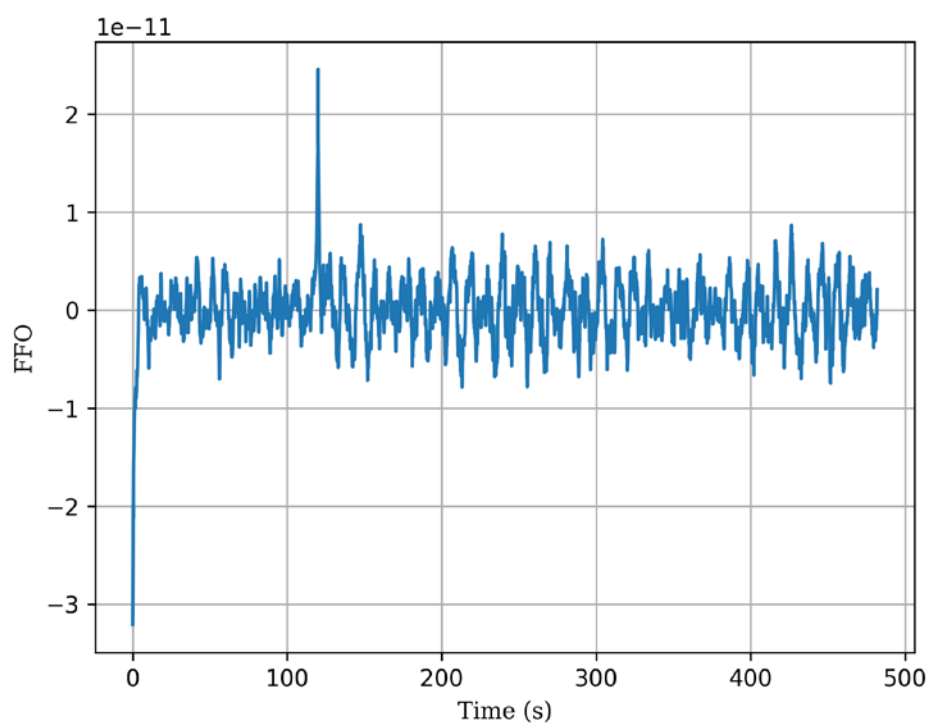
11.1 Phase Discontinuity – G8262_EEC1_1Hz



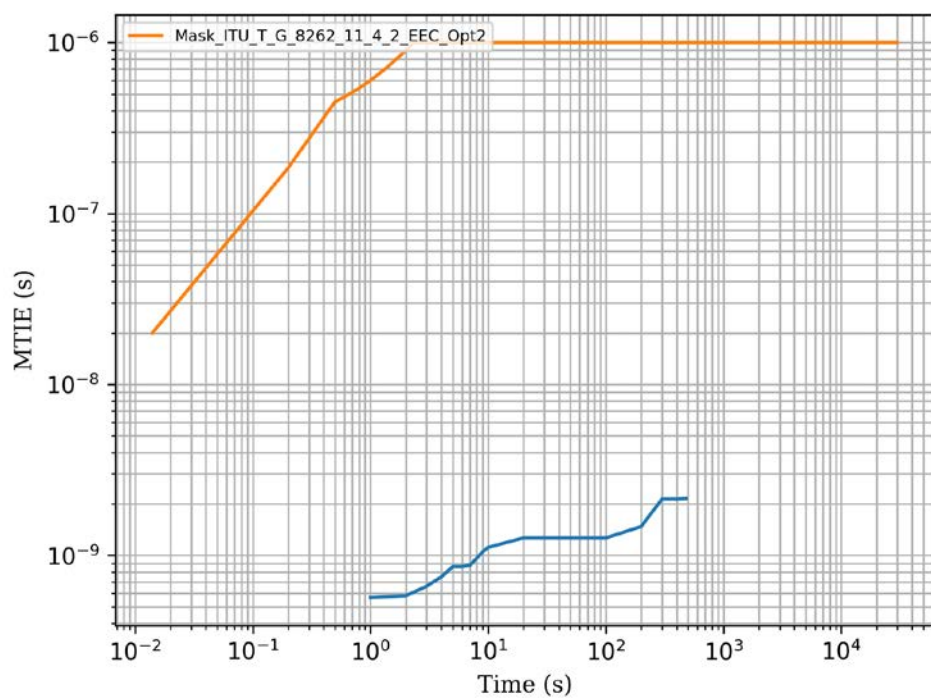
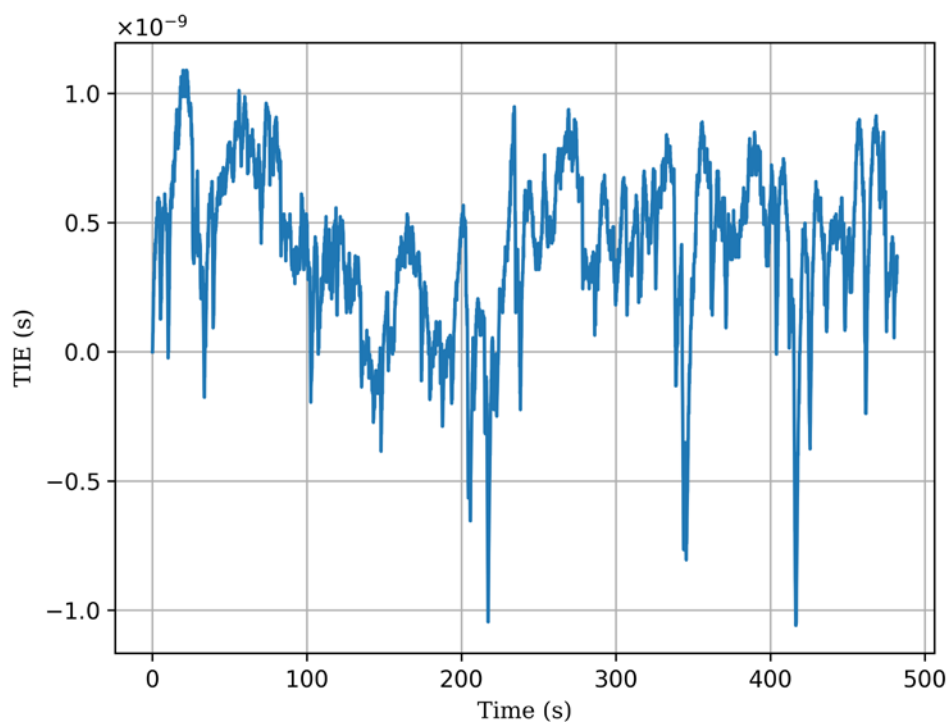


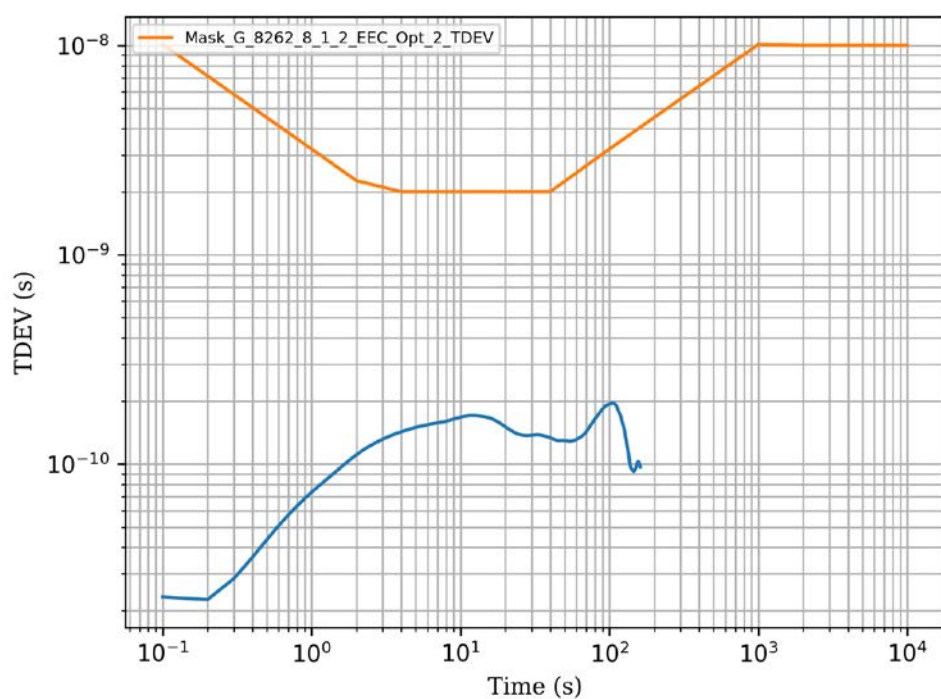
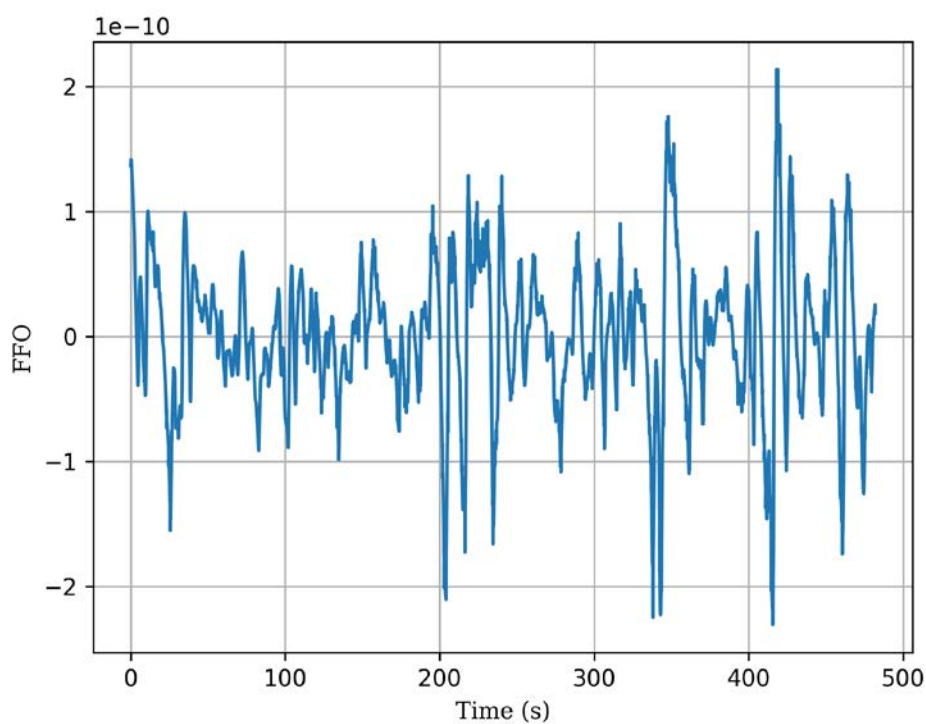
11.2 Phase Discontinuity – G8262_EEC1_10Hz



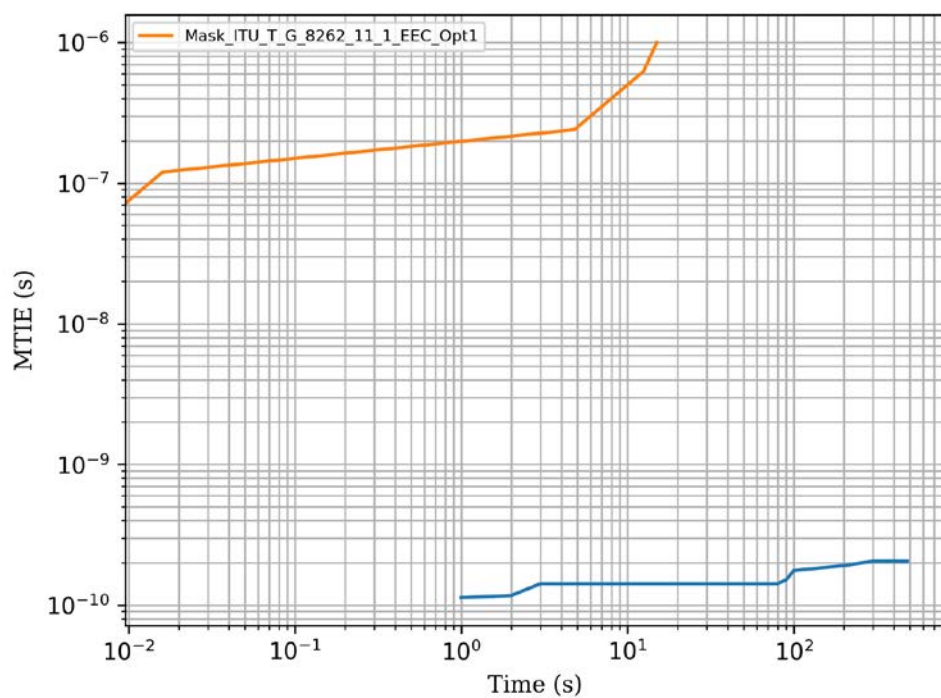
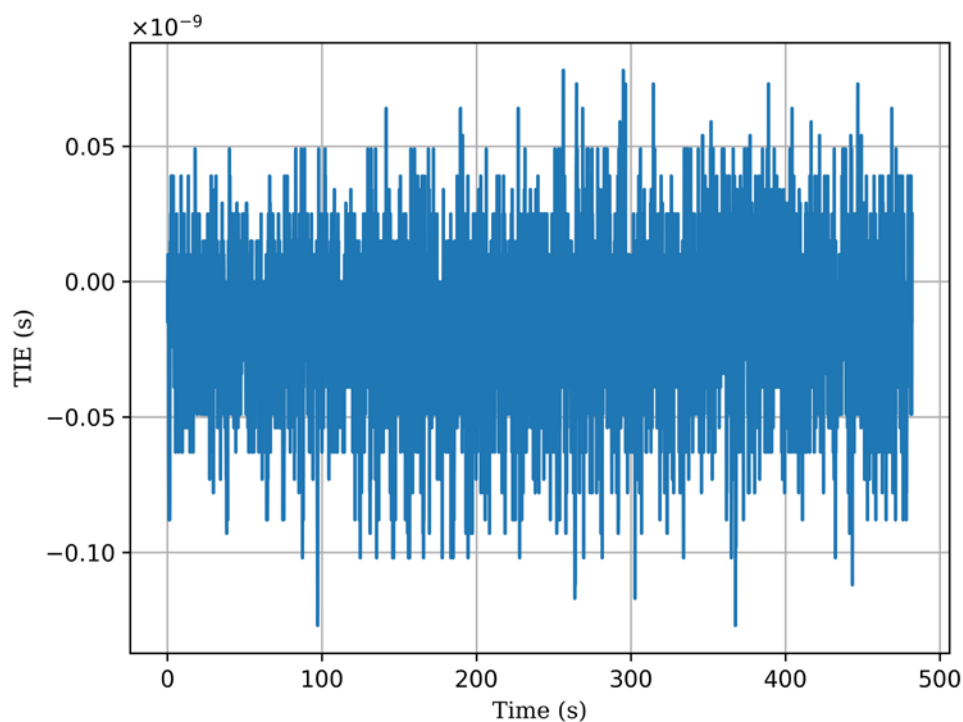


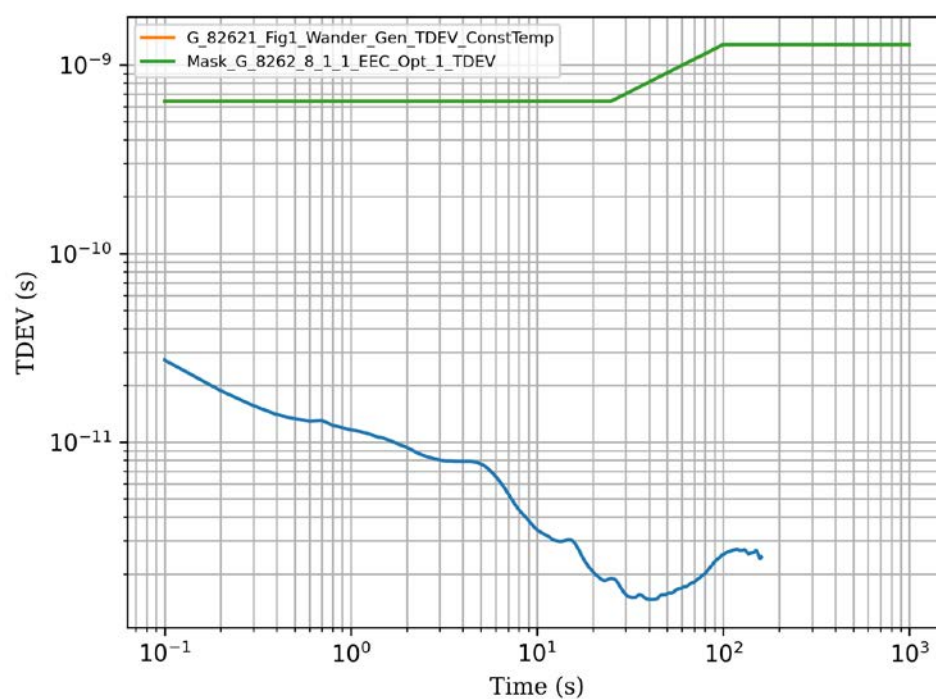
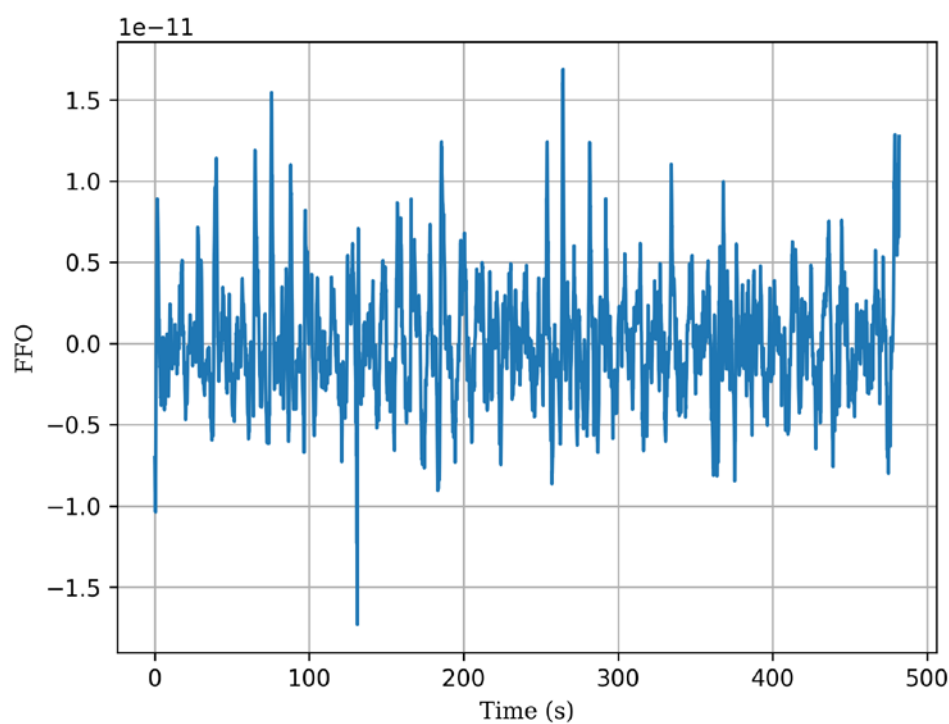
11.3 Phase Discontinuity – G8262_EEC2





11.4 Phase Discontinuity – G8262_eEEEC1_3Hz





12. Interfaces

The ClockMatrix™ PLL can lock to virtually any frequency from 0.5Hz to 1GHz and produce virtually any output frequency from 0.5Hz to 1GHz, supporting a wide range of synchronization input and output interfaces.

13. Revision History

Revision	Date	Description
1.0	May 5, 2021	Initial release.

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