# HS-1840AxH

Combined Neutron and TID Testing of the HS-1840AxH Radiation Hardened 16-Channel Multiplexer

## Introduction

This report summarizes results of combined 1MeV equivalent neutron testing and High Dose Rate (HDR) Total Ionizing Dose (TID) testing of the HS-1840AxH radiation hardened 16-channel multiplexers. The test was conducted to determine the sensitivity of the parts to displacement damage (DD) and total dose effects caused by neutron or proton environments. Neutron fluences ranged from $5\times10^{11}$n/cm$^2$ to $1\times10^{13}$n/cm$^2$. HDR testing was completed through 100krad(Si).

## Product Description

The HS-1840ARH and HS-1840AEH are radiation hardened, monolithic 16-channel multiplexers constructed with the Renesas Rad-Hard Silicon Gate, bonded wafer, Dielectric Isolation process. They provide a high input impedance to the analog source if device power fails (open), or the analog signal voltage inadvertently exceeds the supply by up to ±35V, regardless of whether the device is powered on or off. Excellent for use in redundant applications, because the secondary device can be operated in a standby unpowered mode affording no additional power drain. More significantly, a high impedance exists between the active and inactive devices preventing any interaction.

One of sixteen channel selections is controlled by a 4-bit binary address plus an Enable-Inhibit input that conveniently controls the ON/OFF operation of several multiplexers in a system. All inputs have electrostatic discharge protection. The HS-1840ARH, HS-1840AEH are processed and screened in full compliance with MIL-PRF-38535 and QML standards. The devices are available in a 28-lead SBDIP and a 28-lead ceramic flatpack, which is shown in Figure 1. *Note:* For testing purposes, the 28-lead flatpack was used.

(28 ld Flatpack) CDFP3-F28

Top View

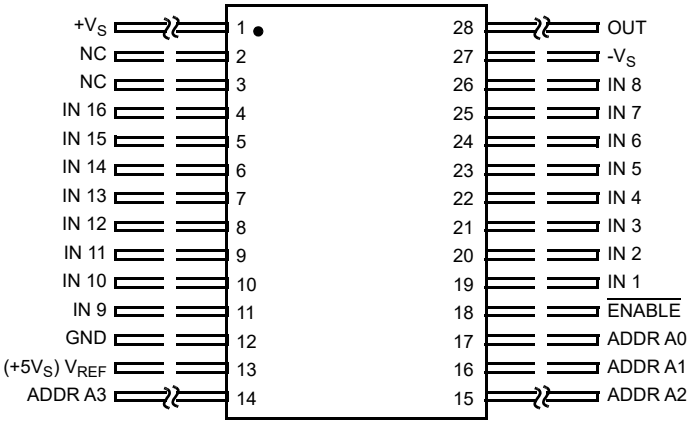


**Figure 1. HS-1840AxH Package and Pinout**

# Contents

# 1. Test Description

## 1.1 Irradiation Facility

Neutron fluence irradiations were performed on the test samples on January 14, 2022, at the University of Massachusetts, Lowell (UMASS Lowell) fast neutron irradiator per Mil-STD-883G, Method 1017.2, with each part unpowered during irradiation. The target irradiation levels were $5\times10^{11}$n/cm$^2$, $2\times10^{12}$n/cm$^2$, and $1\times10^{13}$n/cm$^2$. As neutron irradiation activates many of the heavier elements found in a packaged integrated circuit, the parts exposed at the higher neutron levels required (as expected) some cooldown time before being shipped back to Renesas (Palm Bay, FL) for electrical testing.

HDR testing was performed on January 25, 2022, using a Gammacell 220 gamma-ray irradiator located in the Renesas Palm Bay, Florida facility. The HDR irradiations were performed at 77rad(Si)/s per MIL-STD-883 Method 1019.7. A PbAl box was used to shield the test fixture and devices under test against low energy, secondary gamma radiation.

## 1.2 Test Fixturing

No formal irradiation test fixturing is involved for the neutron testing, as these DD tests are bag tests in the sense that the parts are irradiated with all leads unbiased.

Figure 2 shows the configuration used for the TID testing.

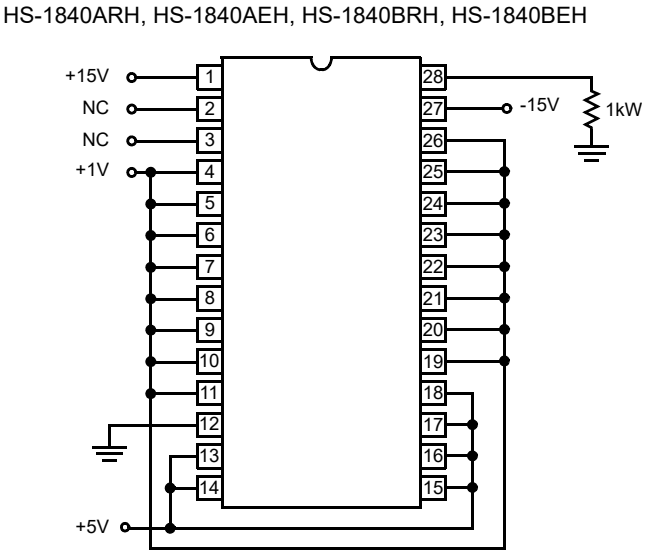


**Figure 2. Irradiation Bias configuration for the HS-1840**

## 1.3 Radiation Dosimetry

Table 1 shows dosimetry from UMASS Lowell indicating the total accumulated gamma dose and actual neutron fluence exposure levels for each set of samples.

**Table 1. HS-1840AxH Neutron Fluence Dosimetry Data**

| Irradiation | Requested Fluence ($n/cm^2$) | Reactor Power (kW) | Time (s) | Fluence Rate ($n/cm^2$-s)[1][2] | Gamma Dose (rad(Si))[3] | Measured Fluence ($n/cm^2$)[4] |
|---|---|---|---|---|---|---|
| CRF#62106-A | 5.00E+11 | 10 | 617 | 8.10E+08 | 70 | 5.38E+11 |
| CRF#62106-B | 2.00E+12 | 100 | 247 | 8.10E+09 | 281 | 2.05E+12 |
| CRF#62106-C | 1.00E+13 | 1000 | 123 | 8.10E+10 | 1401 | 1.14E+13 |

1. Dosimetry method: ASTM E-265.
2. The neutron fluence rate is determined from *Initial Testing of the New Ex-Core Fast Neutron Irradiator at UMass Lowell (6/18/02)*. Validated on 6/07/2011 under the Trident II D5LE neutron facility study by Navy Crane.
3. Based on reactor power at 1000kW, the gamma dose is 41krad(Si)/hr ±5.3% as mapped by TLD-based dosimetry
4. Validated by S-32 flux monitors.

## 1.4 Characterization Equipment and Procedures

Electrical testing for the neutron test was performed before and after neutron irradiation using the Renesas production automated test equipment (ATE). All electrical testing was performed at room temperature.

All electrical testing for the HDR test was performed outside the irradiator using the ATE with datalogging at each downpoint. Downpoint electrical testing was performed at room temperature.

## 1.5 Experimental Matrix

Neutron testing proceeded in general accordance with the guidelines of MIL-STD-883 TM 1017. The experimental matrix consisted of five samples to be irradiated at $5\times10^{11}n/cm^2$, five to be irradiated at $2\times10^{12}n/cm^2$, and five to be irradiated at $1\times10^{13}n/cm^2$. The actual levels achieved, which are shown in Table 2, were $5.38\times10^{11}n/cm^2$, $2.05\times10^{12}n/cm^2$, and $1.14\times10^{13}n/cm^2$. Following neutron testing, each set of samples underwent HDR TID testing. Each set of samples was irradiated under bias to 100krad(Si) with downpoints at 30krad(Si), 50krad(Si), and 100krad(Si). Three control units were used.

The 15 HS-1840AxH samples were drawn from Lot G4T0LEH. Samples were packaged in the standard hermetic 28-lead ceramic flatpack (CDFP). Samples were processed through burn-in before irradiation and were screened to the SMD limits at room, low, and high temperatures before the start of neutron testing.

# 2. Results

Combined neutron and high dose rate total ionizing dose testing of the HS-1840AxH is complete and the results are reported in the balance of this report. It should be understood when interpreting the data that each neutron irradiation was performed on a different set of samples; the damage from neutron testing was not cumulative. Following neutron testing, each set of samples underwent HDR TID testing in which the damage was cumulative.

## 2.1 Attributes Data

**Table 2. HS-1840AxH Attributes Data**

| 1MeV Fluence, (n/cm$^2$) | | TID (krad(Si)) | Sample Size | Pass[1] | Fail | Notes |
|---|---|---|---|---|---|---|
| Planned | Actual | | | | | |
| $5\times10^{11}$ | $5.38\times10^{11}$ | 30 | 5 | 5 | 0 | All passed |
| | | 50 | | | | |
| | | 100 | | | | |
| $2\times10^{12}$ | $2.05\times10^{12}$ | 30 | 5 | 5 | 0 | All passed |
| | | 50 | | | | |
| | | 100 | | | | |
| $1\times10^{13}$ | $1.14\times10^{13}$ | 30 | 5 | 5 | 0 | All passed |
| | | 50 | | | | |
| | | 100 | | | | |

1. A pass indicates a sample that passes all SMD limits.

## 2.2 Variables Data

The plots in Figure 3 through Figure 16 show data for key parameters before and after irradiation to each level. The plots show the mean of each parameter as a function of neutron and total dose irradiation. Each set of samples was irradiated to a different neutron fluence and is plotted as a distinct line. Each line only has markers at the radiation levels to which the corresponding set of samples was exposed. For example, the line representing a parameter of the set of samples irradiated to $5\times10^{11}$n/cm$^2$ has a marker at $5\times10^{11}$n/cm$^2$, but not at $2\times10^{12}$n/cm$^2$ or $1\times10^{13}$n/cm$^2$. All lines have makers at the pre-irradiation level and the total dose levels of 30krad(Si), 50krad(Si), and 100krad(Si).

For the switch measurements, the ATE program recorded the measurements for each of the 16 switches (such as leakage current), however, it was chosen to plot the average of the measurements. Therefore, if the graph and captions state that it is the average, the average of the 16 channels is plotted. Similarly, for the address and enable pins measurements, the average of A0-A4 and enable is plotted when the graph and captions state that it is the average. The plots also include error bars at each downpoint, representing the minimum and maximum measured values of the samples, although in some plots the error bars might not be visible because of their values compared to the scale of the graph. The applicable electrical limits taken from the SMD are also shown.

All samples passed the post-irradiation SMD limits after all three neutron exposures up to and including $1.14\times10^{13}$n/cm$^2$ and after HDR irradiation through 100krad(Si).

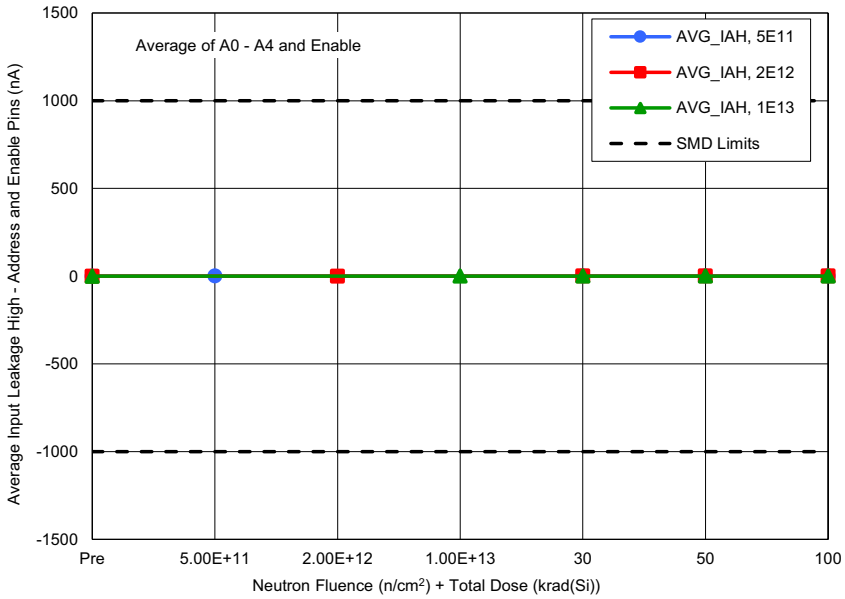


**Figure 3. HS-1840AxH average input leakage current high, address or enable pins ($I_{AH}$) at V+ = +15V, V- = -15V, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all pins. The SMD limits are -1000nA minimum and 1000nA maximum.**

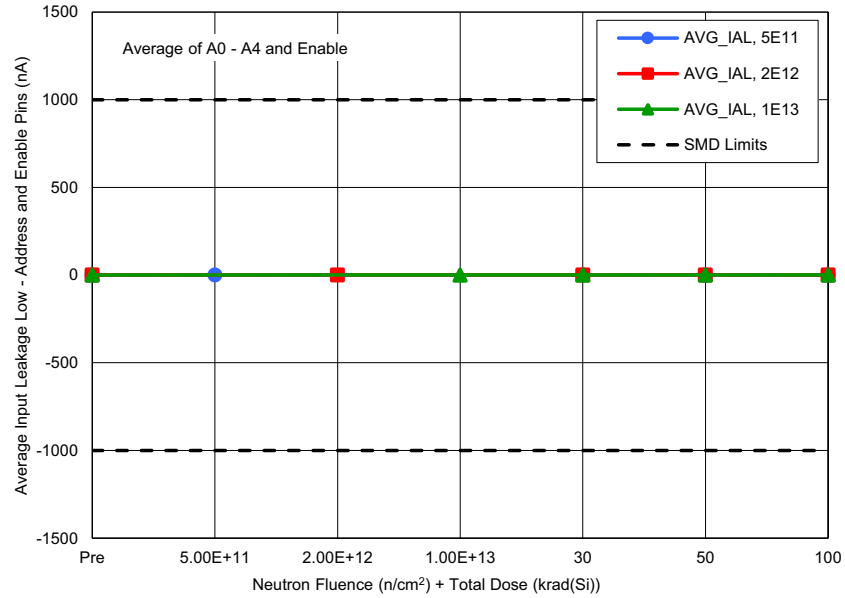


**Figure 4. HS-1840AxH average input leakage current low, address or enable pins ($I_{AL}$) at V+ = +15V, V- = -15V, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all pins. The SMD limits are -1000nA minimum and 1000nA maximum.**

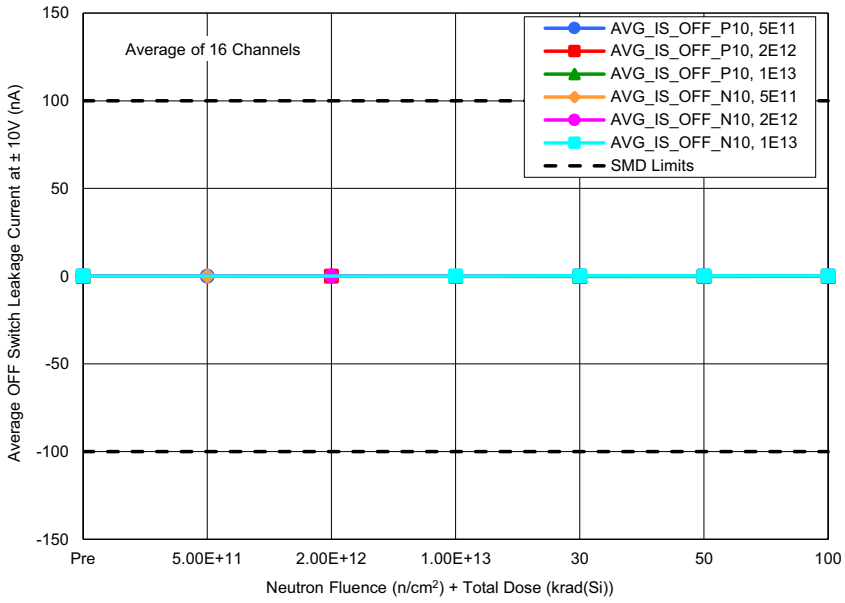


**Figure 5. HS-1840AxH average leakage current into the source terminal of an off switch ($I_{S(OFF)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The SMD limits are -100nA minimum and 100nA maximum.**

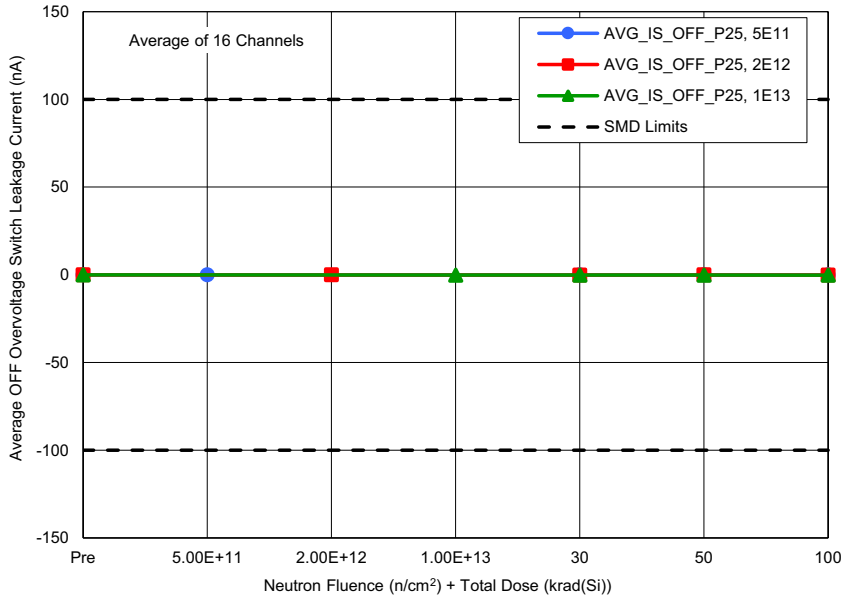


**Figure 6. HS-1840AxH average leakage current into the source terminal of an off switch with power off ($I_{S(OFF)power\ off}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The SMD limits are -100nA minimum and 100nA maximum.**

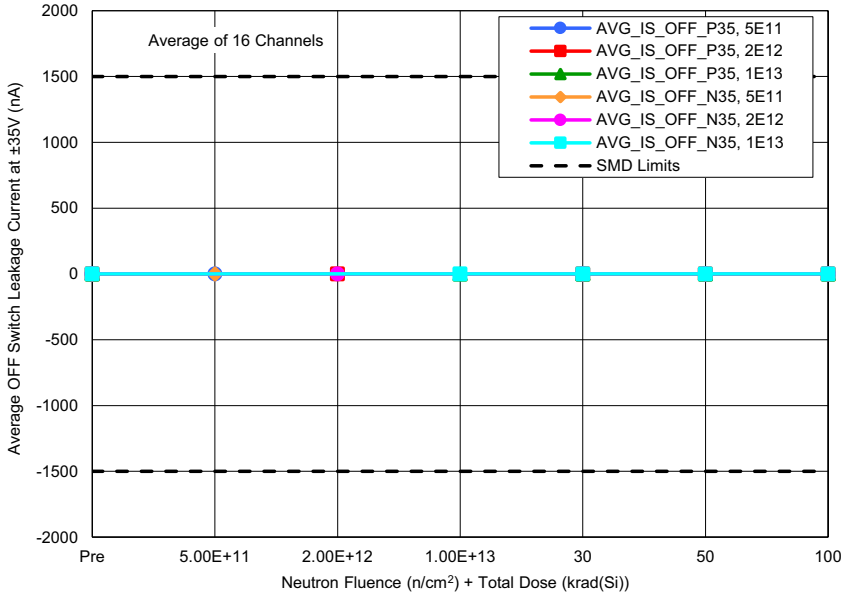


**Figure 7. HS-1840AxH average leakage current into the source terminal of an off switch with overvoltage applied ($I_{S(OFF)overvoltage}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The SMD limits are -1500nA minimum and 1500nA maximum.**

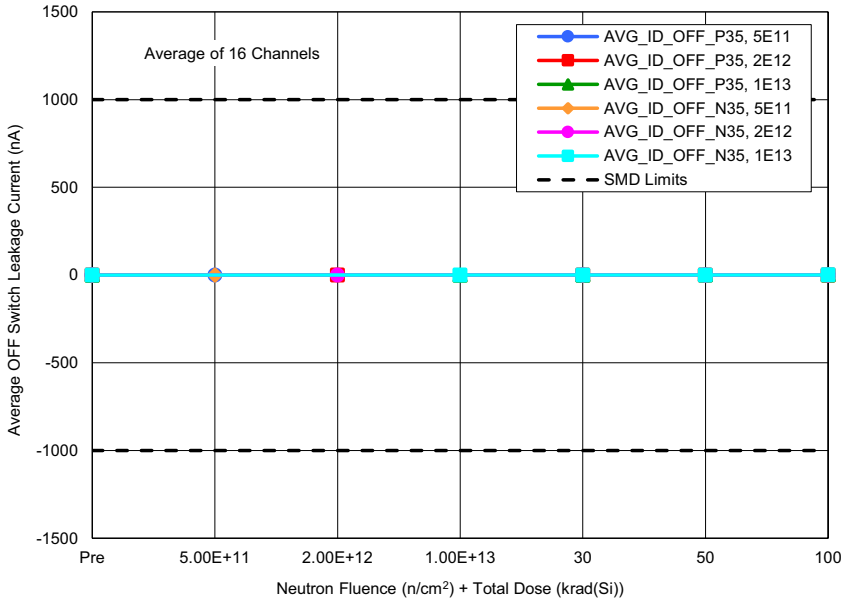


**Figure 8. HS-1840AxH average leakage current into the drain terminal of an off switch with overvoltage applied ($I_{D(OFF)overvoltage}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The SMD limits are -1000nA minimum and 1000nA maximum.**

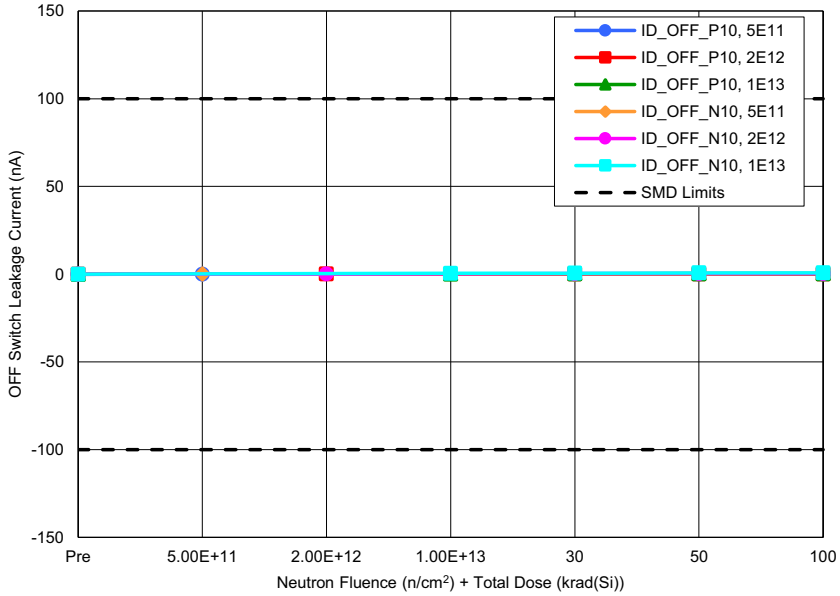


**Figure 9. HS-1840AxH leakage current into the drain terminal of an off switch following ($I_{D(OFF)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -100nA minimum and 100nA maximum.**

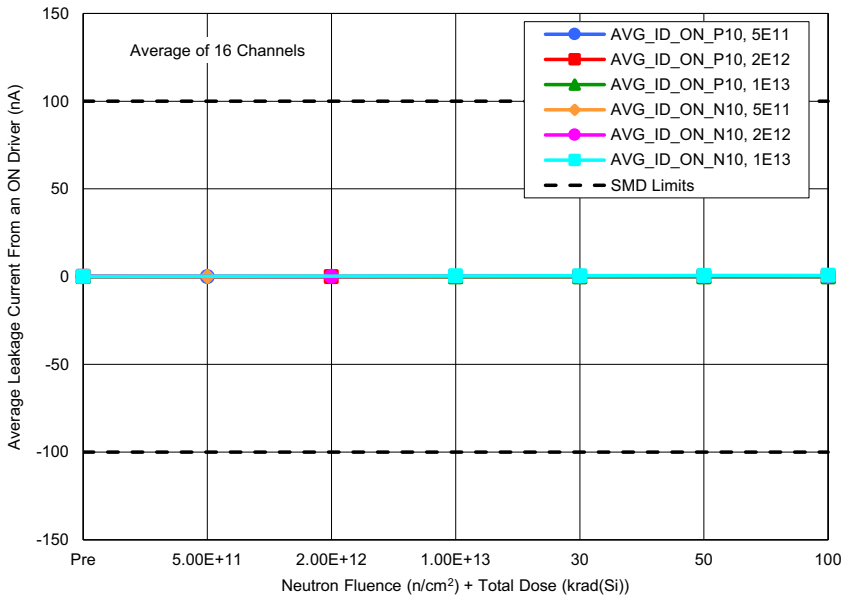


**Figure 10. HS-1840AxH average leakage current from an on driver into the switch (drain and source) ($I_{D(ON)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The SMD limits are -100nA minimum and 100nA maximum.**

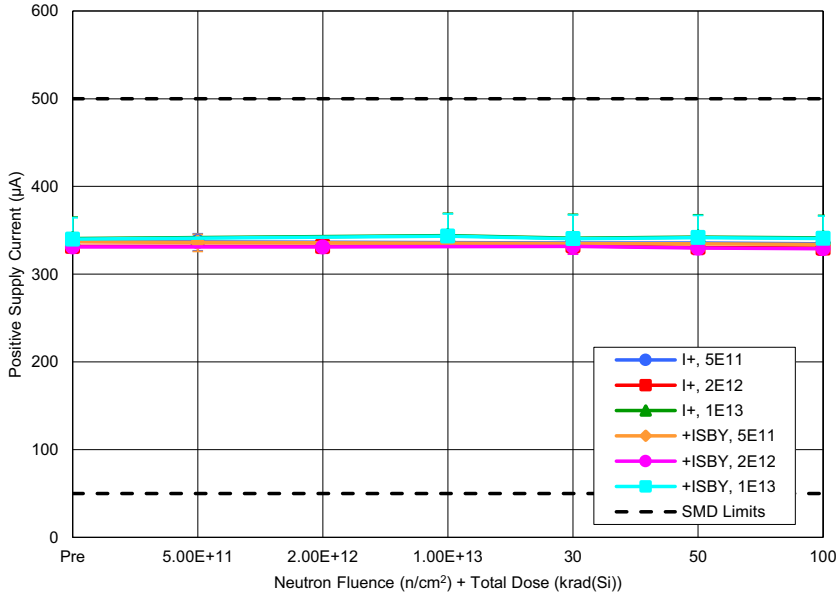


**Figure 11. HS-1840AxH positive supply current (I+) and positive standby supply current (+$I_{SBY}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 50µA minimum and 500µA maximum.**

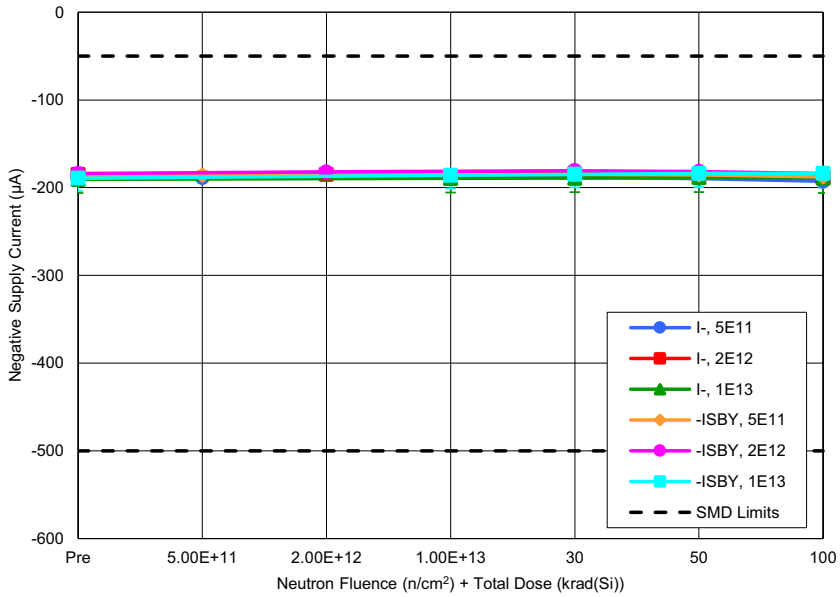


**Figure 12. HS-1840AxH negative supply current (I-) and negative standby supply current (-$I_{SBY}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -500µA minimum and -50µA maximum.**

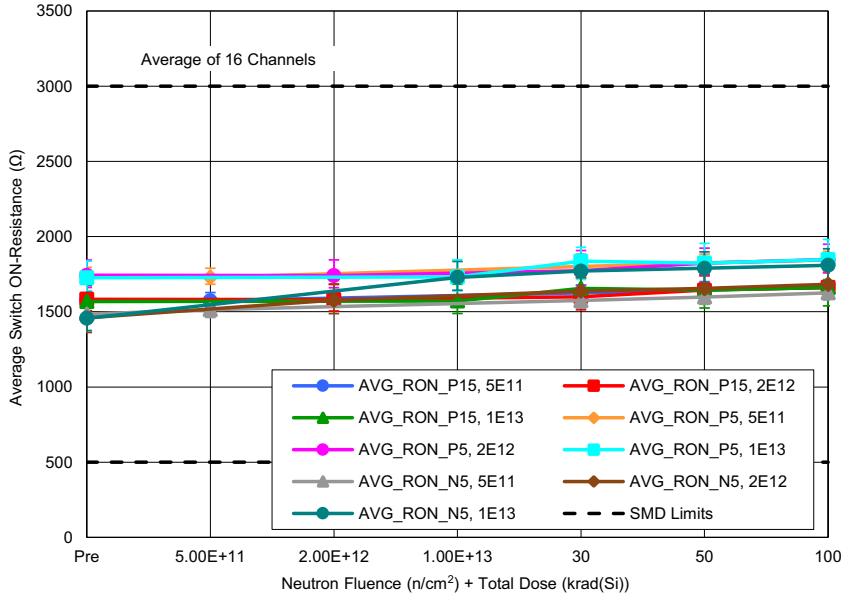


**Figure 13. HS-1840AxH average switch on resistance ($r_{DS(ON)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The SMD limits are 500Ω minimum and 3000Ω maximum.**

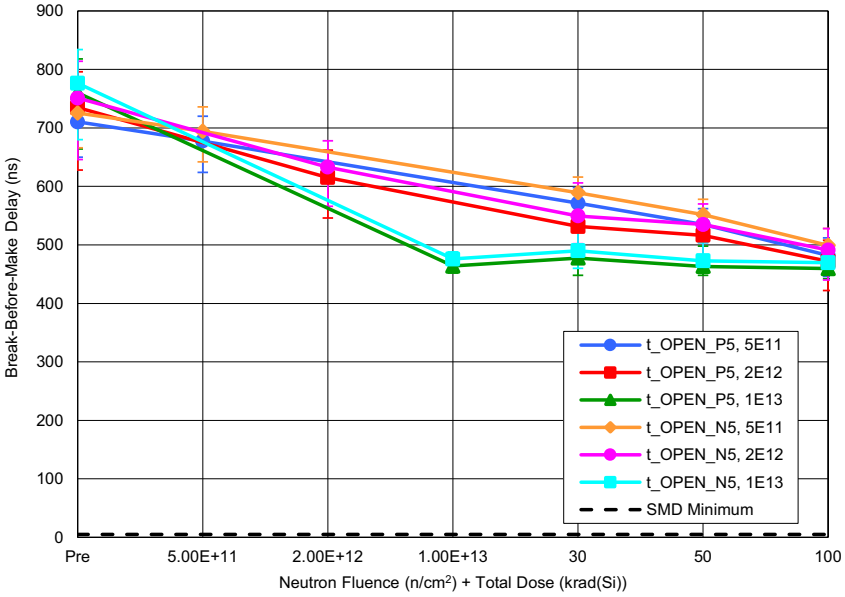


**Figure 14. HS-1840AxH break-before-make time delay ($t_D$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 5ns minimum.**

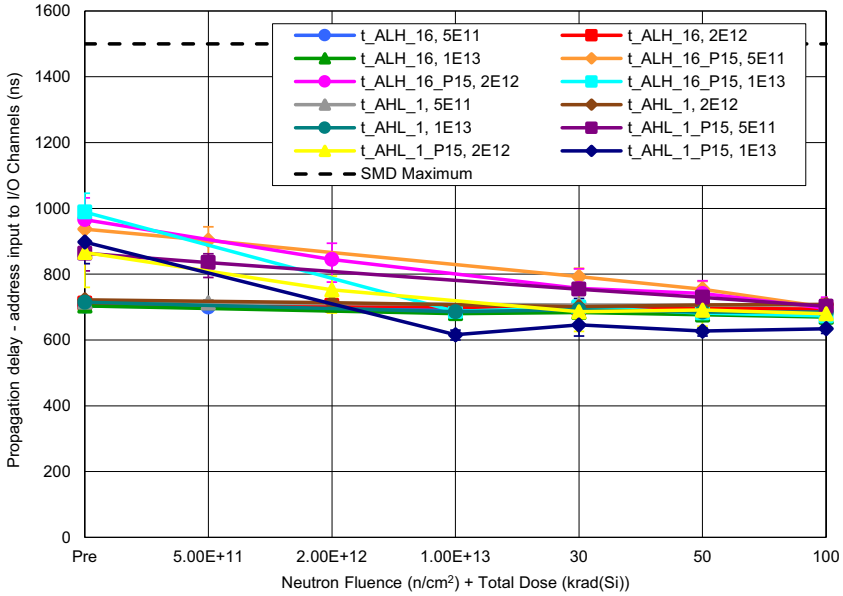


**Figure 15. HS-1840AxH propagation delay time, address input to I/O channels ($t_{on(A)}$, $t_{OFF(A)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 1500ns maximum.**

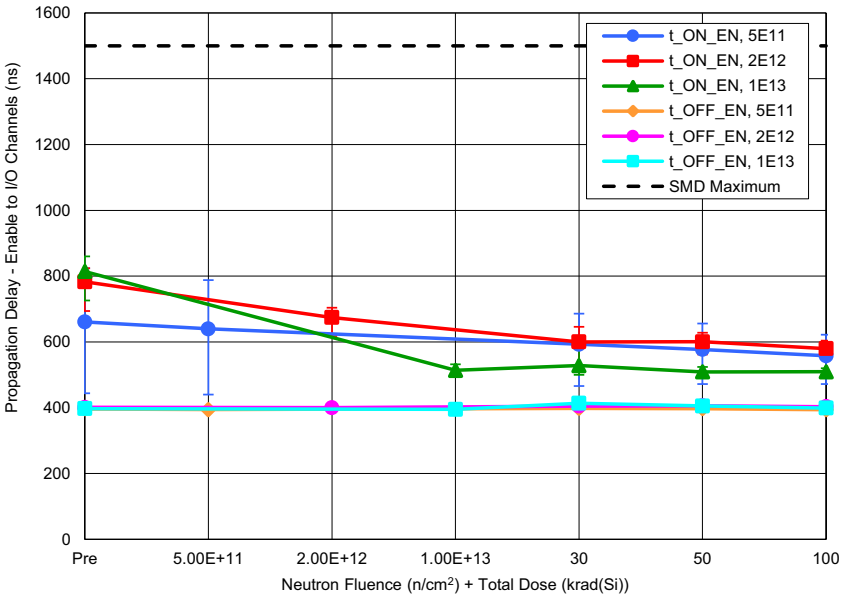


**Figure 16. HS-1840AxH propagation delay time, enable to I/O channels ($t_{ON(EN)}$, $t_{OFF(EN)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 1500ns maximum.**

# 3. Discussion and Conclusion

This report summarizes results of combined 1MeV equivalent neutron testing and High Dose Rate (HDR) Total Ionizing Dose (TID) testing of the HS-1840AxH radiation hardened 16-channel multiplexers. Parts were tested at actual fluences of $5.4\times10^{11}$n/cm$^2$, $2.1\times10^{12}$n/cm$^2$ and $1.1\times10^{13}$n/cm$^2$. Following neutron irradiation and testing, each set of samples underwent HDR TID testing. Each set of samples was irradiated under bias to 100krad(Si) with downpoints at 30krad(Si), 50krad(Si), and 100krad(Si). The results of key parameters before and after irradiation to each level are plotted in Figure 3 through Figure 16. The plots show the mean of each parameter as a function of neutron and total dose irradiation, with error bars that represent the minimum and maximum measured values. The figures also show the applicable electrical limits taken from the SMD.

All samples passed the post-irradiation SMD limits after all three neutron exposures up to and including $1.14\times10^{13}$n/cm$^2$ and after HDR irradiation through 100krad(Si).

# 4. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.01 | May 5, 2025 | Updated Variables Data section.<br>Updated Discussion and Conclusion section. |
| 1.00 | Sep 7, 2022 | Initial release. |

# Appendix

**Table 3. Reported Parameters**

| Fig. | Parameter | Symbol | Test Conditions | Low Limit | High Limit | Unit |
|---|---|---|---|---|---|---|
| 3 | Input leakage current high, address or enable pins | $I_{AH}$ | $V_{AH}$ = 4V, $V_{AL}$ = 0.8V, $V_{EN}$ = 4V and $V_{REF}$ = 5V, all unused inputs = 0V | -1000 | 1000 | nA |
| 4 | Input leakage current low, address or enable pins | $I_{AL}$ | | | | |
| 5 | Leakage current into the source terminal of an off switch | $I_{S(OFF)}$ | $V_S$ = ±10V | -100 | 100 | nA |
| 6 | Leakage current into the source terminal of an off switch with power off | $I_{S(OFF)power\ off}$ | $V_S$ = +25V, $V_A$ = 0V, $V_{EN}$ = 0V, V- = 0V, V+ = 0V, and $V_{REF}$ = 0V, all unused inputs = 0V | -100 | 100 | nA |
| 7 | Leakage current into the source terminal of an off switch with overvoltage applied | $I_{S(OFF)overvoltage}$ | $V_D$ = 0V, all unused inputs = 0V | -1500 | 1500 | nA |
| 8 | Leakage current into the drain terminal of an off switch with overvoltage applied | $I_{D(OFF)overvoltage}$ | $V_D$ = 0V, all unused inputs = 0V | -1000 | 1000 | nA |
| 9 | Leakage current into the drain terminal of an off switch | $I_{D(OFF)}$ | $V_D$ = ±10V, all unused inputs = +10V or -10V | -100 | 100 | nA |
| 10 | Leakage current from an on driver into the switch (drain and source) | $I_{D(ON)}$ | $V_S$ = +10V, $V_D$ = +10V, $V_{EN}$ = 0.8V, all unused inputs = -10V | -100 | 100 | nA |
| 11 | Positive supply current | I+ | $V_A$ = 0V, $V_{EN}$ = 0.8V | 50 | 500 | µA |
| | Positive standby supply current | $+I_{SBY}$ | $V_A$ = 0V, $V_{EN}$ = 4.0V | 50 | 500 | µA |
| 12 | Negative supply current | I- | $V_A$ = 0V, $V_{EN}$ = 0.8V | -500 | -50 | µA |
| | Negative standby supply current | $-I_{SBY}$ | $V_A$ = 0V, $V_{EN}$ = 4.0V | -500 | -50 | µA |
| 13 | Switch on-resistance | $r_{DS(ON)}$ | $V_S$ = V+, $V_{EN}$ = 0.8V, $I_D$ = -1mA | 500 | 3000 | Ω |
| 14 | Break-before-make time delay | $t_D$ | $C_L$ = 50pF, $R_L$ = 1kΩ | 5 | - | ns |
| 15 | Propagation delay time address input to I/O channels | $t_{on(A)}$, $t_{OFF(A)}$ | $C_L$ = 50pF, $R_L$ = 10kΩ | - | 1500 | ns |
| 16 | Propagation delay time enable to I/O channels | $t_{on(EN)}$, $t_{OFF(EN)}$ | $C_L$ = 50pF, $R_L$ = 1kΩ | - | 1500 | ns |

## Related Information

For a full list of related documents, visit our website:

- HS-1840AEH, HS-1840ARH device pages
- MIL-STD-883 test method 1017
- MIL-STD-883 test method 1019

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