ISL70001SRH

Total Dose Testing of the ISL70001SRH Hardened Point-of-Load Regulator

Introduction

This report provides results of a Low Dose Rate (LDR) and High Dose Rate (HDR) total dose test of the ISL70001SRH point-of-load converter. The test was conducted to determine the sensitivity of the part to the total dose environment and to determine if the part is LDR or bias sensitive. The reported results for the base ISL70001SRH apply equally to the ISL70001ASRH and other ISL71001 variants such as the ISL71001SLHM and ISL71001SEHM. These parts vary in packaging technology, SEE ratings, and TID ratings.

Related Information

- MIL-STD-883G test method 1019
- ISL70001SRH datasheet
- DSCC Standard Microcircuit Drawing (SMD) 5962-09225

Contents

© 2021 Renesas Electronics

1. Product Description

The ISL70001SRH is a high-efficiency monolithic synchronous buck regulator with integrated power MOSFET devices, eliminating the need for external MOSFET devices. The part is designed for Point-of-Load (POL) applications and provides a single-chip power management solution for digital ICs such as processors and field-programmable gate arrays. The ISL70001SRH is designed and rated for the total dose and SEE environments as encountered in space and is manufactured in compliance with MIL-PRF-38535 (QML). The part operates across an input voltage range of 3V to 5.5V and provides a regulated output voltage that is externally adjustable from 0.8V to ~85% of the input voltage. Output load current capacity is 6A for T_J < +145°C. The ISL70001SRH uses peak current-mode control with integrated compensation and switches at a fixed frequency of 1MHz. The high level of integration provided by integrating the power MOSFET devices makes the ISL70001SRH a good choice to power small form factor applications in space systems. A simplified block diagram of the part is shown in Figure 1.

The ISL70001ASRH is a minor revision of the ISL70001SRH. The revision was made to correct a startup issue and the total dose results in this report are considered applicable to this revised part. The ISL70001SEH and ISL70001ASEH are variants that are acceptance tested at both LDR and HDR on a wafer-by-wafer basis and are otherwise identical to the -SRH versions; the present results apply to these parts as well.

The ISL71001SLHM and ISL71001SEHM are versions of the ISL70001SRH that use a 64 Ld Thin Quad Flatpack (EP-TQFP) plastic package. The package features Pb-free materials including molding compounds, die attach material, and NiPdAu-Ag plated termination finish that are RoHS compliant. Renesas' radiation-hardened plastic packaging flow leverages more than 50 years of experience developing radiation hardened and radiation tolerant products for harsh environments. The upfront radiation effects characterization and AEC-Q100 automotive-like qualification flow give customers the confidence to design Renesas radiation-hardened plastic parts into cost-sensitive small satellites for MEO and LEO mission profiles. In addition, the ISL71001SLHM and ISL71001SEHM receive production and lot assurance testing that is similar to the flows outlined by SAE standard AS6294/1 which governs the use of plastic encapsulated microcircuits for space use. These parts also receive RLAT screening in the same way that the ISL70001ASRH and ISL70001SRH do. The radiation-hardened plastic parts use the same die as the base ISL70001SRH and the TID results provided in this report apply equally to all parts. These parts differ in radiation specifications and quality assurance flows.

The ISL70001SRH is implemented in a submicron BiCMOS process optimized for power management applications, with 0.6um minimum ground rules and three layers of interconnect. The process is in volume production under MIL-PRF-38535 certification and is used for a wide range of commercial power management devices.

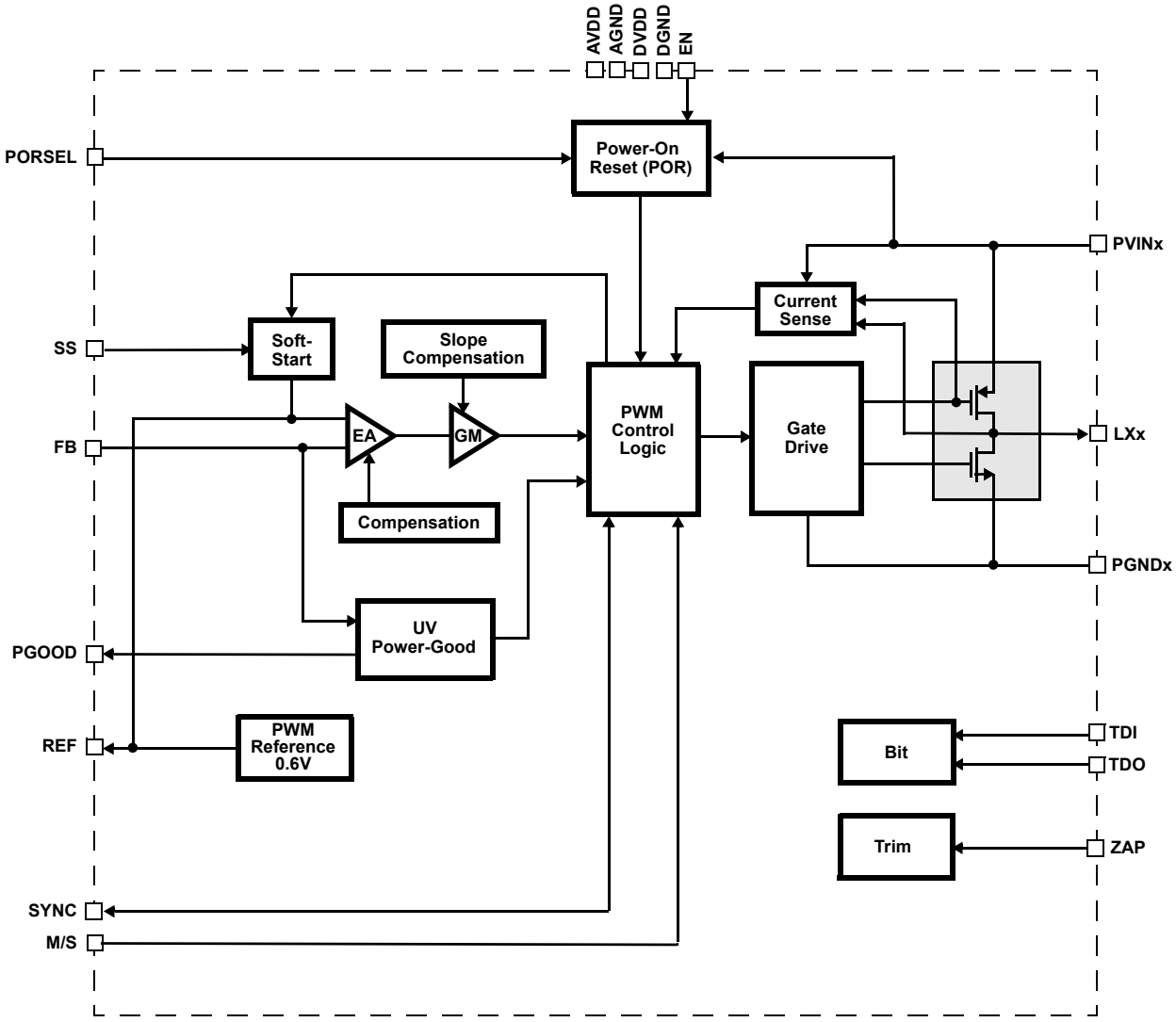


Figure 1. ISL70001SRH Block Diagram

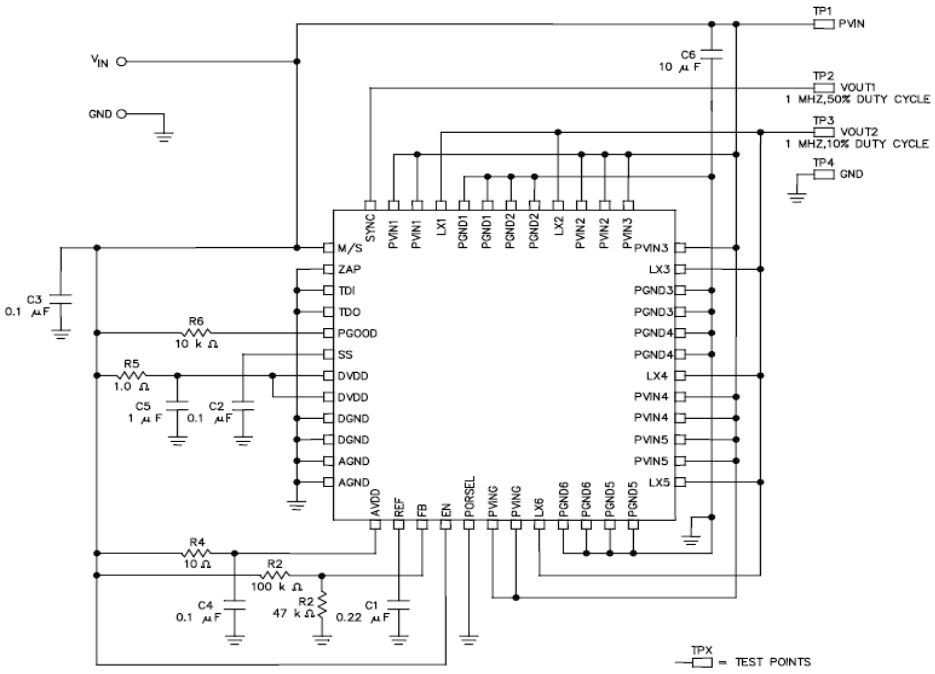
2. Test Description

2.1 Irradiation Facilities

HDR testing was performed using a Gammacell 220 ^{60}Co irradiator located in the Palm Bay, Florida Renesas facility. LDR testing used a J. L. Shepherd and Associates (JLS) LDR ^{60}Co model 484 research irradiator located in the same facility. The HDR irradiations were done at 55rad(Si)/s and the LDR work was performed at 0.010rad(Si)/s, both per MIL-STD-883 Method 1019. Dosimetry for both tests was performed using radiochromic dosimeters and on-site readout equipment. A PbAl box was used to shield the test fixture and devices under test against low energy secondary gamma radiation.

2.2 Test Fixturing

Figure 2 shows the configuration used for biased irradiation. This configuration was used for LDR and HDR testing.



NOTES:

V_{IN} = +5.5 V, -0 V, +0.2 V
I_{CC} = 50 mA per part
TP1 PVIN = V_{IN}
TP2 VOUT1 = 1 MHz 50% duty cycle
TP3 VOUT2 = 1 MHz 10% duty cycle
TP4 = GND

Figure 2. Irradiation Bias Configuration for the ISL70001SRH

2.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using on-site production Automated Test Equipment (ATE) with datalogging at each downpoint. Downpoint electrical testing was performed at room temperature.

2.4 Experimental Matrix

Testing proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of five samples irradiated at HDR with all pins grounded, five samples irradiated at HDR under bias, five samples irradiated at LDR with all pins grounded, and five samples irradiated at LDR under bias. One control unit was used.

Samples of the ISL70001SRH were drawn from preproduction lots I2J43H00YG, wafer V03I6HW, I2K14H00YG, wafer VB3FLJW and I2K14H01YG, wafer AIBWBPW. Samples were packaged in the standard hermetic 48 Ld ceramic quad flatpack (CQFP) production package. Samples were processed through the standard burn-in cycle before irradiation, as required by MIL-STD-883, and were screened to the SMD 5962-09225 limits at room, low and high temperatures before the start of total dose testing.

2.5 Downpoints

Downpoints for the LDR tests were 0krad(Si), 10krad(Si), 25krad(Si), 50krad(Si), 100krad(Si), 125krad(Si), and 150krad(Si). Downpoints for the HDR tests were 0krad(Si), 10krad(Si), 25krad(Si), 50krad(Si), 100krad(Si), and 150krad(Si).

3. Results

3.1 Attributes Data

The high and LDR tests of the ISL70001SRH are complete and showed no reject devices after irradiation to 150krad(Si), screening to the SMD 5962-09225 post-irradiation limits. Table 1 provides attributes data.

Table 1. Attributes Data

Part	Dose Rate (rad(Si)/s)	Bias	Sample Size	Downpoint	Pass [1]	Fail
ISL70001SRH	0.01	Biased	5	Pre-irradiation		
				10krad(Si)	5	0
				25krad(Si)	5	0
				50krad(Si)	5	0
				100krad(Si)	5	0
				125krad(Si)	5	0
				150krad(Si)	5	0
ISL70001SRH	0.01	Grounded	5	Pre-irradiation		
				10krad(Si)	5	0
				25krad(Si)	5	0
				50krad(Si)	5	0
				100krad(Si)	5	0
				125krad(Si)	5	0
				150krad(Si)	5	0
ISL70001SRH	55	Biased	5	Pre-irradiation		
				10krad(Si)	5	0
				25krad(Si)	5	0
				50krad(Si)	5	0
				100krad(Si)	5	0
				150krad(Si)	5	0
ISL70001SRH	55	Grounded	5	Pre-irradiation		
				10krad(Si)	5	0
				25krad(Si)	5	0
				50krad(Si)	5	0
				100krad(Si)	5	0
				150krad(Si)	5	0

1. A pass indicates a sample that passes all SMD 5962-09225 limits.

3.2 Variables Data

The ISL70001SRH is a complex part with some 250 datalogged parameters and plotting all parameters would be a lengthy undertaking. The plots in Figure 3 through Figure 20 show data for 17 key parameters at all downpoints. The plots show the median as a function of total dose for each of the irradiation conditions; we chose to use the median because of the relatively small sample sizes. All parts showed excellent stability over irradiation, with no observed LDR sensitivity. Several parameters such as the bandgap voltage (Figure 4), the error amplifier offset voltage (Figure 16 and Figure 17), and the feedback adjust margin (Figure 19) are informational in nature and are not specified in either the datasheet or the SMD; as a result these parameters do not have formal parametric limits.

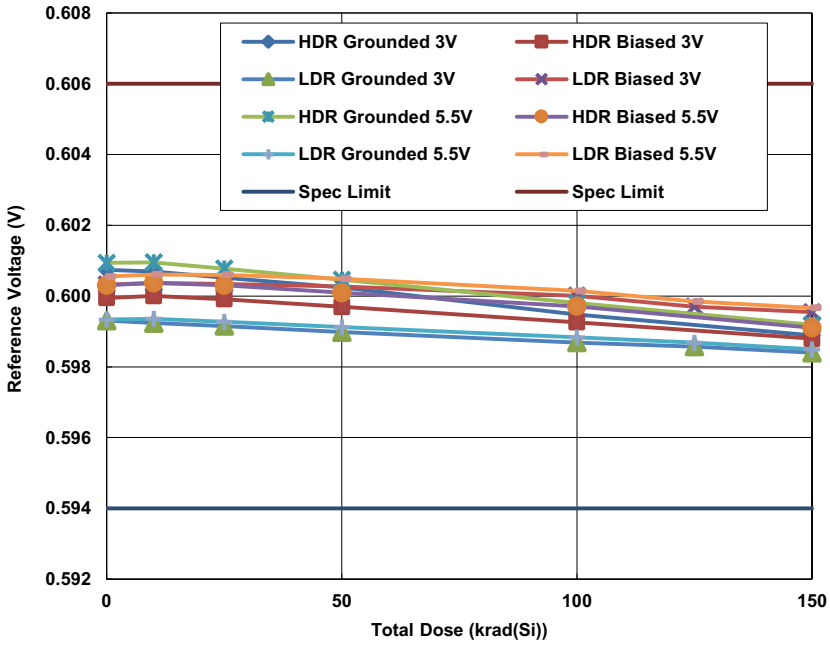


Figure 3. ISL70001SRH reference voltage as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are 0.594 – 0.606V.

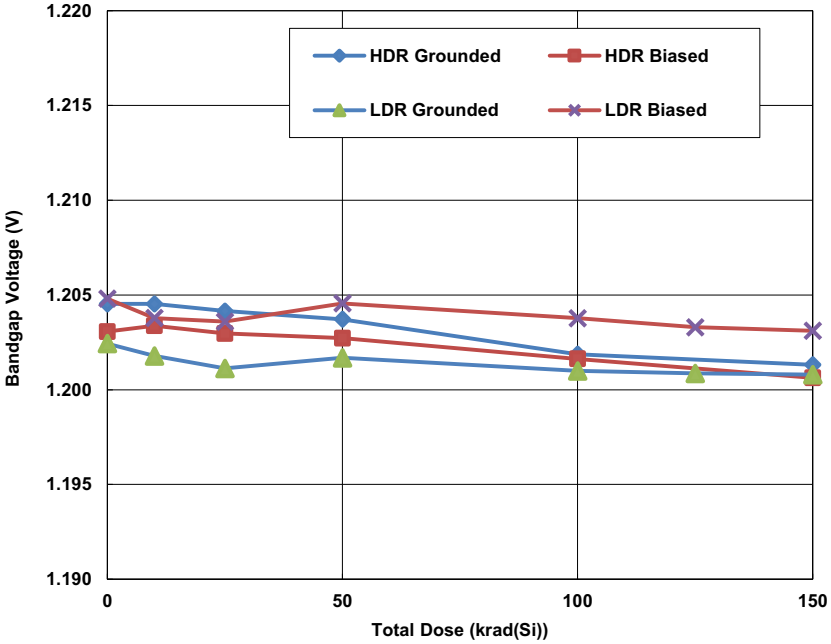


Figure 4. ISL70001SRH bandgap voltage as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. Bandgap voltage is an informational parameter and is not specified in the SMD or datasheet.

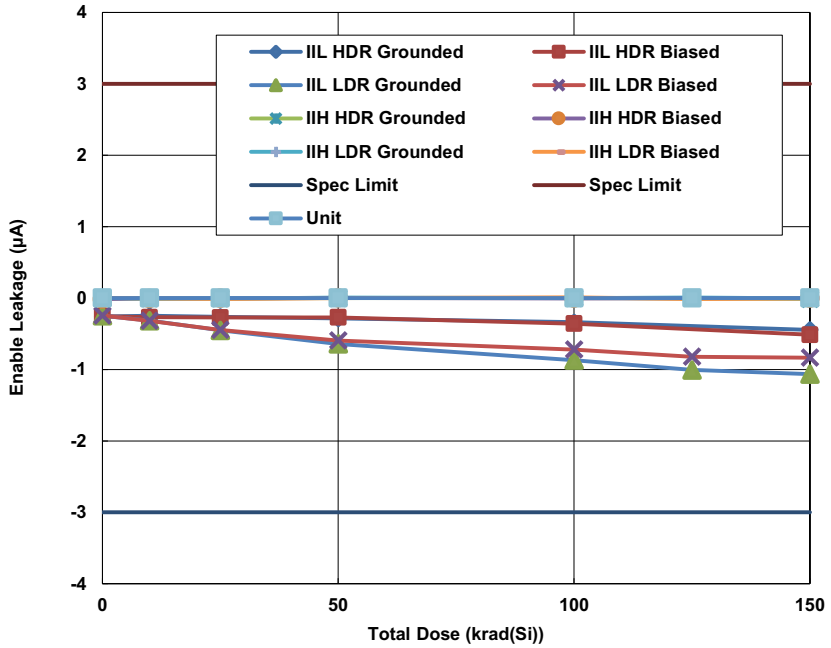


Figure 5. ISL70001SRH enable input LOW leakage current as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are -3µA to 3µA.

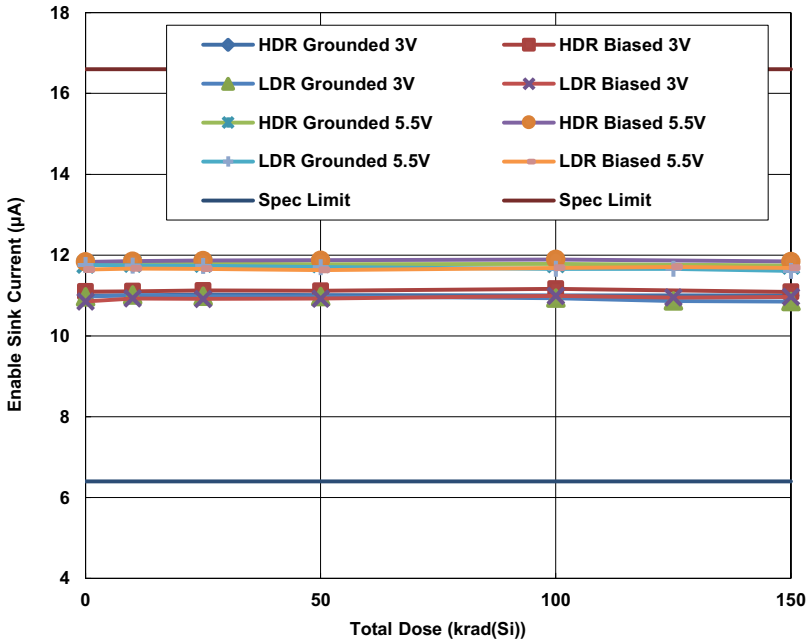


Figure 6. ISL70001SRH enable sink current (3V and 5.5V supply) as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are 6.46µA to 16.6µA.

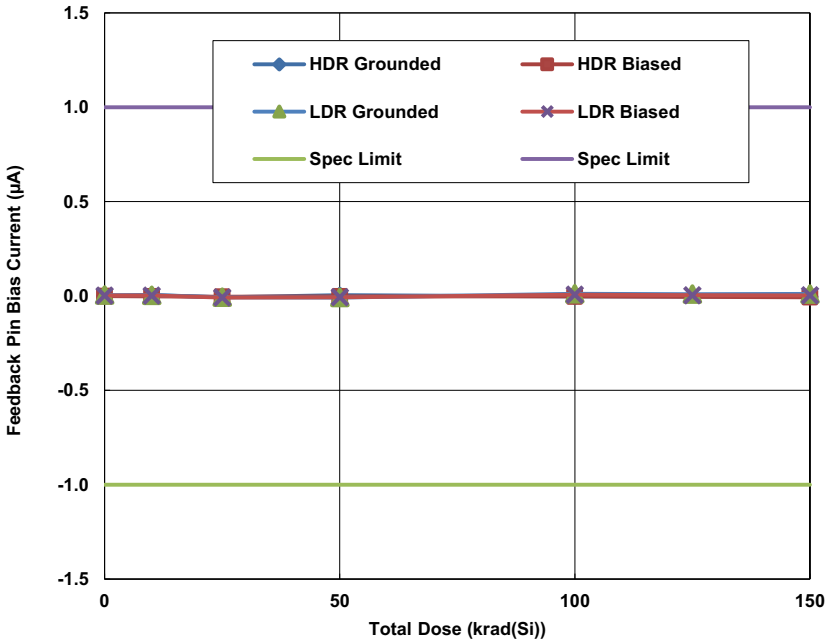


Figure 7. ISL70001SRH feedback pin input bias current as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are -1µA to 1µA.

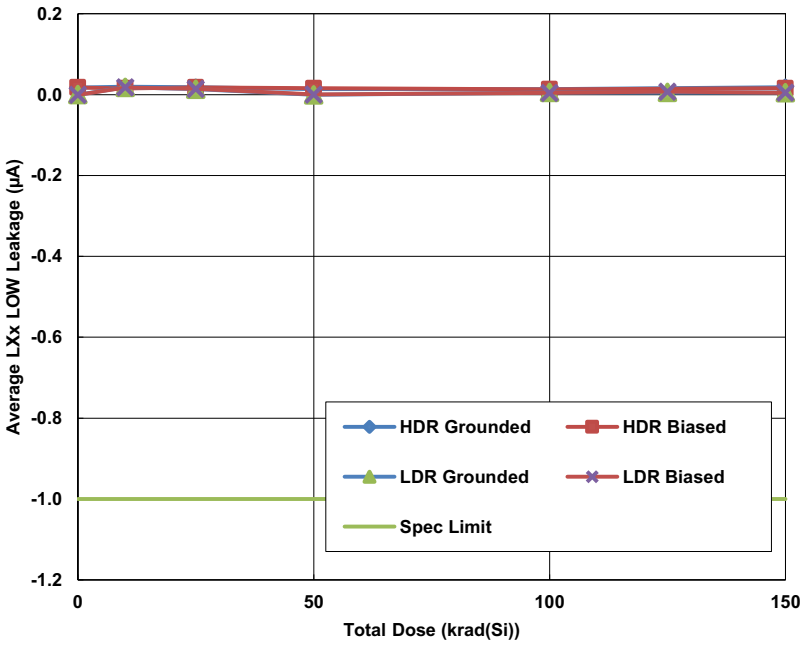


Figure 8. ISL70001SRH average of LX1 through LX6 LOW leakage current as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limit is -1µA minimum.

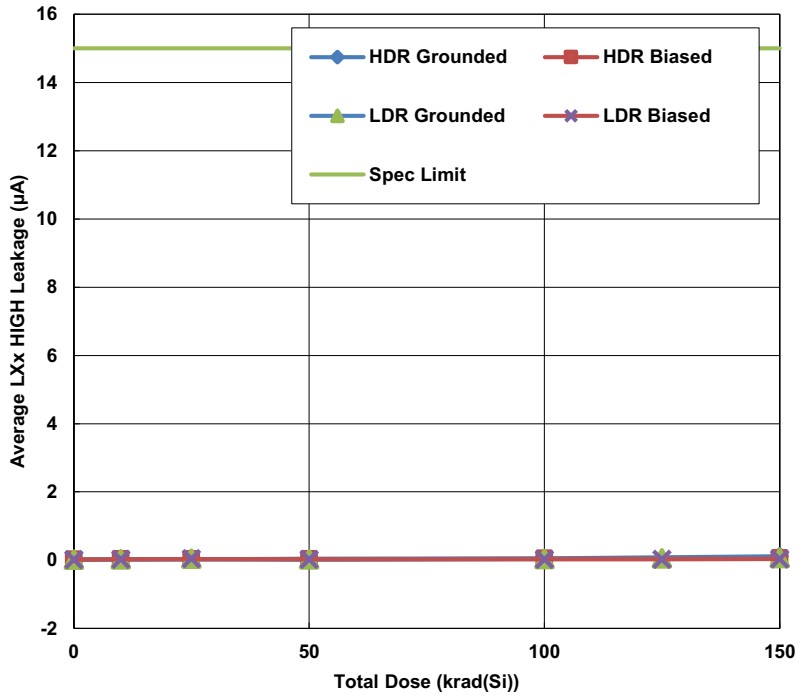


Figure 9. ISL70001SRH average of LX1 through LX6 HIGH leakage current as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limit is 15µA maximum.

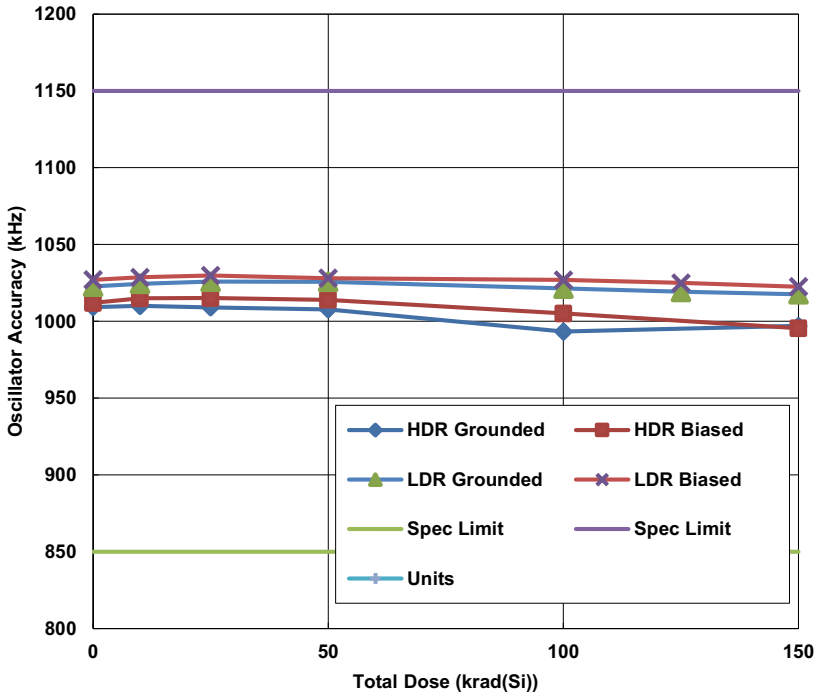


Figure 10. ISL70001SRH average oscillator frequency as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are 850kHz – 1150kHz.

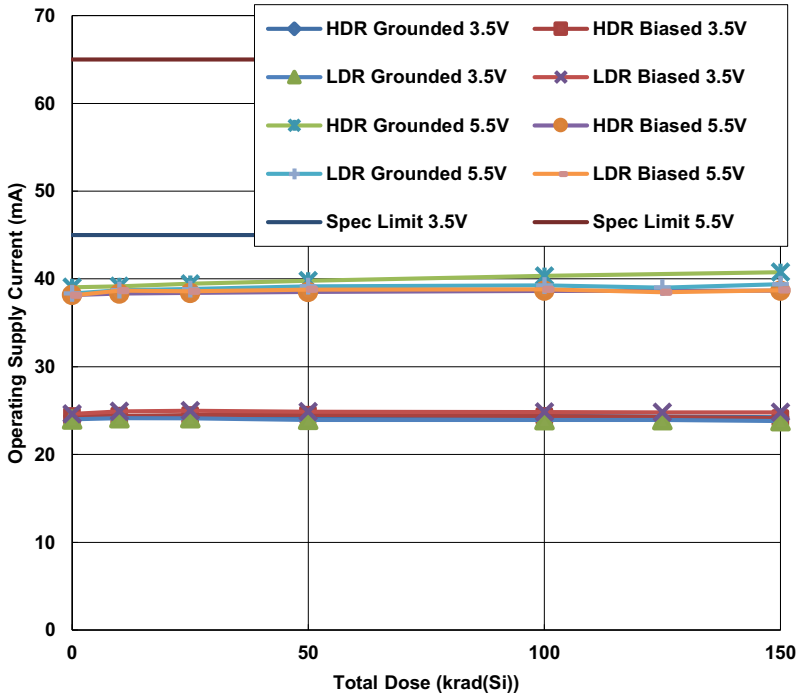


Figure 11. ISL70001SRH operating current (3.5V and 5.5V supply) as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are 45mA maximum (3.5V supply) and 65mA maximum (5.5V supply).

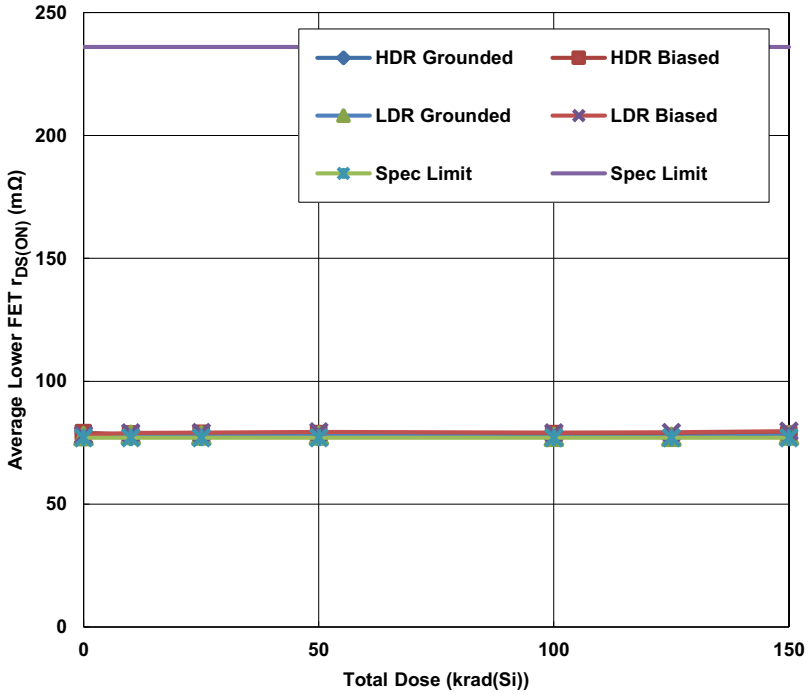


Figure 12. ISL70001SRH average lower LX1 through LX6 FET $r_{DS(ON)}$ resistance as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are 77mΩ to 236mΩ.

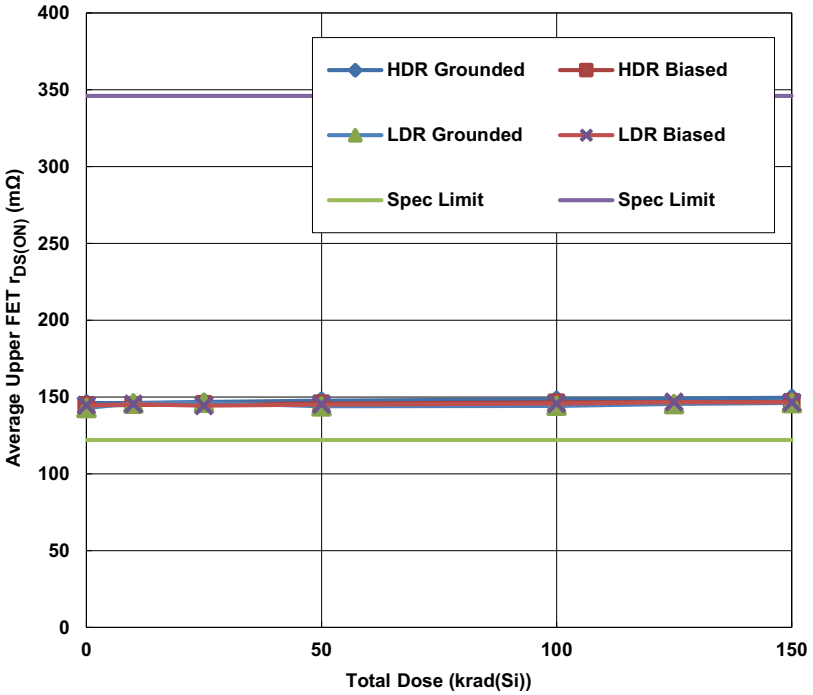


Figure 13. ISL70001SRH average upper LX1 through LX6 FET $r_{DS(ON)}$ resistance as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are 122mΩ to 346mΩ.

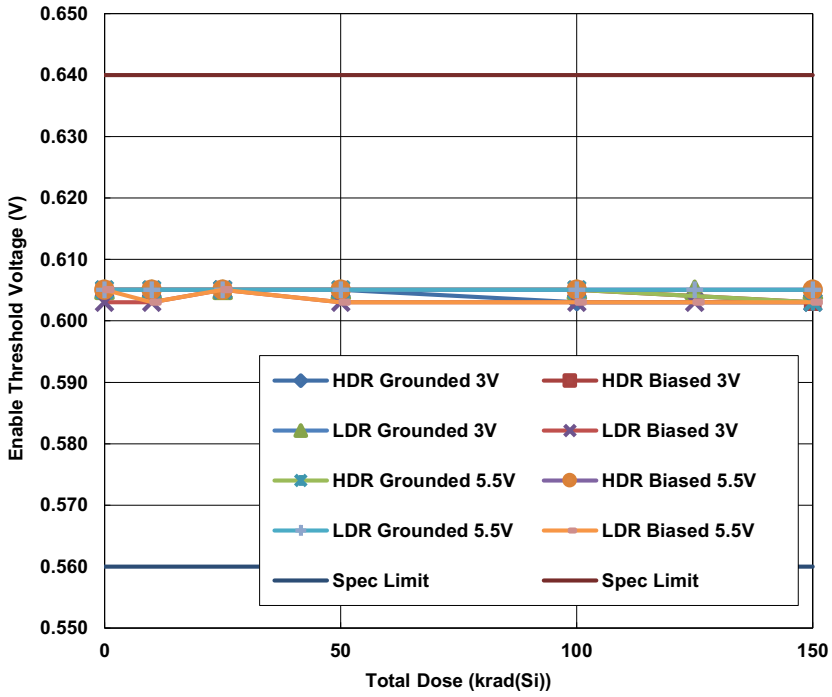


Figure 14. ISL70001SRH enable threshold voltage, 3V and 5.5V supply voltage, as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are 0.560V - 0.640V.

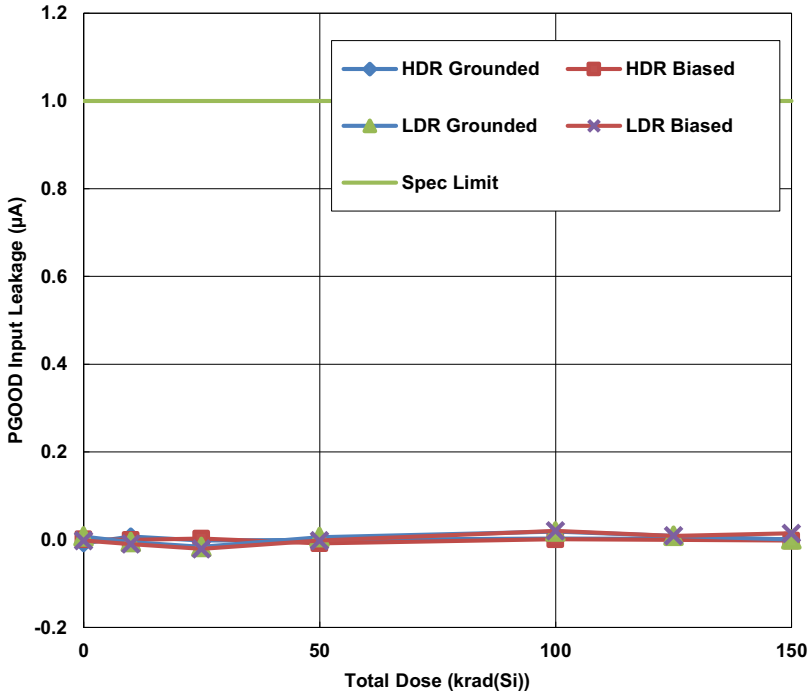


Figure 15. ISL70001SRH PGOOD input leakage current as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limit is 1µA maximum.

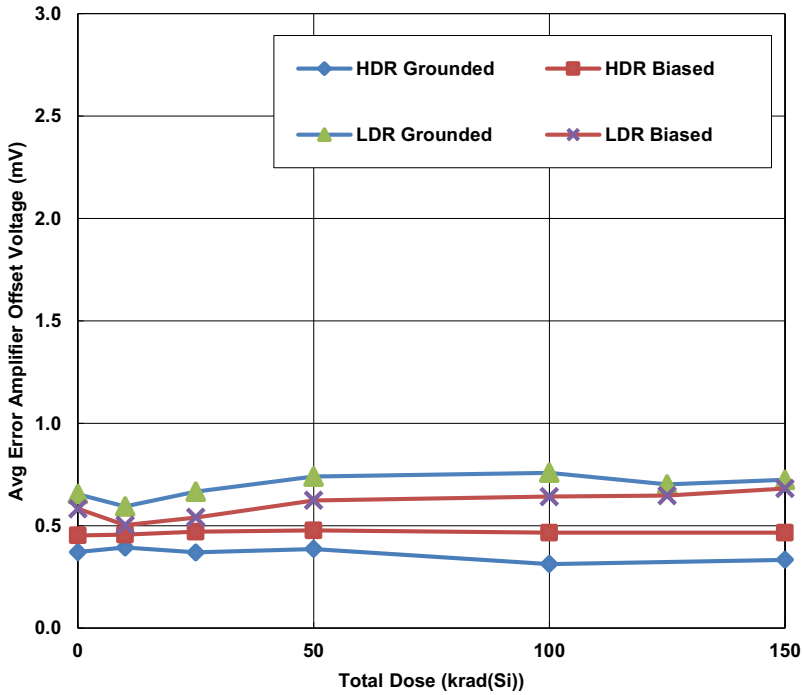


Figure 16. ISL70001SRH average error amplifier offset voltage (3V supply) as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. Error amplifier offset voltage is an informational parameter and is not formally specified in the SMD or datasheet.

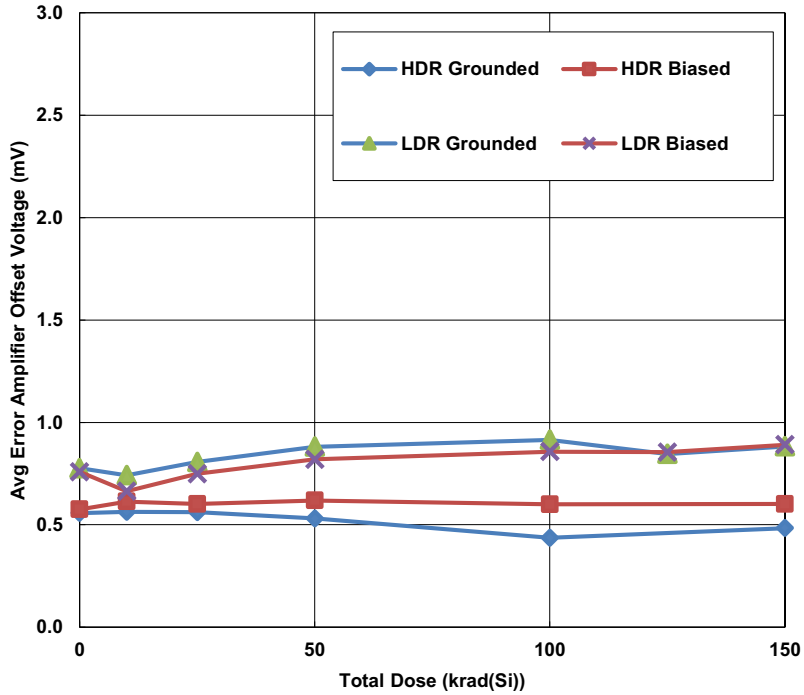


Figure 17. ISL70001SRH average error amplifier offset voltage (5.5V supply) as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. Error amplifier offset voltage is an informational parameter and is not formally specified in the SMD or datasheet.

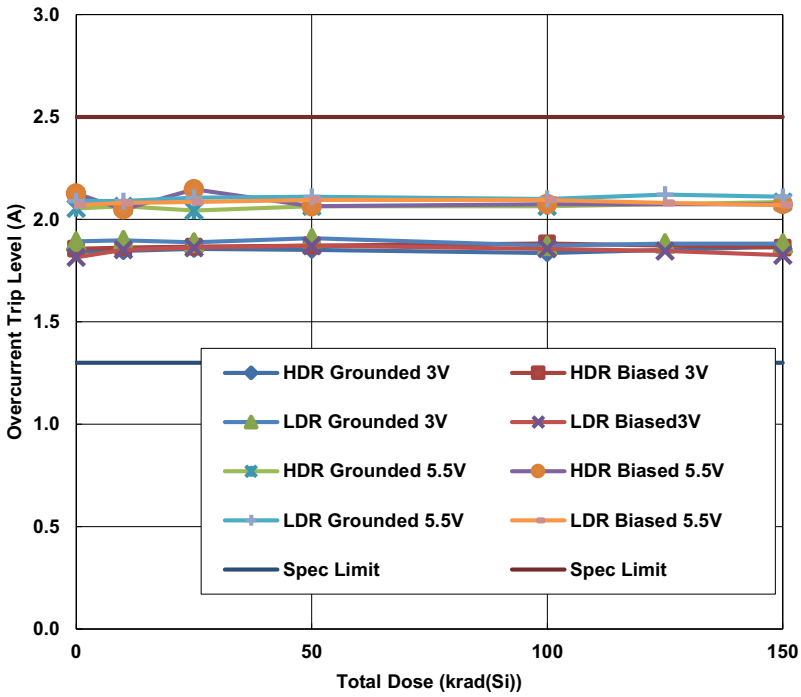


Figure 18. ISL70001SRH overcurrent limit threshold (3V and 5.5V supply) as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are 1.3A to 2.5A.

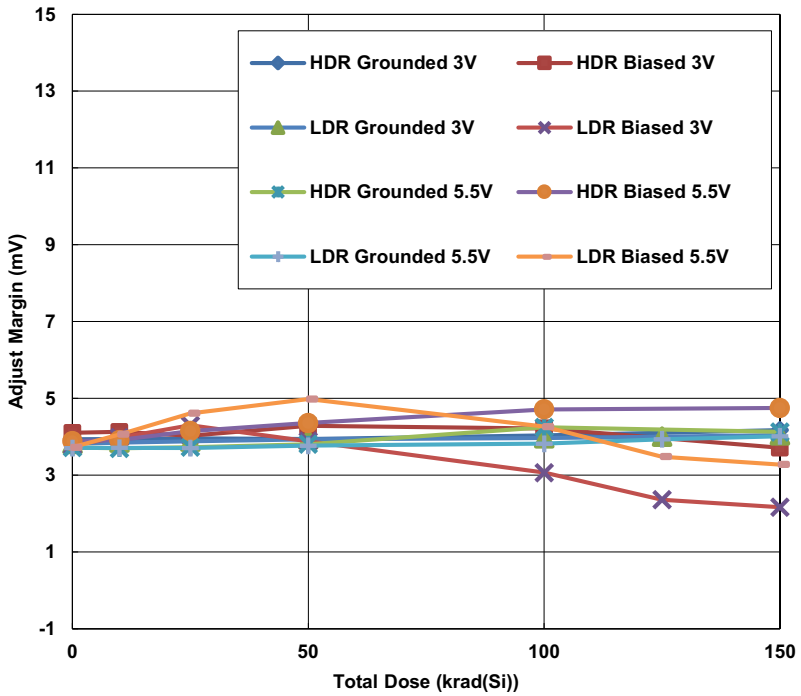


Figure 19. ISL70001SRH feedback adjust margin (3V and 5.5V supply) as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. Feedback adjust margin is an informational parameter and is not formally specified in the SMD or datasheet.

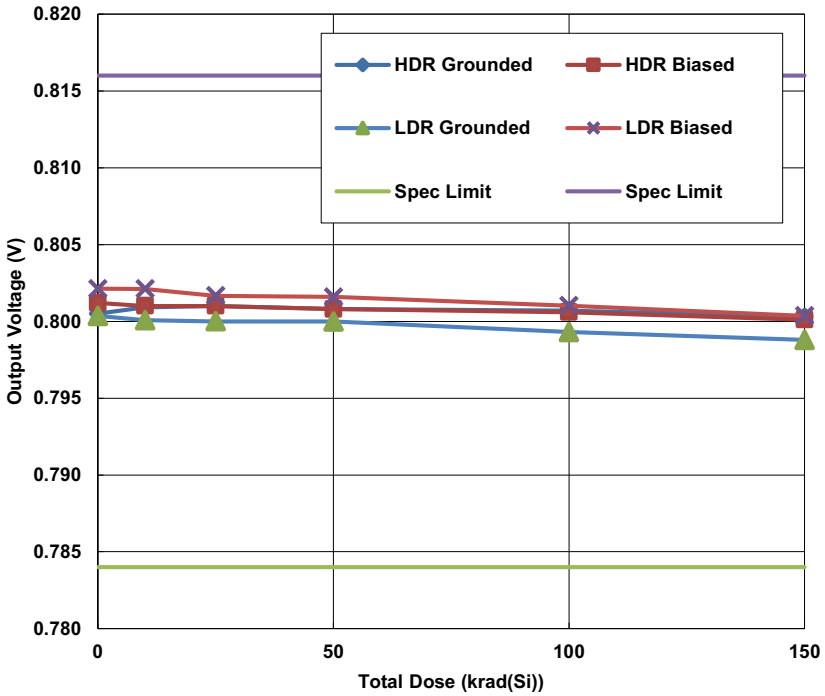


Figure 20. ISL70001SRH output voltage (3V supply) as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR was 55rad(Si)/s. Sample size for each cell was 5. The SMD limits are ±2% post-irradiation, which equals 0.784V to 0.816V for the 0.800V output voltage set point used for this test.

4. Conclusion

This document reports the results of total dose testing of the ISL70001SRH hardened point-of-load regulator. Parts were tested at LDR and HDR under biased and unbiased conditions as outlined in MIL-STD-883 Test Method 1019, to a maximum total dose of 150krad(Si) at both dose rates.

ATE characterization testing at downpoints showed no rejects to the SMD Group A limits. Variables data for selected parameters is presented in Figure 3 through Figure 20.

As a determinant of LDR sensitivity, MIL-STD-883 Test Method 1019.7 specifies that a delta_parameter calculation can be performed for any parameters that exceed the Group A limits. These calculations were not required as there were no rejects against the Group A limits. Accordingly, the ISL70001SRH is considered ELDRS-free up to the 100krad(Si) total dose rating specified in the SMD. It should be noted that the ISL70001SRH pre-irradiation and post-irradiation limits are identical.

Similarly, no differences between biased and unbiased irradiation were noted, and the part is not considered bias sensitive.

The ISL70001ASRH is a minor revision of the ISL70001SRH to correct a startup issue and the total dose results in this report are considered to be closely applicable to this part. The ISL70001SEH and ISL70001ASEH are variants that are acceptance tested at both LDR and HDR on a wafer-by-wafer basis and differ from the –RH versions in these screening procedures only. The ISL71001SLHM and ISL71001SEHM are plastic versions of the ISL70001SRH that use a 64 Ld Thin Quad Flatpack (EP-TQFP) plastic package, and the TID results provided in this report apply equally to these parts as well.

5. Revision History

Revision	Date	Description
1.0	Jun 8, 2021	Initial release

Appendix A: Reported Parameters

Table 2. Key Total Dose Parameters

Fig.	Parameter[1]	Low Limit	High Limit	Units	Notes
3	Reference Voltage	0.594	0.606	V	
4	Bandgap Voltage	none	none	V	Info only
5	Enable Low Leakage	-3	3	µA	
	Enable High Leakage	-3	3	µA	
6	Enable Sink Current	6.46	16.6	µA	3.6V supply
		6.46	16.6	µA	5.5V supply
7	FB Pin Bias Current	-1	1	µA	
8	LXx Low Leakage	-1	-	µA	Average of LX1 – LX6
9	LXx High Leakage	-	15	µA	Average of LX1 – LX6
10	Oscillator Frequency	850	1150	kHz	
11	Operating Supply Current	-	45	mA	3.6V supply
		-	65	mA	5.5V supply
12	Lower FET $r_{DS(ON)}$	77	236	mΩ	Average of LX1 – LX6
13	Upper FET $r_{DS(ON)}$	122	346	mΩ	Average of LX1 – LX6
14	Enable Threshold Voltage	0.56	0.64	V	3.6V supply
		0.56	0.64	V	5.5V supply
15	PGOOD Input Leakage	-	1	µA	
16	Error Amplifier Offset Voltage (3.6V)	none	none	mV	Info only, 3.6V supply
17	Error Amplifier Offset Voltage (5.5V)	none	none	mV	Info only, 5.5V supply
18	Overcurrent Limit	1.3	2.5	A	3.6V supply
		1.3	2.5	A	5.5V supply
19	Feedback Adjust Margin	none	none	mV	Info only, 3V supply
		none	none	mV	Info only, 5.5V supply
20	Output Voltage, V_{DD} = 3V	0.784	0.816	V	V_{OUT} set point of 800mV

1. Limits are taken from Standard Microcircuit Drawing (SMD) 5962-09225.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.