

ISL70218SEH

Neutron Testing of the ISL70218SEH Dual, Low-Power Precision Amplifier

Introduction

This report summarizes the results for the 1MeV equivalent neutron testing of the [ISL70218SEH](#) dual operational amplifier. The test was conducted to determine the sensitivity of the part to Displacement Damage (DD) caused by neutron or proton environments. Planned neutron fluences ranged from $5 \times 10^{11} \text{ n/cm}^2$ to $1 \times 10^{14} \text{ n/cm}^2$ with actual fluences coming in within 10% of that. This project was carried out in collaboration with Honeywell Aerospace Corporation in Clearwater, FL. Their support is gratefully acknowledged. This report applies to the ISL70218SRH and ISL71218M devices too.

Related Literature

For a full list of related documents, visit our website:

- [ISL70218SEH](#) device page
- MIL-STD-883 test method 1017

Part Description

The ISL70218SEH is a dual, low-power precision amplifier optimized for single-supply applications. This operational amplifier features a common-mode input voltage range extending to 0.5V below the negative supply rail, rail-to-rail differential input voltage range, and rail-to-rail output voltage swing, which makes it ideal for single-supply applications where input operation at ground is important. The device features low power, low offset voltage, and low-temperature drift, making it ideal for applications requiring both high DC accuracy and AC performance. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency (DLA) in Columbus, OH. The SMD is the controlling document and must be cited when ordering.

Contents

1. Test Description	2
1.1 Irradiation Facility	2
1.2 Test Fixturing	2
1.3 Radiation Dosimetry	2
1.4 Characterization Equipment and Procedures	2
1.5 Experimental Matrix	2
2. Results	2
2.1 Attributes Data	3
2.2 Variables Data	3
3. Discussion and Conclusion	11
4. Appendices	11
4.1 Reported parameters	11
5. Revision History	11

1. Test Description

1.1 Irradiation Facility

Neutron fluence irradiations were performed on the test samples on June 25, 2018, at the WSMR Fast Burst Reactor (FBR) per MIL-STD-883G, Method 1017.2, with each part not powered during irradiation and all leads shorted. The target irradiation levels were $5 \times 10^{11} \text{ n/cm}^2$, $1 \times 10^{12} \text{ n/cm}^2$, $1 \times 10^{13} \text{ n/cm}^2$, and $1 \times 10^{14} \text{ n/cm}^2$. As neutron irradiation activates many of the heavier elements found in a packaged integrated circuit, the parts exposed at the higher neutron levels required (as expected) some cooldown time before being shipped back to Renesas (Palm Bay, FL) for electrical testing.

1.2 Test Fixturing

No formal irradiation test fixturing is involved, as these DD tests are bag tests in the sense that the parts are irradiated with all leads shorted together.

1.3 Radiation Dosimetry

Table 1 shows the TLD and Sulfur pellet dosimetry from WSMR indicating the total accumulated gamma dose and actual neutron fluence exposure levels for each set of samples. This dosimetry process is traceable to NIST (IAW ASTM E722).

Table 1. ISL70218SEH Neutron Fluence Dosimetry Data

TLD		Sulfur Pellet						
TLD Number	cGy(Si) ^[1]	Pellet #	Distance (inches)	Exposure ID	Flu >3MeV (n/cm ²)	% Unc ^[2]	Total Fluence (n/cm ²)	1Mev Si (n/cm ²)
292	1.151E+02	6478	26.6	Free Field	7.493E+10	7.1%	6.059E+11	5.212E+11
282	3.732E+02	6418	13.45	Free Field	2.826E+11	7.1%	2.230E+12	1.977E+12
265	2.140E+03	6490	24	Free Field	1.381E+12	7.1%	1.107E+13	9.58E+12
251	1.841E+04	6466	8	Free Field	1.294E+13	7.1%	1.016E+14	9.077E+13

1. 1cGy(Si) = 1 rad(Si)

2. The Uncertainty (% Unc) column is applicable only to the Fluence > 3MeV.

1.4 Characterization Equipment and Procedures

Electrical testing was performed before and after irradiation using the Intersil production automated test equipment (ATE). All electrical testing was performed at room temperature.

1.5 Experimental Matrix

Testing proceeded following the guidelines of MIL-STD-883 TM 1017. The experimental matrix consisted of five samples to be irradiated at $5 \times 10^{11} \text{ n/cm}^2$, five to be irradiated at $1 \times 10^{12} \text{ n/cm}^2$, five to be irradiated at $1 \times 10^{13} \text{ n/cm}^2$, and five to be irradiated at $1 \times 10^{14} \text{ n/cm}^2$. Two control units were used.

ISL70218SEH samples were drawn from Lot WLH4WAAKC. Samples were packaged in the standard hermetic 10 lead ceramic flatpack (CFP) production package. Samples were processed through burn-in before irradiation and were screened to the SMD limits at room, low, and high temperatures before the start of neutron testing.

2. Results

Neutron testing of the ISL70218SEH is complete and the results are reported in the balance of this report. It should be understood when interpreting the data that each neutron irradiation was performed on a different set of samples; this is not total dose testing, where the damage is cumulative.

2.1 Attributes Data

Table 2. Attributes Data

Fluence, (n/cm ²)		Sample Size	Pass ^[1]	Fail	Notes
Planned	Actual				
5x10 ¹¹	5.21x10 ¹¹	5	5	0	All passed
2x10 ¹²	1.98x10 ¹²	5	5	0	All passed
1x10 ¹³	9.58x10 ¹²	5	0	5	Some parameters failed
1x10 ¹⁴	9.08x10 ¹³	5	0	5	Most parameters failed

1. A Pass indicates a sample that passes all SMD limits.

2.2 Variables Data

Figure 1 through Figure 15 show data plots for key parameters before and after irradiation to each level. The plots show the mean of each parameter as a function of neutron irradiation. The plots also include error bars at each down point, representing the minimum and maximum measured values of the samples, although in some plots the error bars might not be visible due to their values compared to the scale of the graph. The applicable electrical limits taken from the SMD are also shown.

All samples passed the post-irradiation SMD limits after all exposures up to and including 1x10¹²n/cm², but all five units failed several SMD post-irradiation limits after 1x10¹³n/cm², and all five units failed most parameters after 1x10¹⁴n/cm² and some parameters could not be plotted without greatly increasing the minimum or maximum y-axis values of the graphs and comprising the usefulness of the passing data.

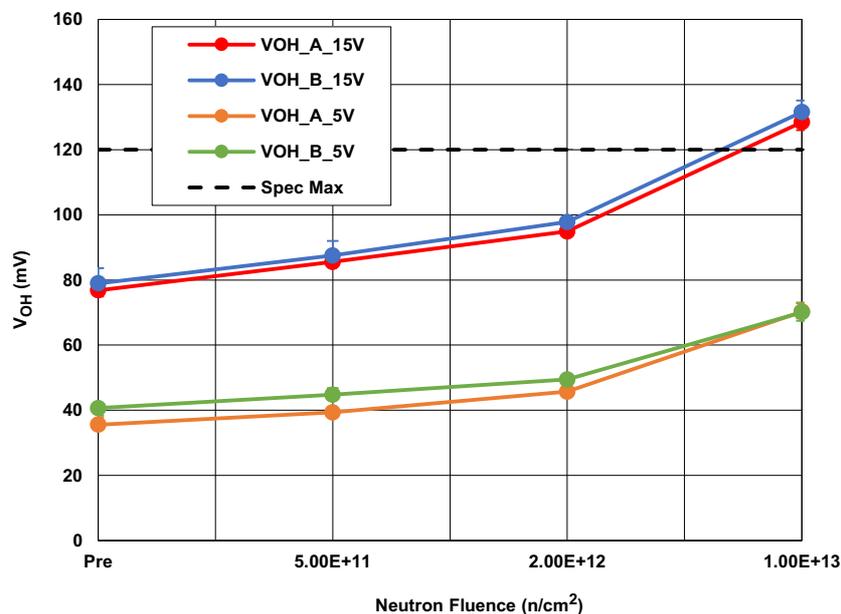


Figure 1. ISL70218SEH Output Voltage High (V_{OH}), Channels A and B, with V_S = 15V and 5V, R_L = 10kΩ, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 120mV maximum. The values at 1x10¹⁴n/cm² are not plotted due to the magnitude of their values.

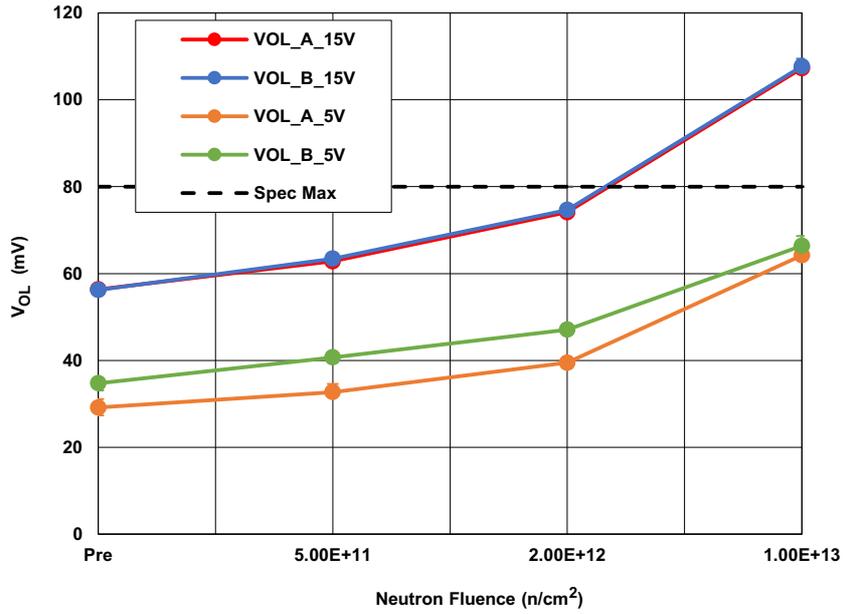


Figure 2. ISL70218SEH Output Voltage Low (V_{OL}), Channels A and B, with $V_S = 15V$ and $5V$, $R_L = 10k\Omega$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 80mV maximum. The values at $1 \times 10^{14} n/cm^2$ are not plotted due to the magnitude of their values.

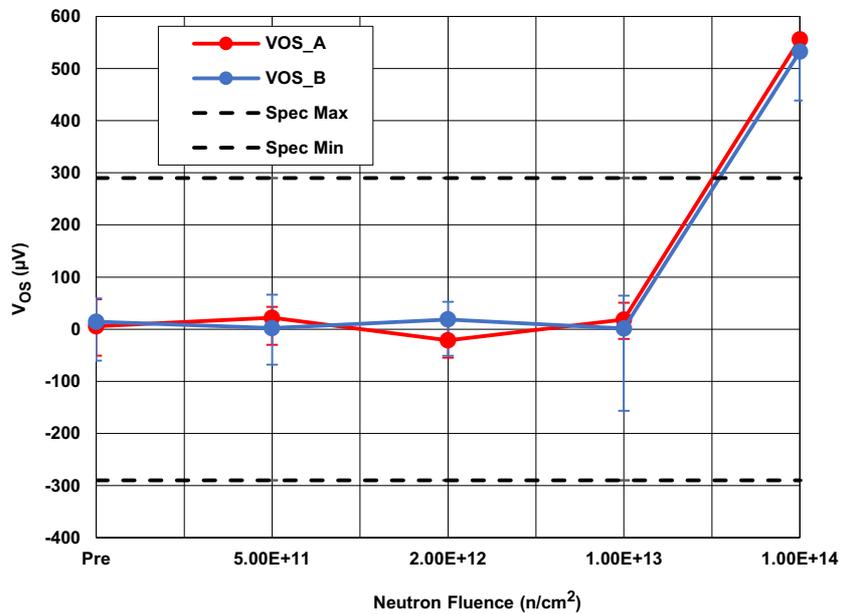


Figure 3. ISL70218SEH Input Offset Voltage (V_{OS}), Channels A and B, with $V_S = 15V$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are $-290\mu V$ minimum and $290\mu V$ maximum.

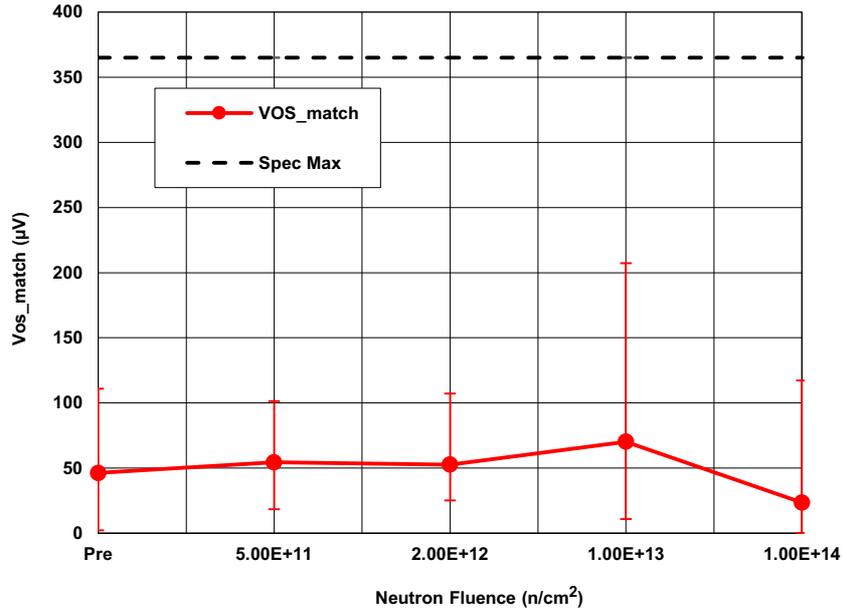


Figure 4. ISL70218SEH Input Offset Voltage Match (ΔV_{OS}) with $V_S = 15V$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 365µV maximum.

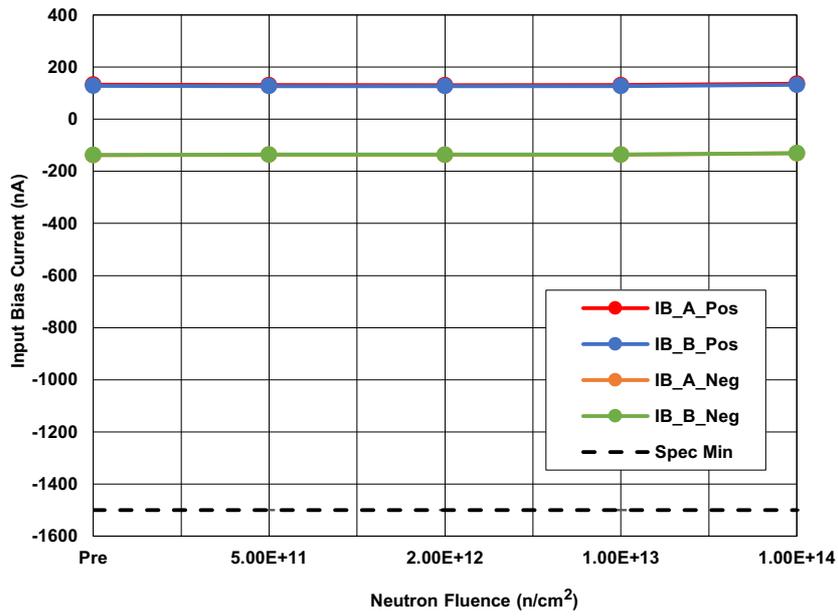


Figure 5. ISL70218SEH Input Bias Current (I_B), Channels A and B, with $V_S = 15V$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is -1500nA minimum.

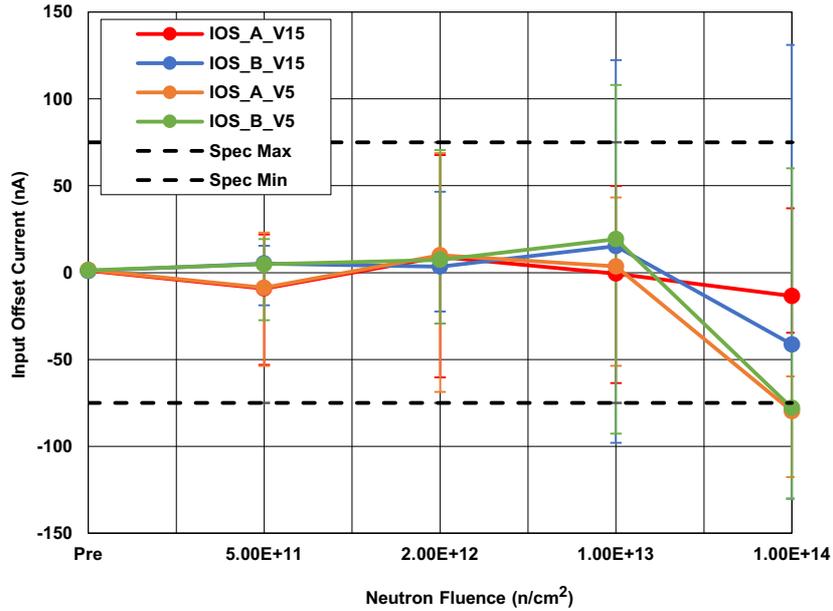


Figure 6. ISL70218SEH Input Offset Current (I_{OS}), Channels A and B, with $V_S = 15V$ and $5V$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are $-75nA$ minimum and $75nA$ maximum.

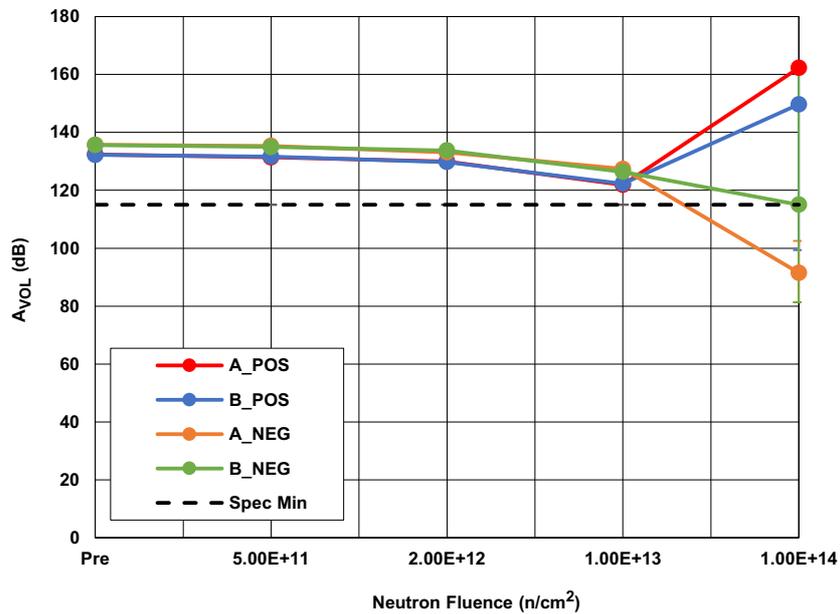


Figure 7. ISL70218SEH Open-Loop Gain (A_{VOL}), Channels A and B, with $V_S = 15V$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is $115dB$ minimum.

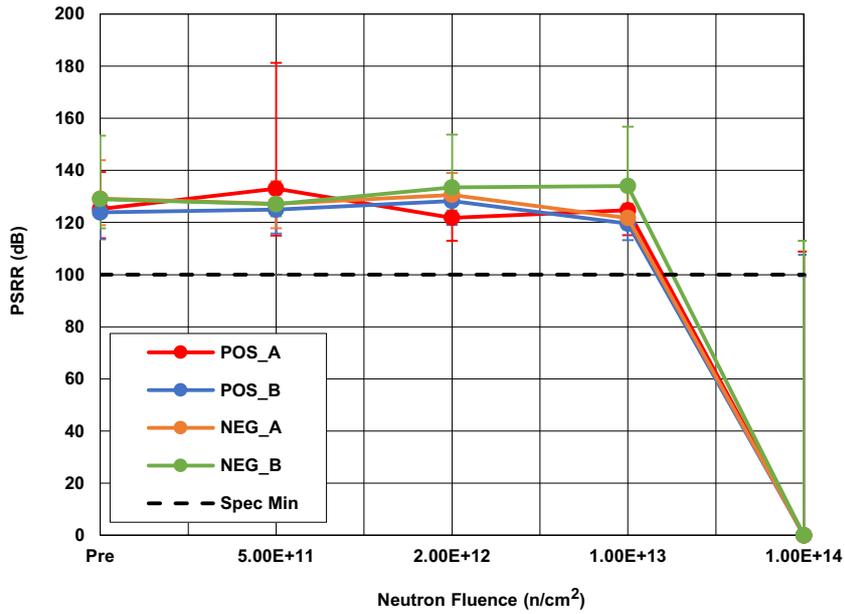


Figure 8. ISL70218SEH Power Supply Rejection Ratio (PSRR), Channels A and B, with $V_S = 15V$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 100dB minimum.

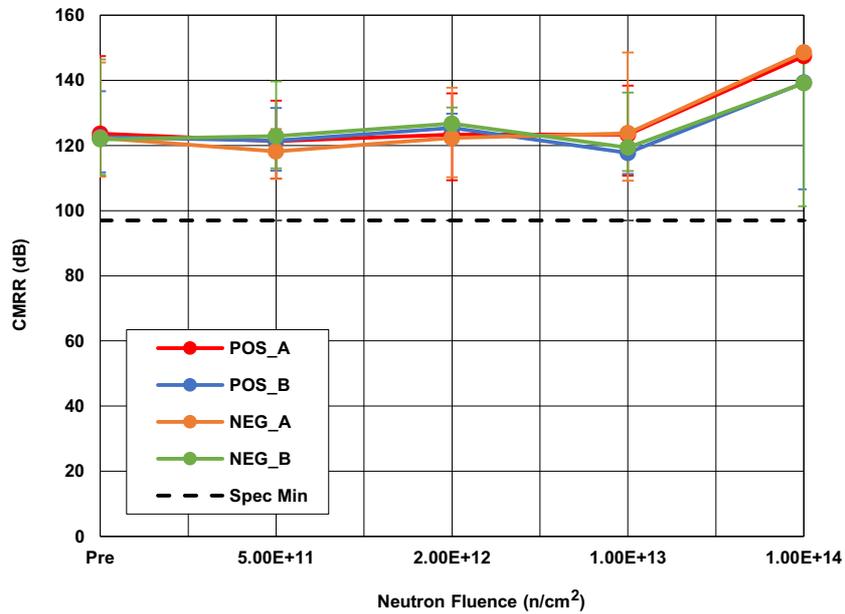


Figure 9. ISL70218SEH Common-Mode Rejection Ratio (CMRR), Channels A and B, with $V_S = 15V$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 97dB minimum.

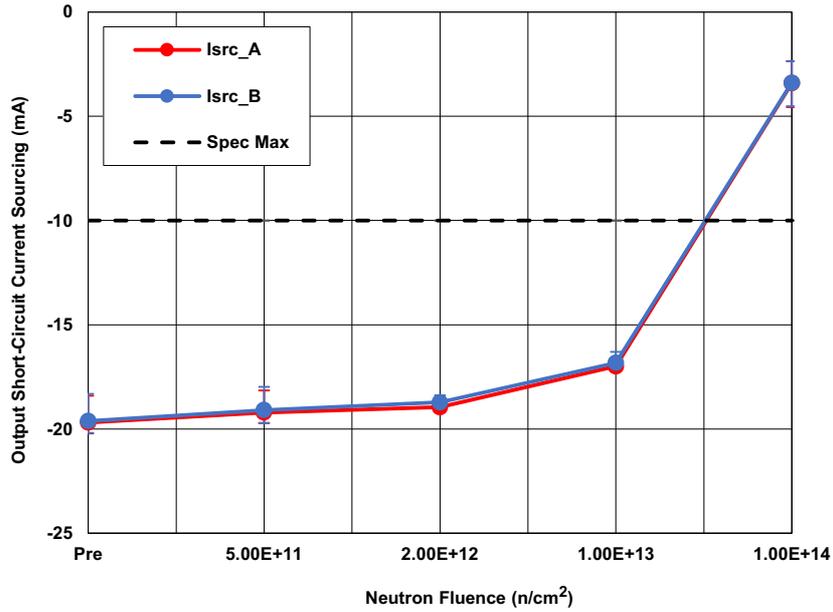


Figure 10. ISL70218SEH Output Short-Circuit Current, Sourcing, (I_{S+}), Channels A and B, with $V_S = 15V$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is -10mA maximum.

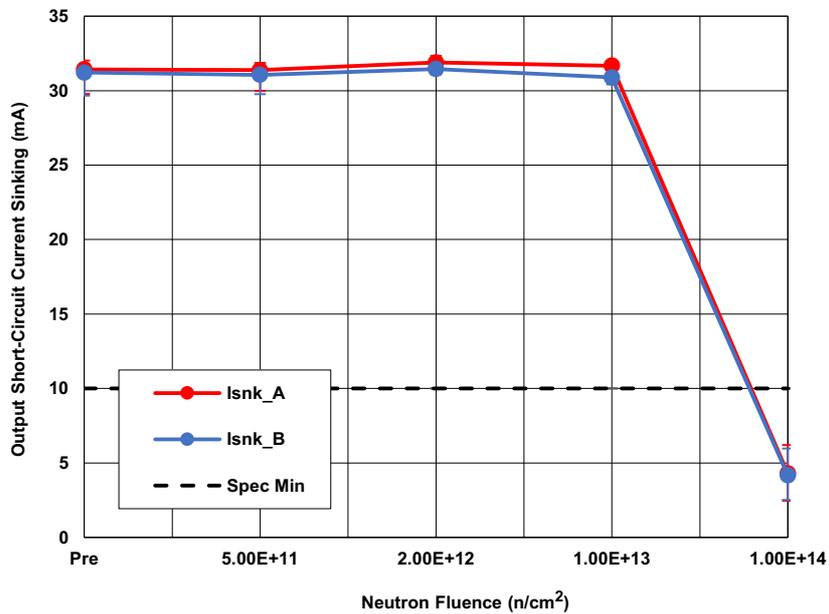


Figure 11. ISL70218SEH Output Short-Circuit Current, Sinking, (I_{S-}), Channels A and B, with $V_S = 15V$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 10mA minimum.

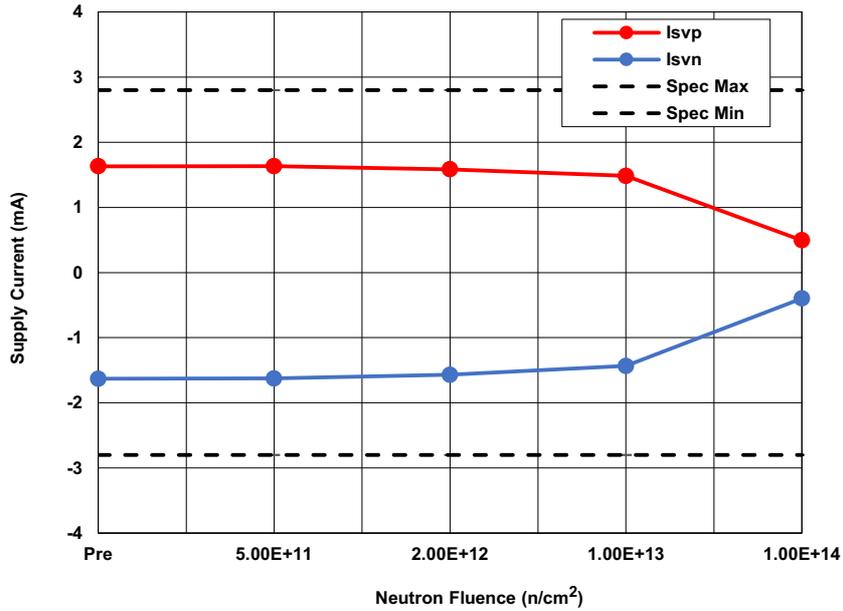


Figure 12. ISL70218SEH Supply Current (I_S), Channels A and B, with $V_S = 15V$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -2.8mA minimum and 2.8mA maximum.

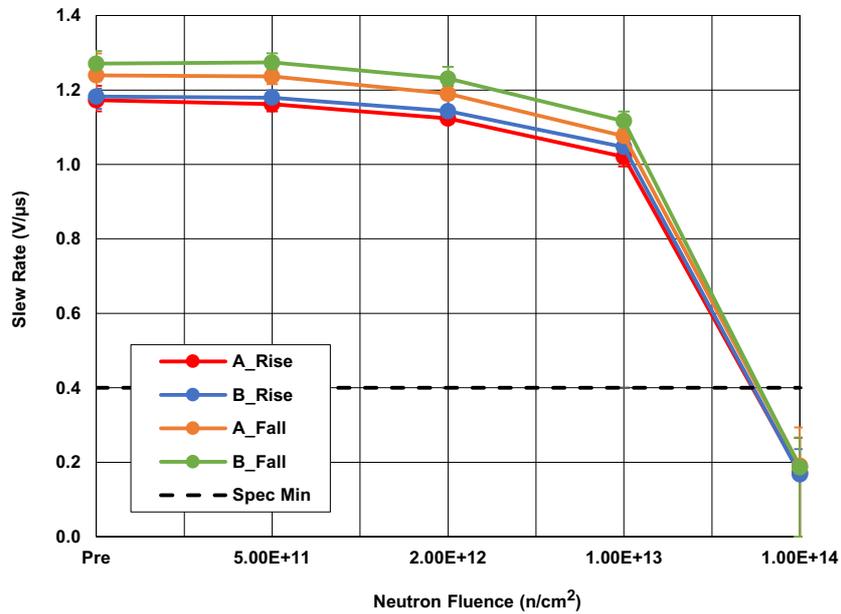


Figure 13. ISL70218SEH Slew Rate (SR), Channels A and B, with $V_S = 15V$, $AV = 1$, $R_L = 2k\Omega$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is $0.4V/\mu s$.

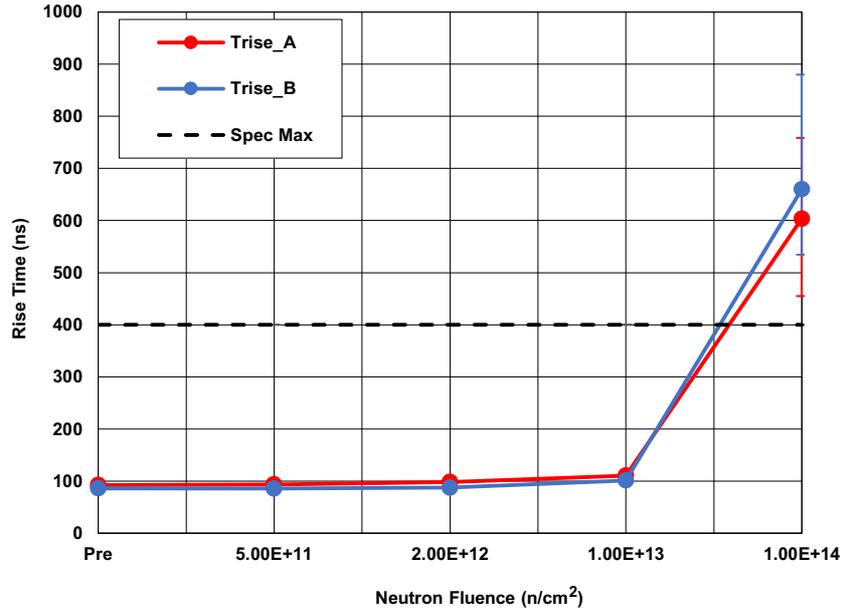


Figure 14. ISL70218SEH Rise Time (t_r), Channels A and B, with $V_S = 15V$, $AV = 1$, $R_L = 2k\Omega$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 400ns maximum.

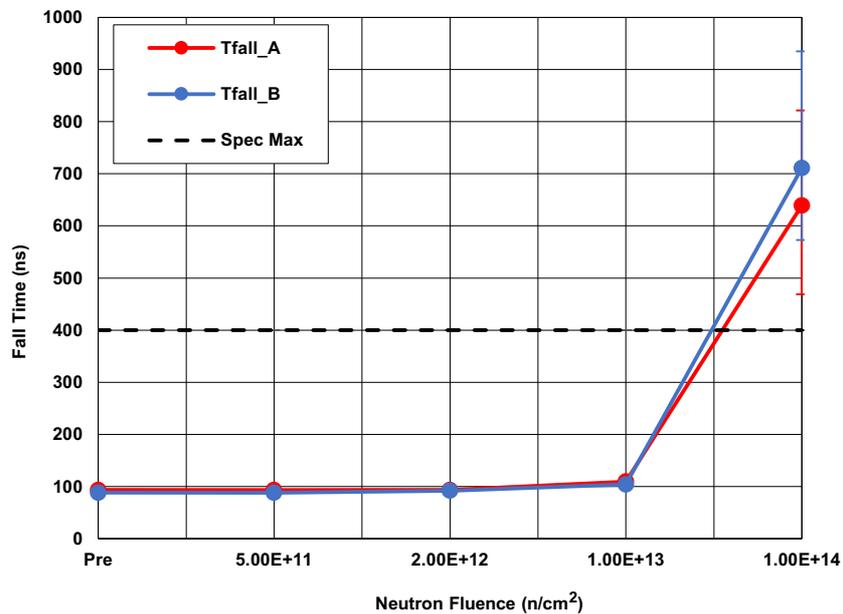


Figure 15. ISL70218SEH fall time (t_f) channels A and B, with $V_S = 15V$, $AV = 1$, $R_L = 2k\Omega$, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 400ns maximum.

3. Discussion and Conclusion

This document reports the results of 1MeV equivalent neutron testing of the ISL70218SEH dual, low-power precision amplifier. Parts were tested at $1 \times 10^{11} \text{n/cm}^2$, $5 \times 10^{11} \text{n/cm}^2$, $1 \times 10^{12} \text{n/cm}^2$, $1 \times 10^{13} \text{n/cm}^2$, and $1 \times 10^{14} \text{n/cm}^2$. All samples passed the post-irradiation SMD limits after all exposures up to and including $1 \times 10^{12} \text{n/cm}^2$, but all five units failed several SMD post-irradiation limits after $1 \times 10^{13} \text{n/cm}^2$, and all five units failed almost all parameters after $1 \times 10^{14} \text{n/cm}^2$. The results of key parameters before and after irradiation to each level are plotted in [Figure 1](#) through [Figure 15](#). The plots show the mean of each parameter as a function of neutron irradiation, with error bars that represent the minimum and maximum measured values. The figures also show the applicable electrical limits taken from the SMD.

4. Appendices

4.1 Reported parameters

Figure	Parameter	Symbol	Low Limit	High Limit	Units	Notes
1	Output Voltage High	V_{OH}	-	120	mV	Ch A and B
2	Output Voltage Low	V_{OL}	-	80	mV	Ch A and B
3	Input Offset Voltage	V_{OS}	-290	290	μV	Ch A and B
4	Input Offset Voltage Match	ΔV_{OS}	-	365	μV	Ch to Ch
5	Input Bias Current	I_B	-1500	-	nA	Ch A and B
6	Input Offset Current	I_{OS}	-75	75	nA	Ch A and B
7	Open-Loop Gain	A_{VOL}	115	-	dB	Ch A and B
8	Power Supply Rejection Ratio	PSRR	100	-	dB	Ch A and B
9	Common-Mode Rejection Ratio	CMRR	97	-	dB	Ch A and B
10	Output Short-Circuit Current, Sourcing	I_{S+}	-10	-	mA	Ch A and B
11	Output Short-Circuit Current, Sinking	I_{S-}	10	-	mA	Ch A and B
12	Supply Current	I_S	-2.8	2.8	mA	Sum of both Ch
13	Slew Rate	SR	0.4	-	$\text{V}/\mu\text{s}$	Ch A and B
14	Rise Time	t_r	400	-	ns	Ch A and B
15	Fall Time	t_f	400	-	ns	Ch A and B

5. Revision History

Rev.	Date	Description
1.01	May 28, 2025	Applied the latest template. Updated Data Variables and Discussion and Conclusion sections.
1.00	Mar 12, 2020	Initial release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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