Total dose testing of the ISL7124SRH Radiation Hardened Quad operational amplifier

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1. Introduction

This report reports the results of a low and high dose rate total dose test of the ISL7124SRH quad operational amplifier. The test was conducted in order to determine the sensitivity of the part to the total dose environment and to determine if dose rate and bias sensitivity exist.

2. Reference Documents

MIL-STD-883G test method 1019.7
ISL7124SRH data sheet
DSCC Standard Microcircuit Drawing (SMD) 5962-02542

3: Part Description

The single-event radiation hardened ISL7124SRH consists of four independent internally frequency compensated operational amplifiers, specifically designed to operate from a single power supply over a wide range of voltages. The device is functionally equivalent to industry standard 124 types, offering improvements in supply current and power supply rejection ratio.

Constructed with Intersil's dielectrically isolated, radiation hardened silicon gate (RSG) BiCMOS process, this device is immune to single event latchup. Additionally, the design has been hardened to prevent single event transients (SETs) in excess of 1V for LETs up to 36MeV/mg/cm^2.

The ISL7124SRH has been specifically designed and manufactured to provide reliable performance in harsh radiation environments. It is total dose hardened to 300krad(Si) at high dose rate and offers guaranteed performance over the full -55^{o}C to +125^{o}C military temperature range.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering. Detailed electrical specifications for this device are contained in SMD 5962-02542. A "hot-link" is provided on the Intersil website for downloading.

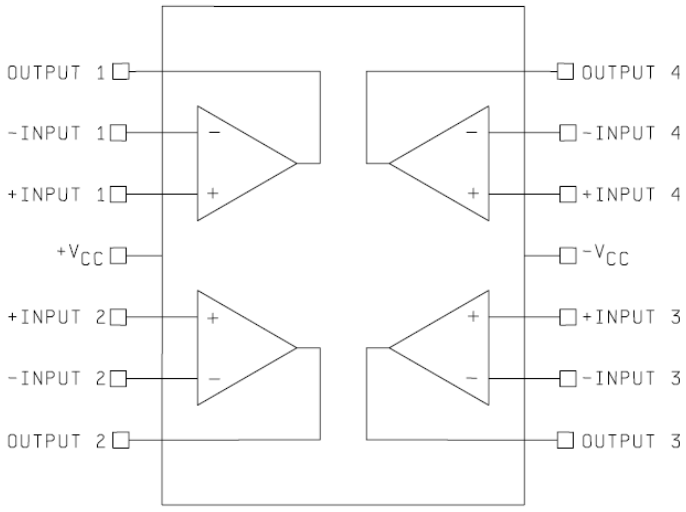

Figure 1: ISL7124SRH block diagram.

4: Test Description

4.1 Irradiation Facilities

High dose rate testing was performed using a Gammacell 220 ^{60}Co irradiator located in the Palm Bay, Florida Intersil facility. Low dose rate testing was performed on a subcontract basis at White Sands Missile Range (WSMR) Survivability, Vulnerability and Assessment Directorate (SVAD), White Sands, NM, using a vault-type ^{60}Co irradiator. The high dose rate irradiations were done at 55rad(Si)/s and the low dose rate work was performed at 0.010rad(Si)/s, both per MIL-STD-883 Method 1019.7. Dosimetry for both tests was performed using Far West Technology radiochromic dosimeters and readout equipment.

4.2 Test Fixturing

Figure 2 shows the configuration used for biased irradiation in conformance with Standard Microcircuit Drawing (SMD) 5962-02542.

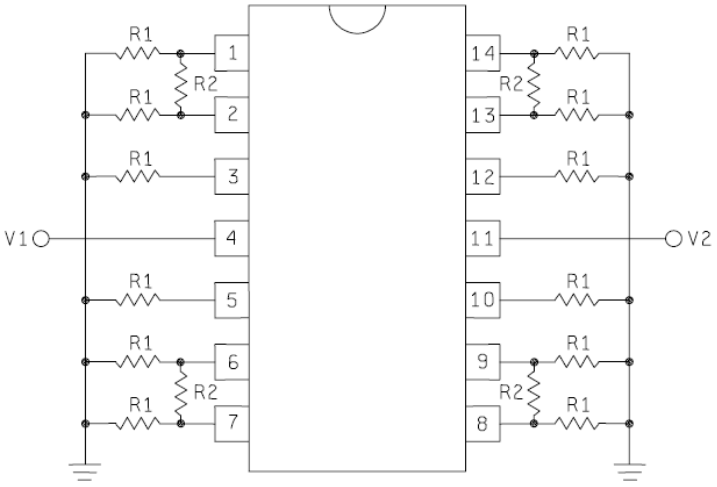

Figure 2: Irradiation bias configuration for the ISL7124SRH per Standard Microcircuit Drawing (SMD) 5962-02542.

4.3 Characterization equipment and procedures

All electrical testing was performed outside the irradiator using the production automated test equipment (ATE) with datalogging at each downpoint. Downpoint electrical testing was performed at room temperature. Performing low dose rate testing at a remote site introduces some challenges, and shipping had to be done in a foam container with a frozen Gelpack™ along with a strip chart temperature recorder in order to remain well within the temperature limits imposed by MIL-STD-883 Test Method 1019.7. Close coordination between the two organizations is required, and support by WSMR is gratefully acknowledged.

4.4 Experimental matrix

Total dose irradiations proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019.7. The experimental matrix consisted of five samples irradiated at high dose rate with all pins grounded, five samples irradiated at high dose rate under bias, five samples irradiated at low dose rate with all pins grounded and five samples irradiated at low dose rate under bias. One control unit was used.

Samples of the ISL7124SRH die were drawn from wafer 3 of production lot DCR6TFA and were packaged in the standard hermetic 14-pin solder-sealed flatpack (CDFP4-F14) production package. Samples were processed through the standard burnin cycle before irradiation, as required by MIL-STD-883, and were screened to the SMD 5962-02542 limits at room, low and high temperatures prior to the test.

4.5 Downpoints

Downpoints for the tests were zero, 50krad(Si), 100krad(Si) and 150krad(Si) for the high dose rate test and zero, 10krad(Si), 25krad(Si), 50krad(Si), 100krad(Si), 125krad(Si) and 150krad(Si) for the low dose rate test.

5: Results

5.1 Test results

Testing at both dose rates to 150krad(Si) of the ISL7124SRH is complete.

The part was found to be dose rate sensitive, with unbiased low dose rate irradiation worst case as expected. The input offset voltage was outside the +/-10mV SMD post-irradiation specification at the 100krad(Si) downpoint. The positive input bias current was close to the +/-400nA post-irradiation limit at the 125krad(Si) downpoint but recovered somewhat at 150krad(Si). The cause of the bias current degradation is considered to be the gradually degradation of the current gain (‘beta’) of the input PNP transistor pair. The negative input bias current was outside the +/-400nA limit after 125krad(Si). The input offset current remained very stable, indicating that the input pair current gain remains well-matched in spite of the degradation in absolute value.

Open-loop voltage gain was outside the 20V/mV (86dB) minimum limit at the 100krad(Si) downpoint. Common-mode rejection ratio data for Channel 3 was of doubtful quality, as was the positive and negative slew rate data for Channels 2 and 4. We have plotted this anomalous data for information only.

The part is considered low dose rate sensitive but remains within the SMD post-irradiation limits to a maximum of 50krad(Si) in this environment. Similarly, we observed some bias sensitivity in the low dose rate results.

5.2 Variables data

The plots in Figures 3 through 59 show data at all downpoints. The plots show the median of key parameters as a function of total dose for each of the four irradiation conditions. We chose to plot the median for these parameters due to the relatively small sample sizes.

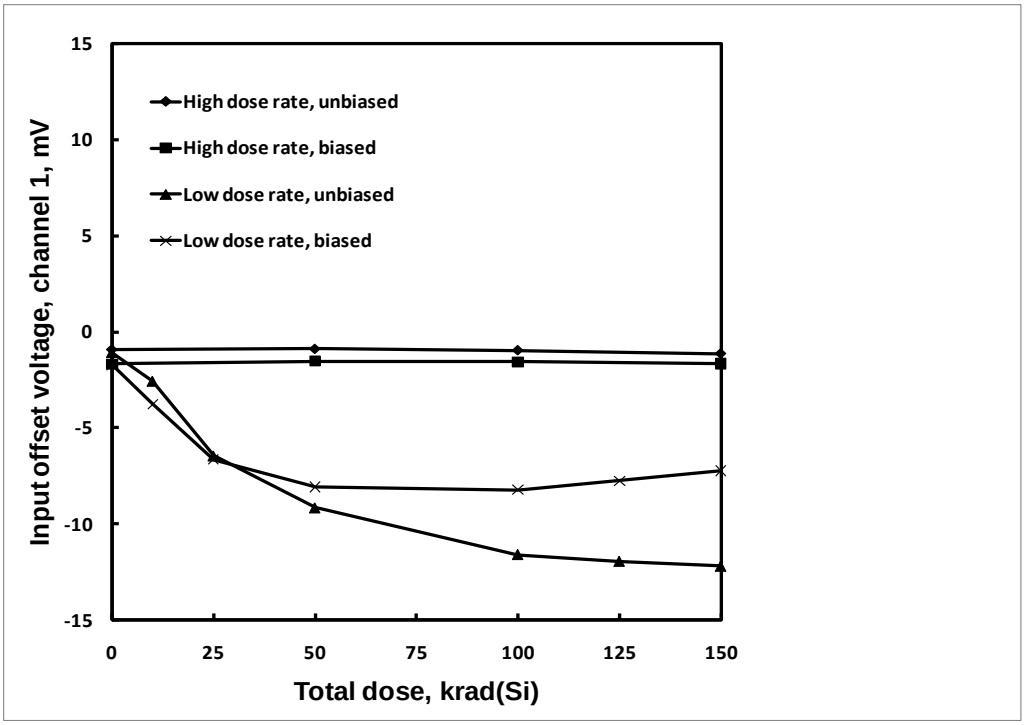

Figure 3: ISL7124SRH input offset voltage, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are -10mV to +10mV.

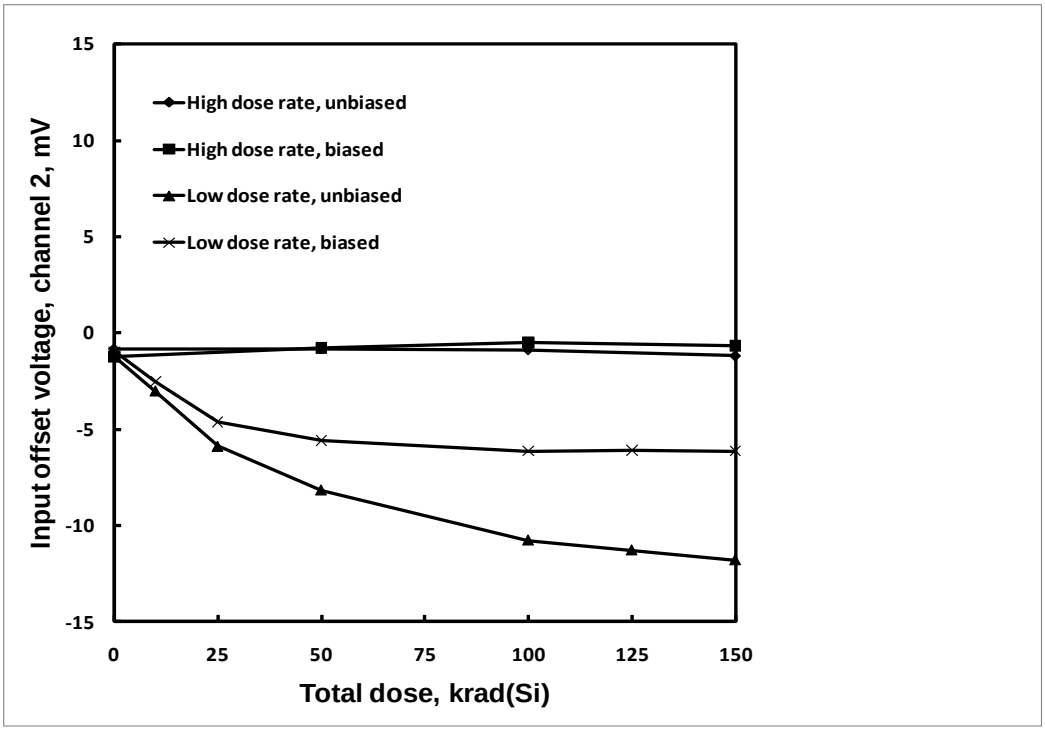

Figure 4: ISL7124SRH input offset voltage, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are -10mV to +10mV.

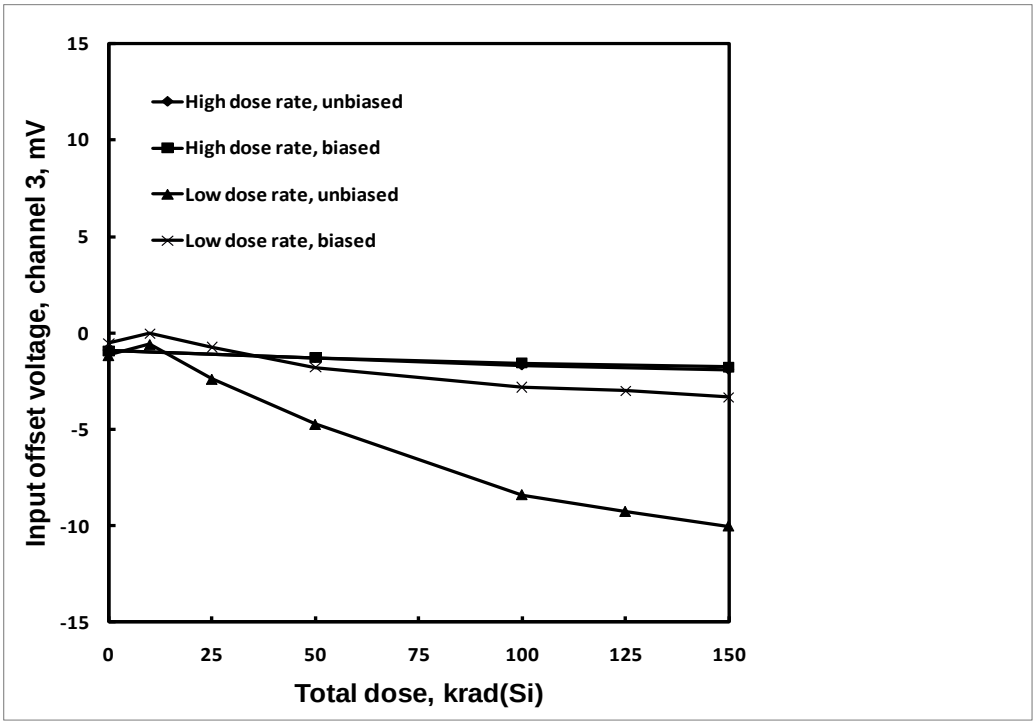

Figure 5: ISL7124SRH input offset voltage, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -10mV to +10mV.

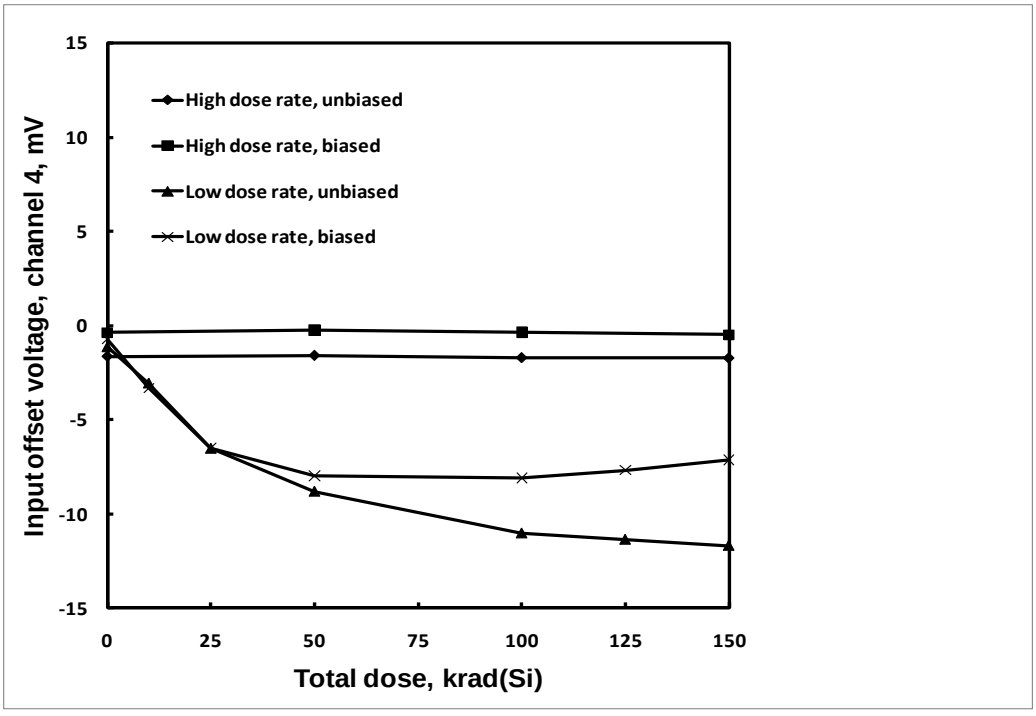

Figure 6: ISL7124SRH input offset voltage, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -10mV to +10mV.

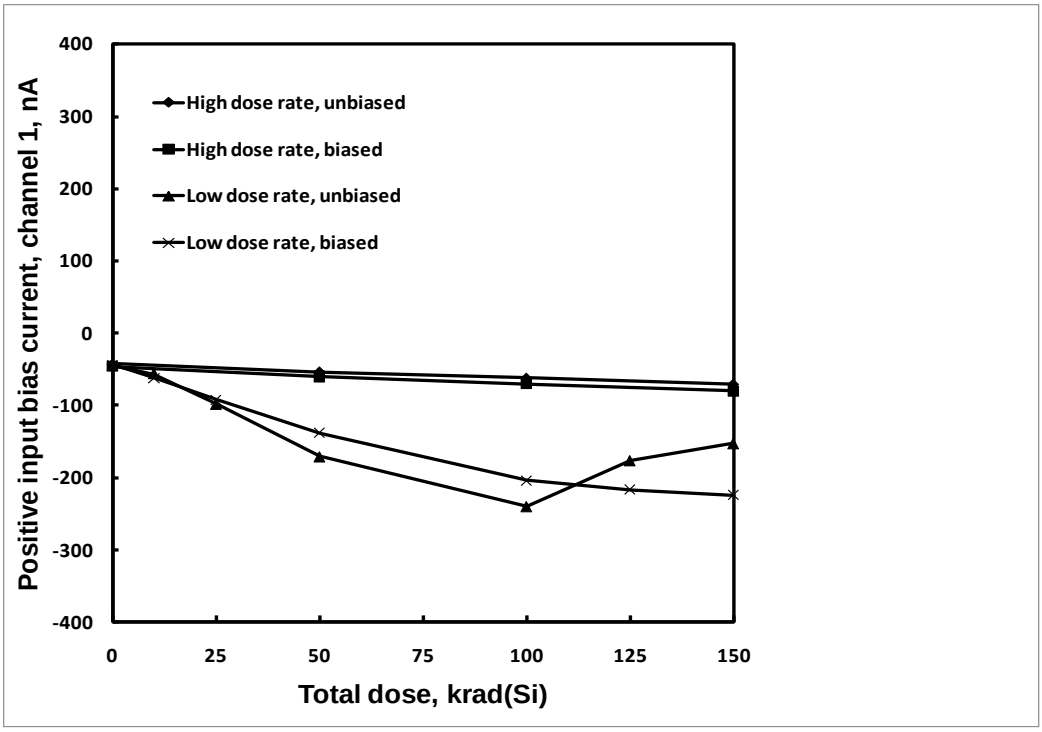

Figure 7: ISL7124SRH positive input bias current, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -400nA to +400nA.

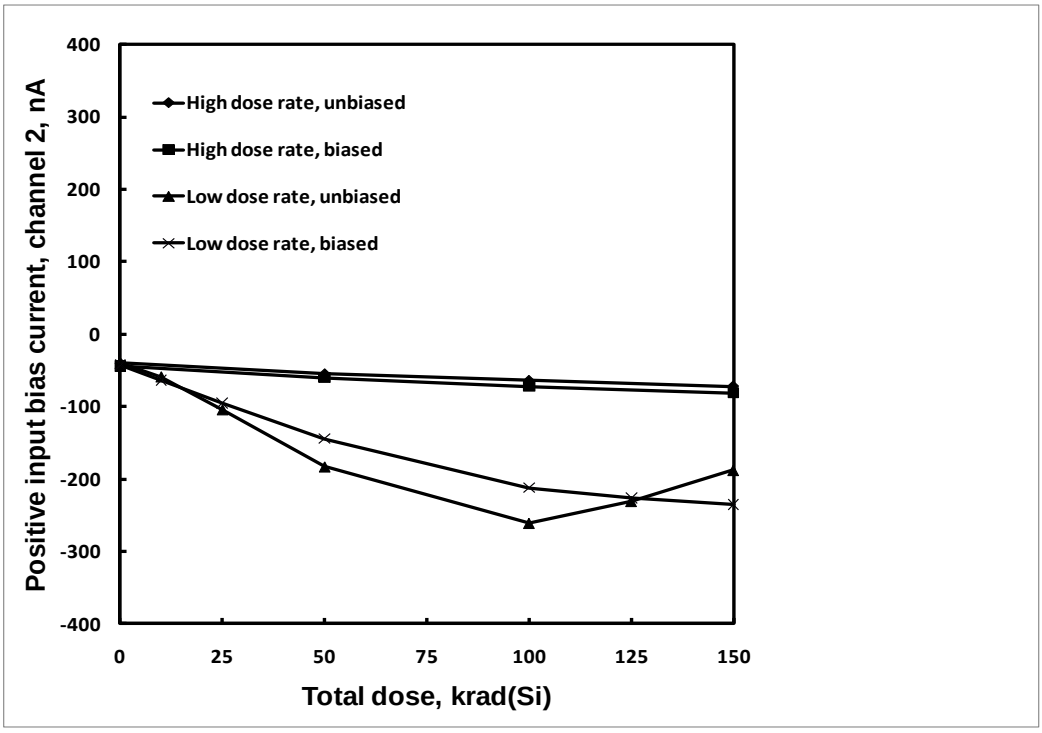

Figure 8: ISL7124SRH positive input bias current, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -400nA to +400nA.

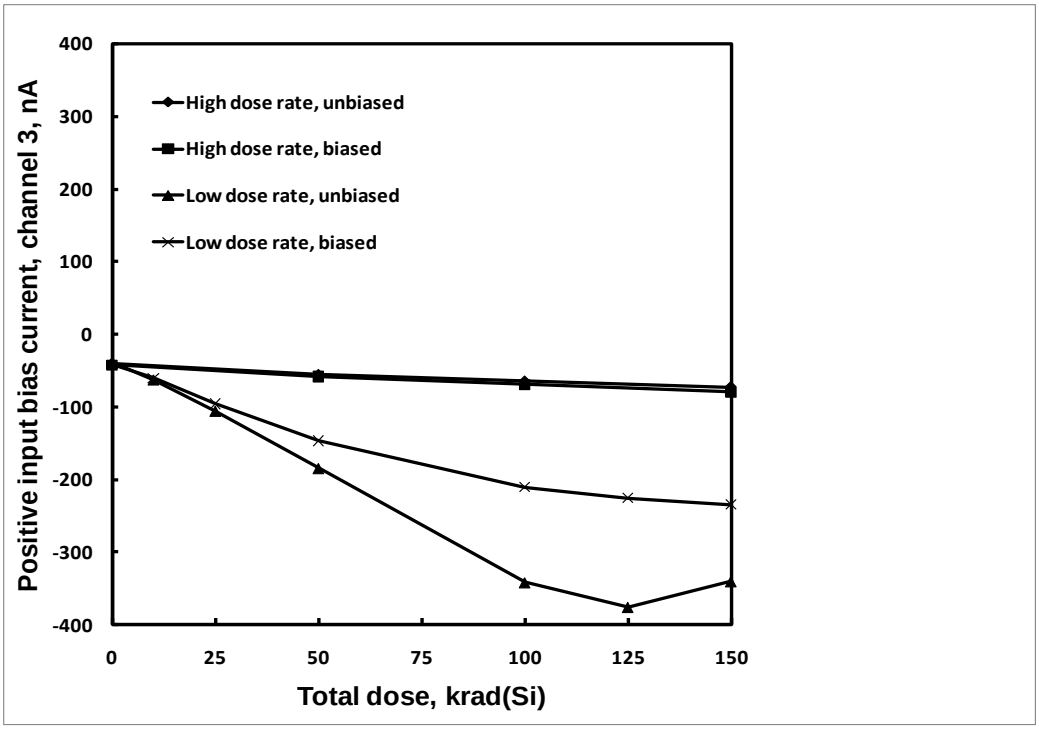

Figure 9: ISL7124SRH positive input bias current, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -400nA to +400nA.

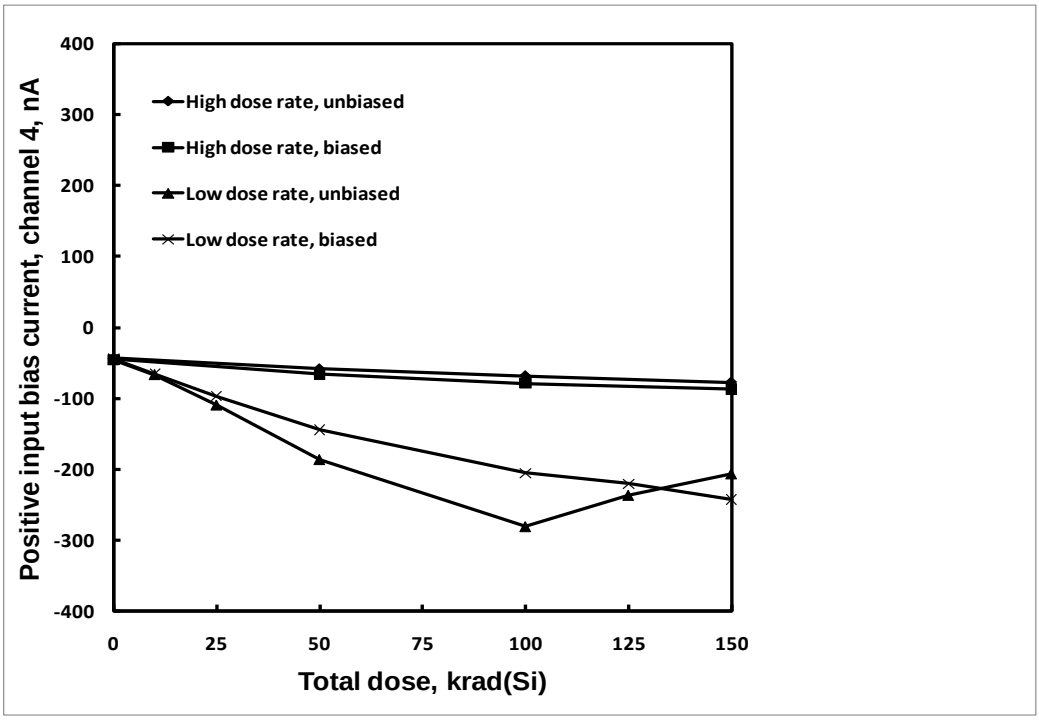

Figure 10: ISL7124SRH positive input bias current, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -400nA to +400nA.

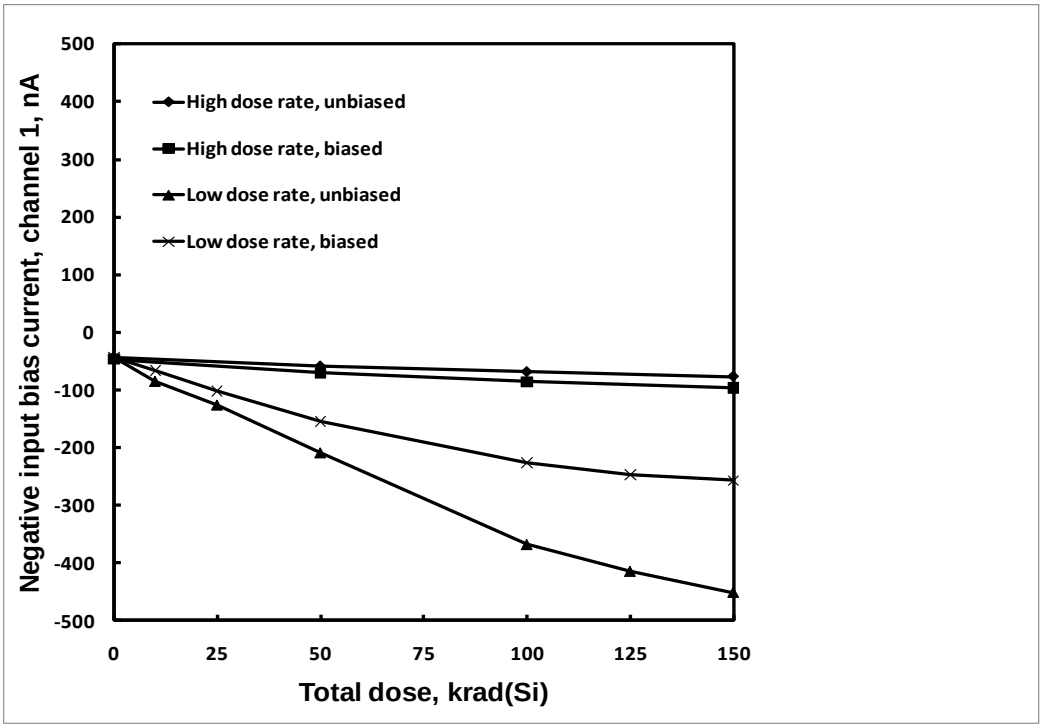

Figure 11: ISL7124SRH negative input bias current, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -400nA to +400nA.

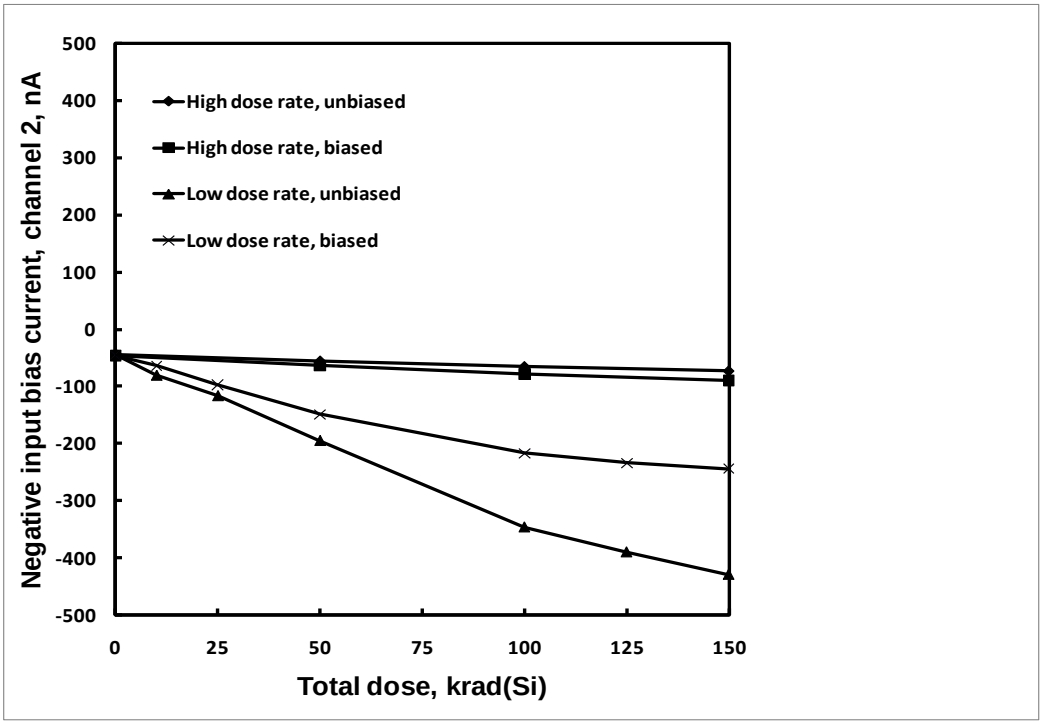

Figure 12: ISL7124SRH negative input bias current, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -400nA to +400nA.

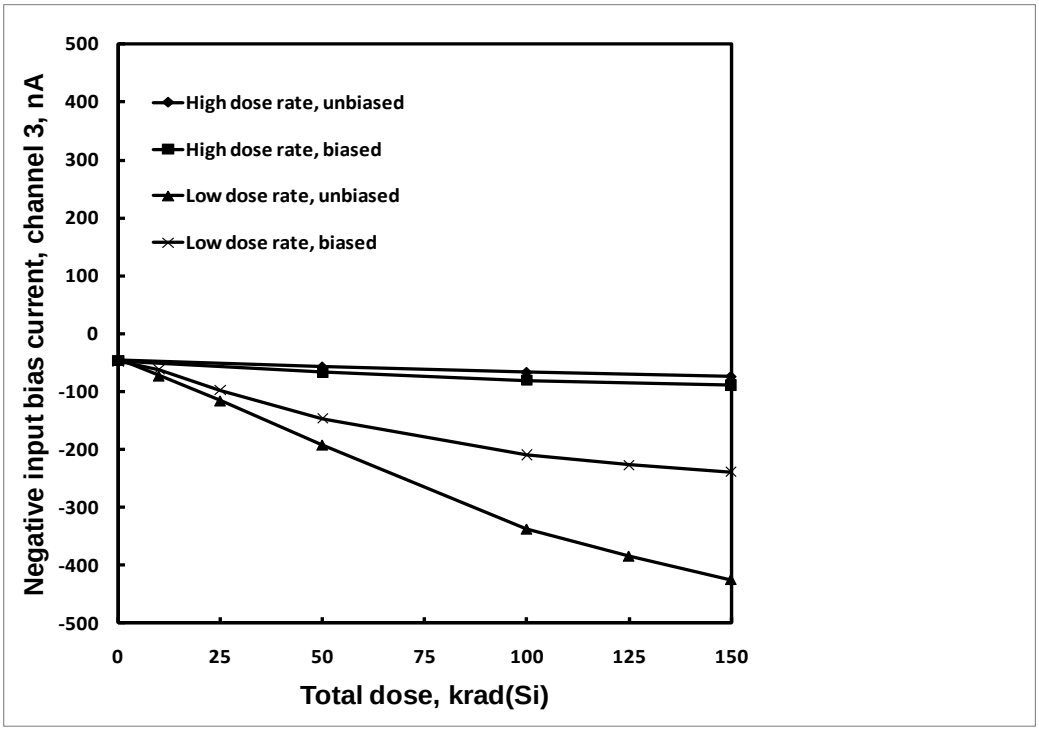

Figure 13: ISL7124SRH negative input bias current, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -400nA to +400nA.

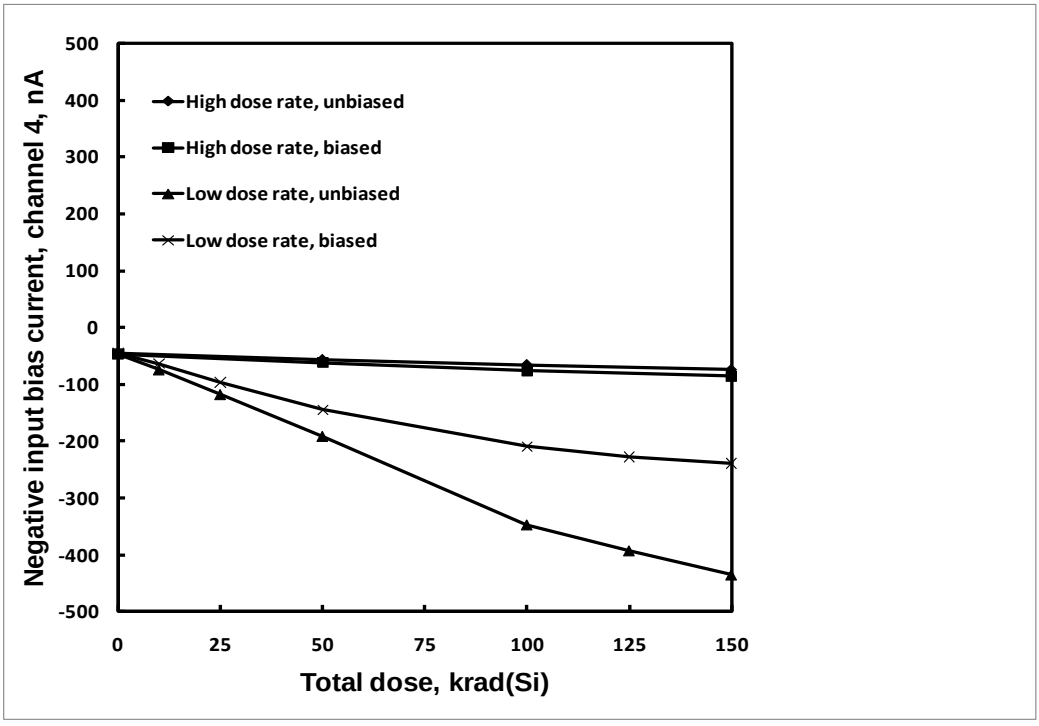

Figure 14: ISL7124SRH negative input bias current, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -400nA to +400nA.

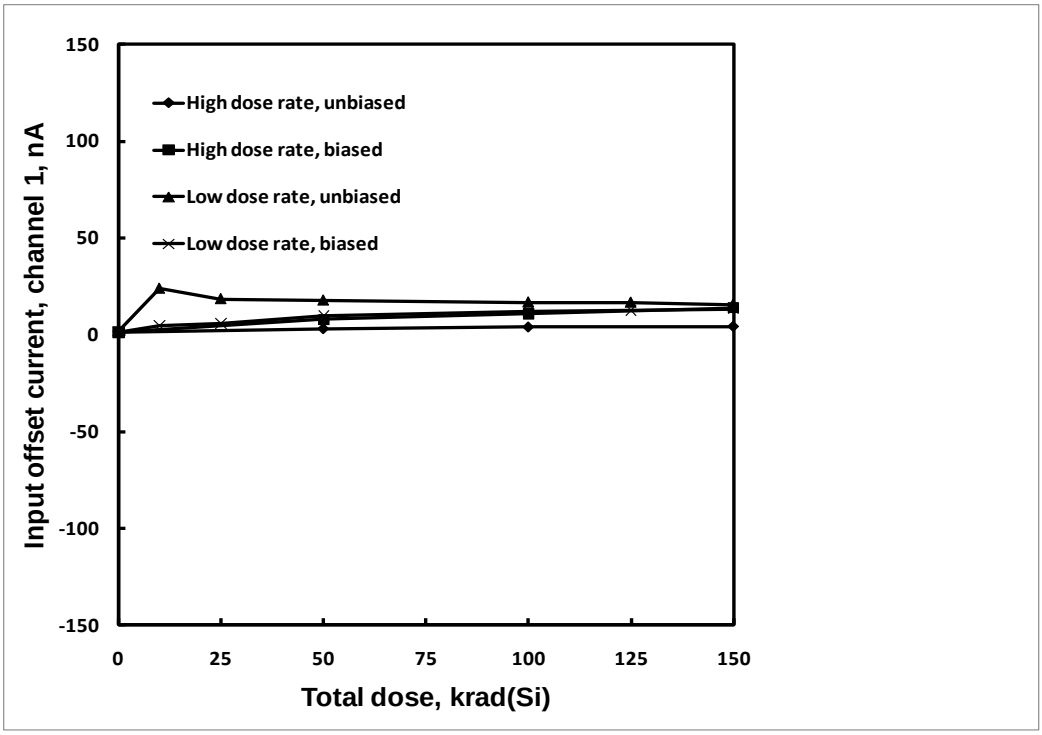

Figure 15: ISL7124SRH input offset current, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -150nA to +150nA.

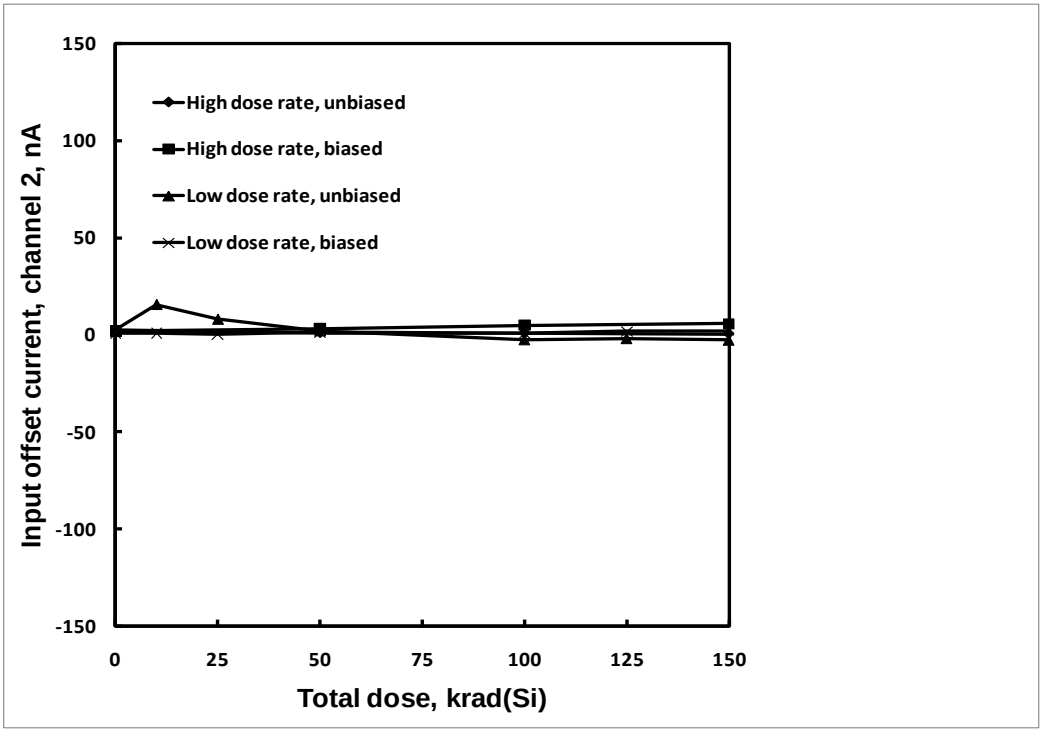

Figure 16: ISL7124SRH input offset current, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -150nA to +150nA.

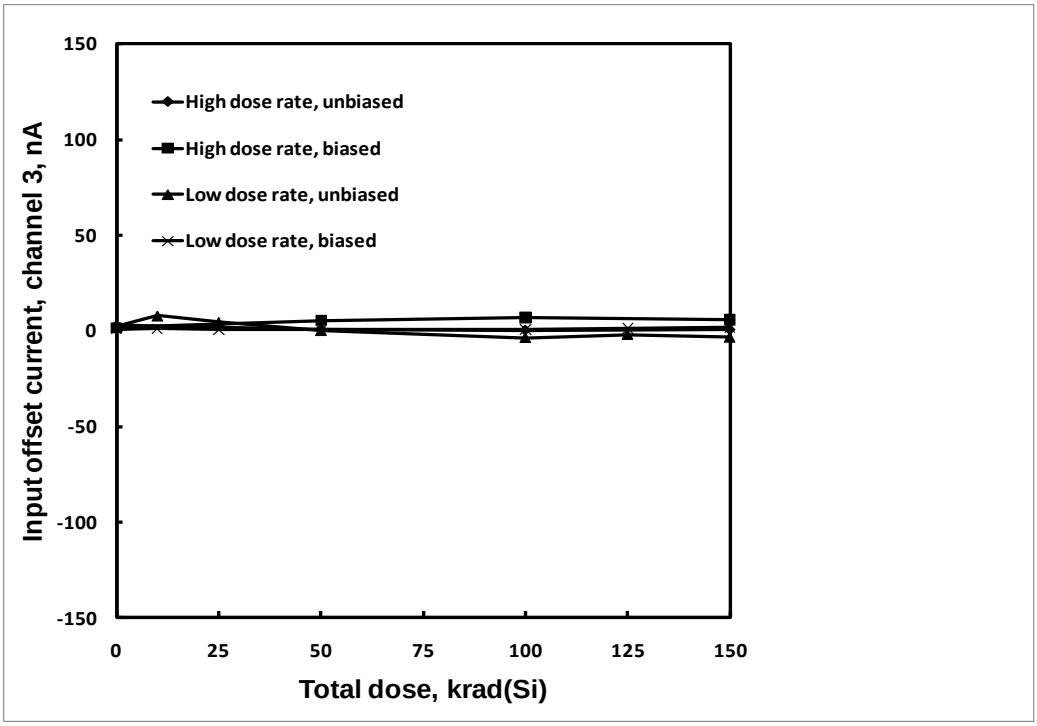

Figure 17: ISL7124SRH input offset current, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -150nA to +150nA.

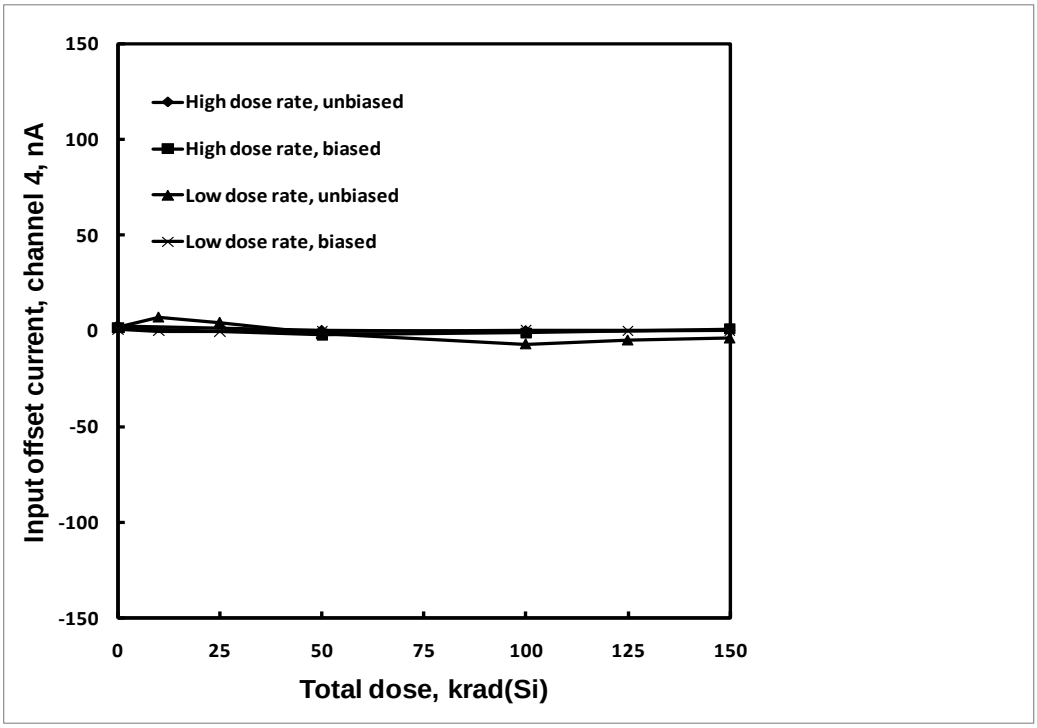

Figure 18: ISL7124SRH input offset current, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -150nA to +150nA.

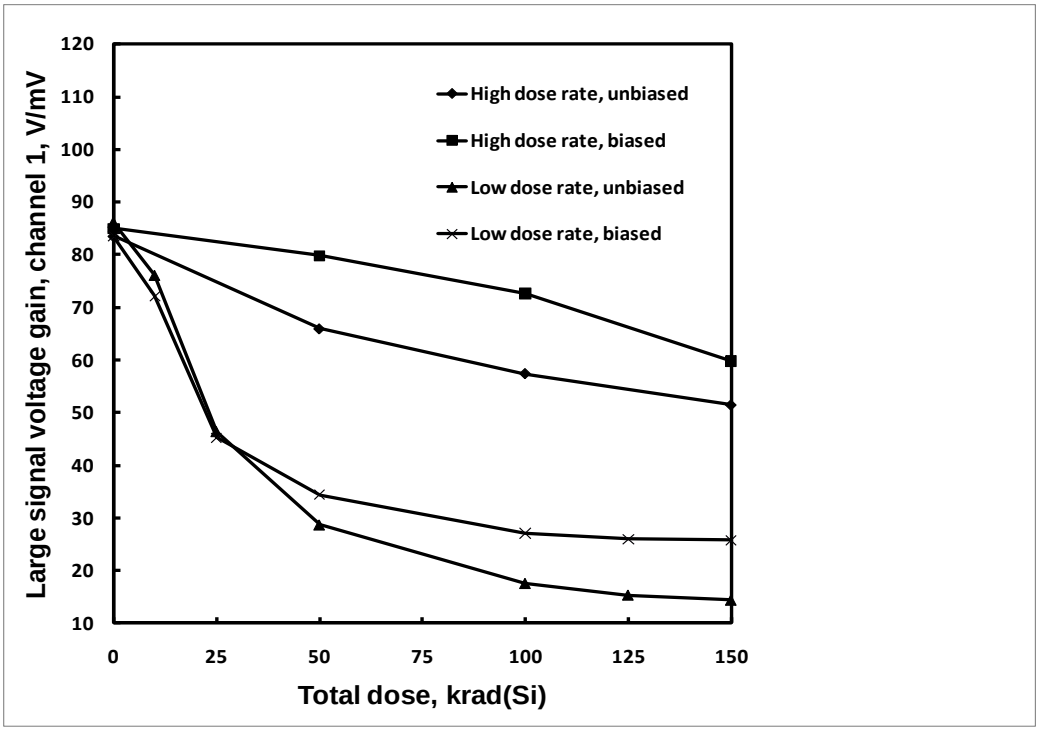

Figure 19: ISL7124SRH large signal open-loop voltage gain, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 20V/mV minimum (86dB).

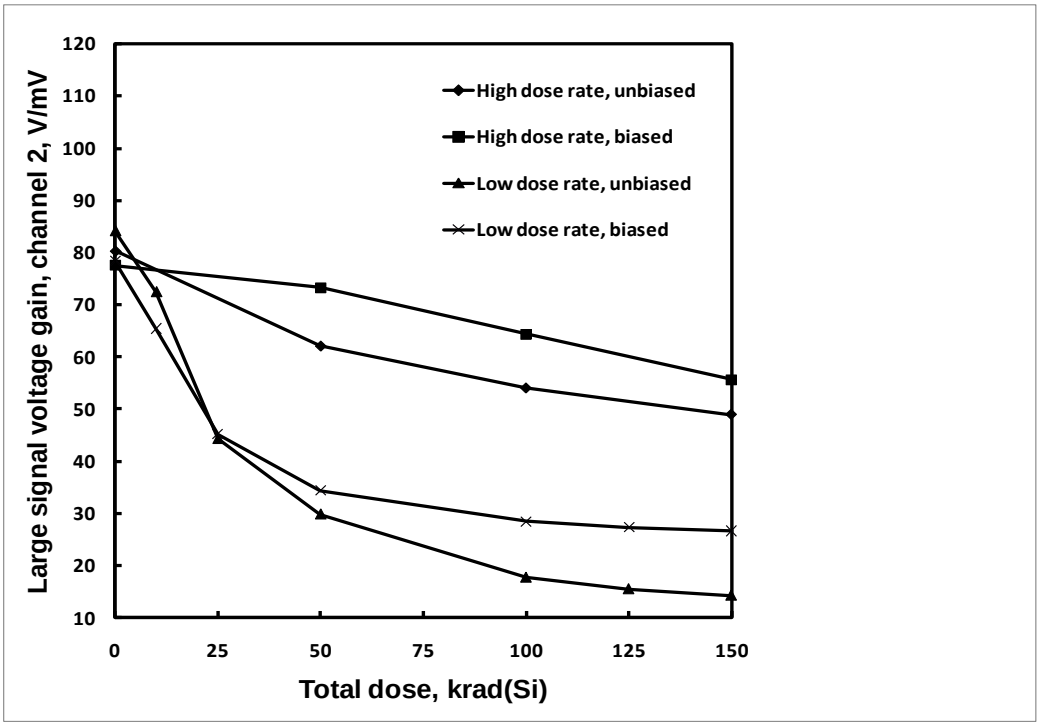

Figure 20: ISL7124SRH large signal open-loop voltage gain, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 20V/mV minimum (86dB).

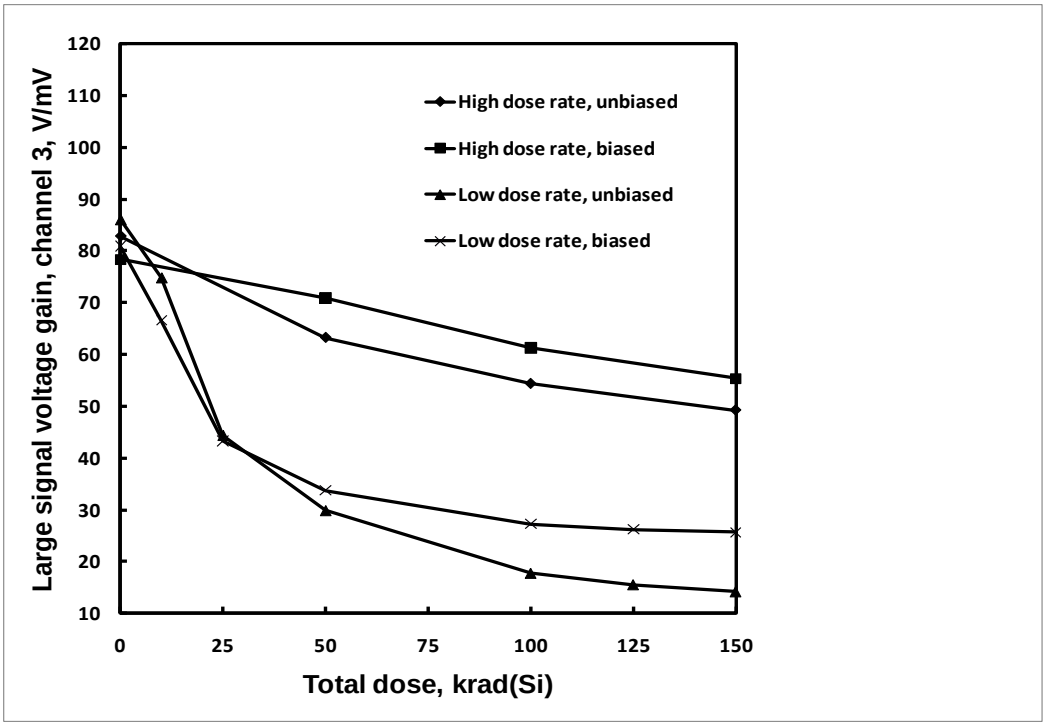

Figure 21: ISL7124SRH large signal open-loop voltage gain, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 20V/mV minimum (86dB).

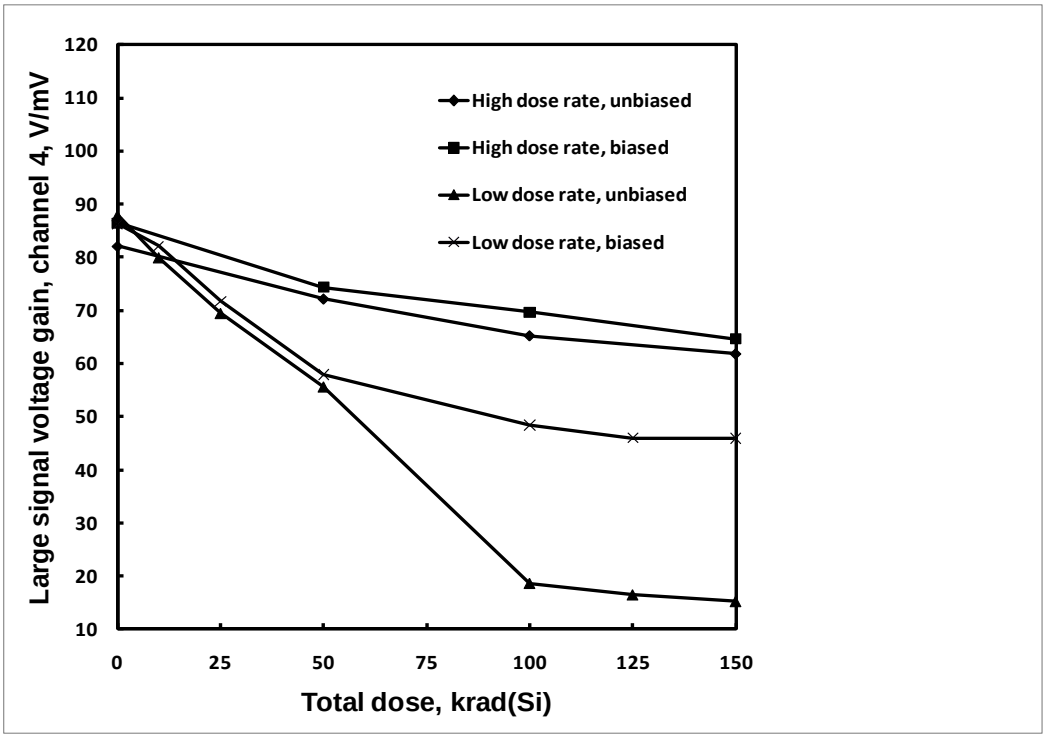

Figure 22: ISL7124SRH large signal open-loop voltage gain, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 20V/mV minimum (86dB).

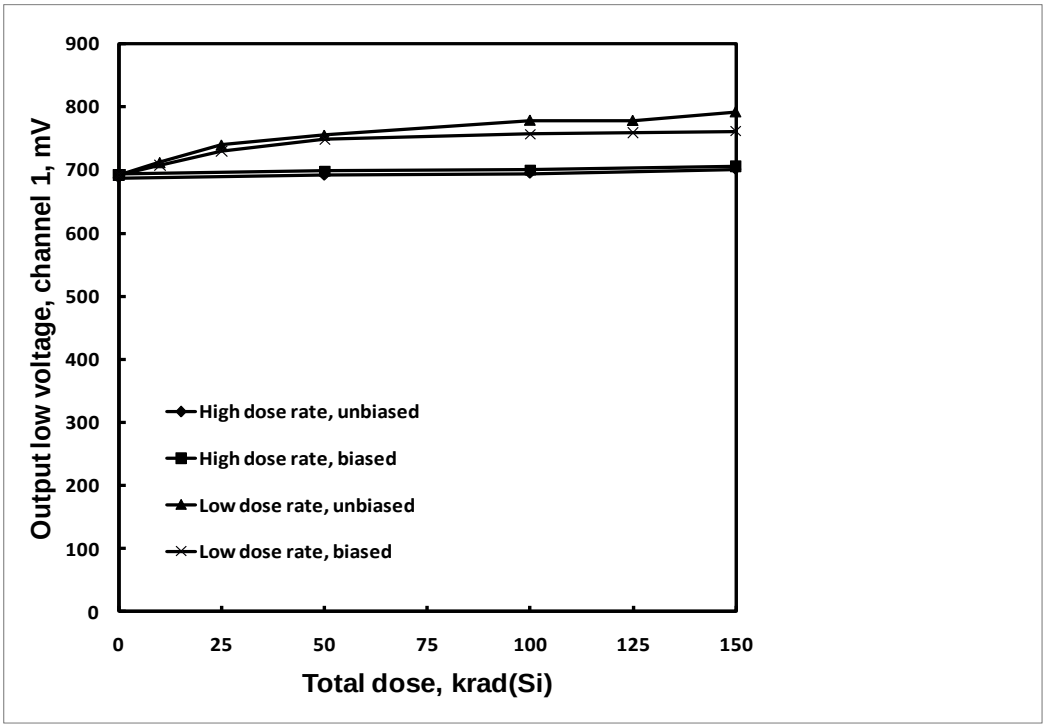

Figure 23: ISL7124SRH output low voltage, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 900mV maximum.

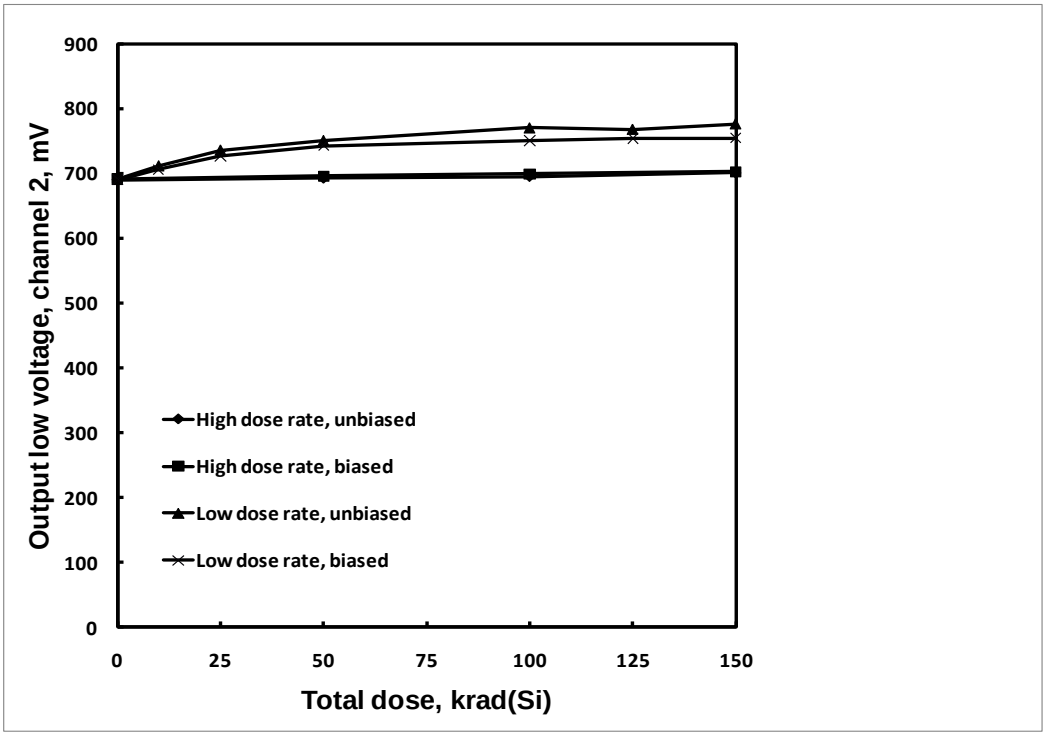

Figure 24: ISL7124SRH output low voltage, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 900mV maximum.

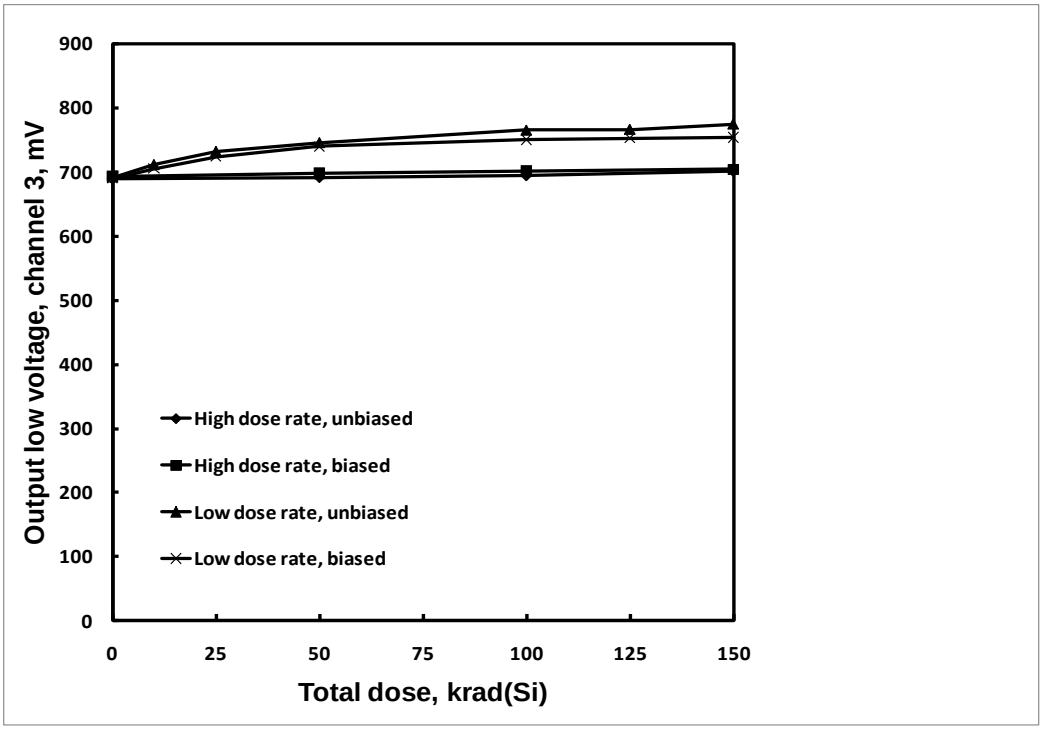

Figure 25: ISL7124SRH output low voltage, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 900mV maximum.

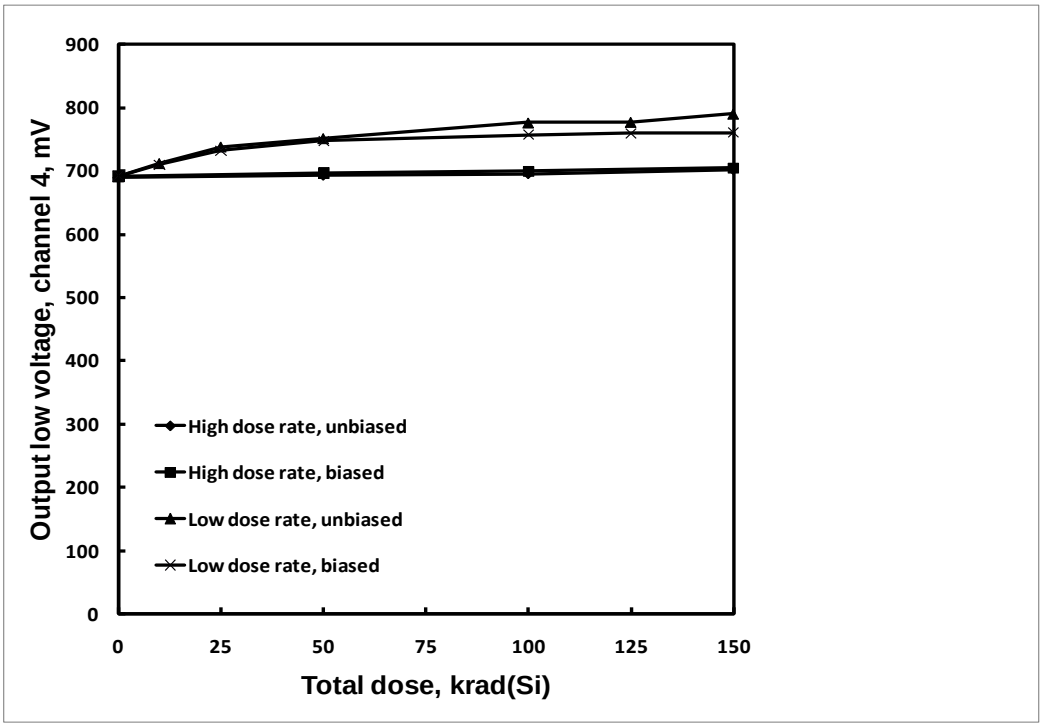

Figure 26: ISL7124SRH output low voltage, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 900mV maximum.

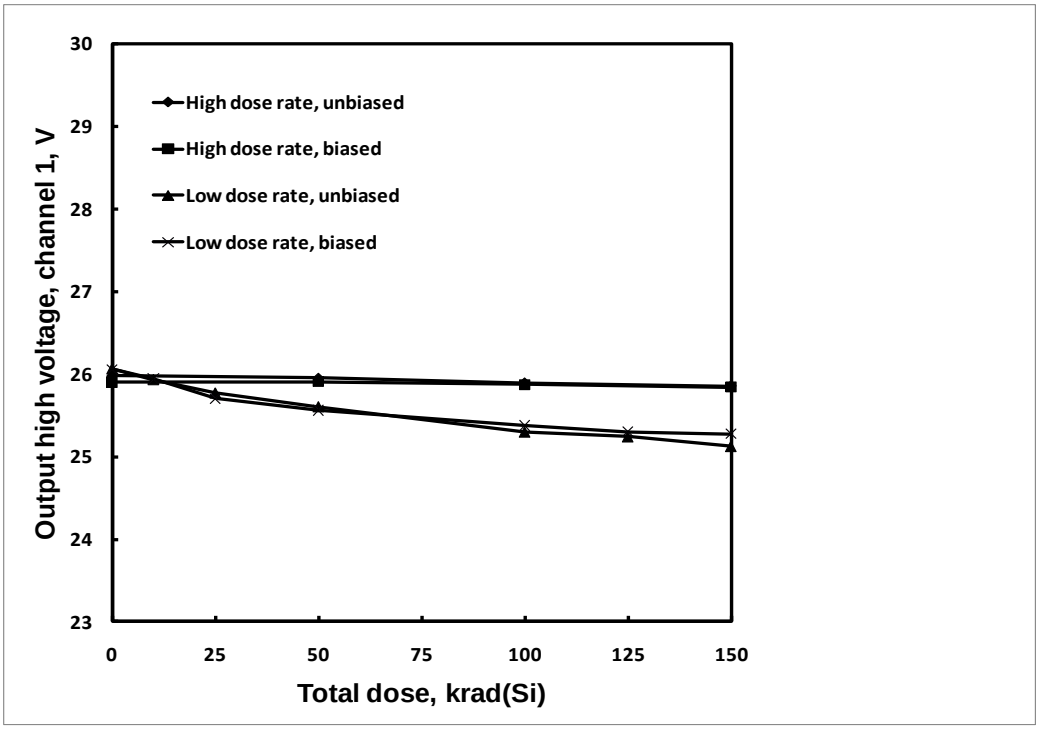

Figure 27: ISL7124SRH output high voltage, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 23V minimum.

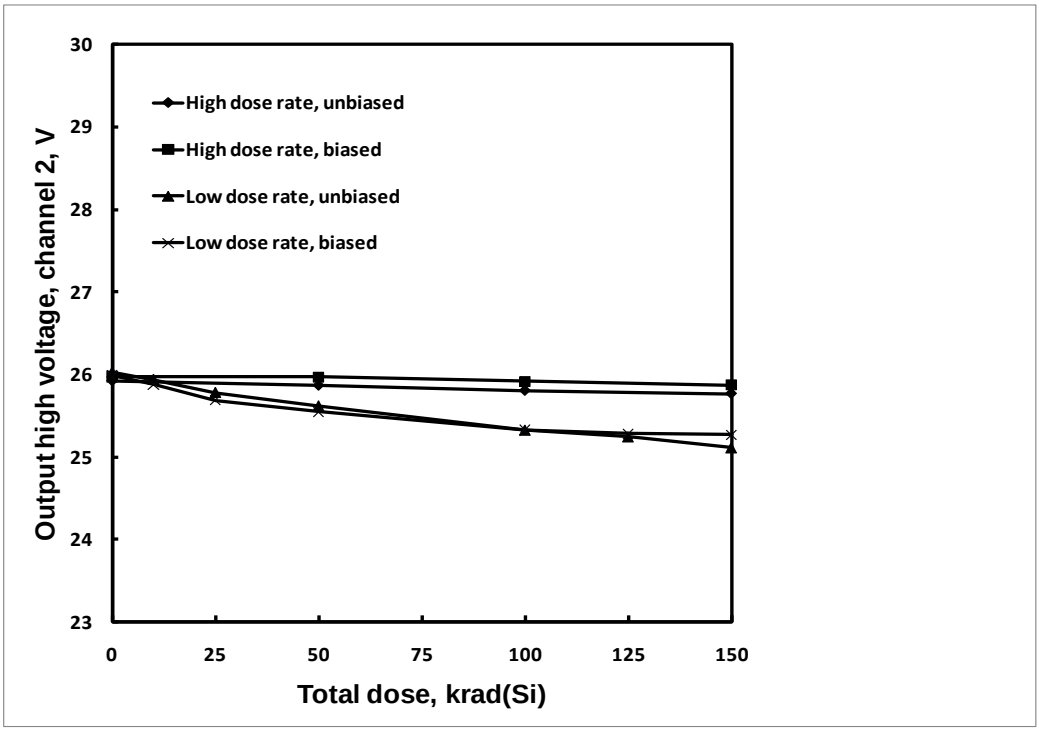

Figure 28: ISL7124SRH output high voltage, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 23V minimum.

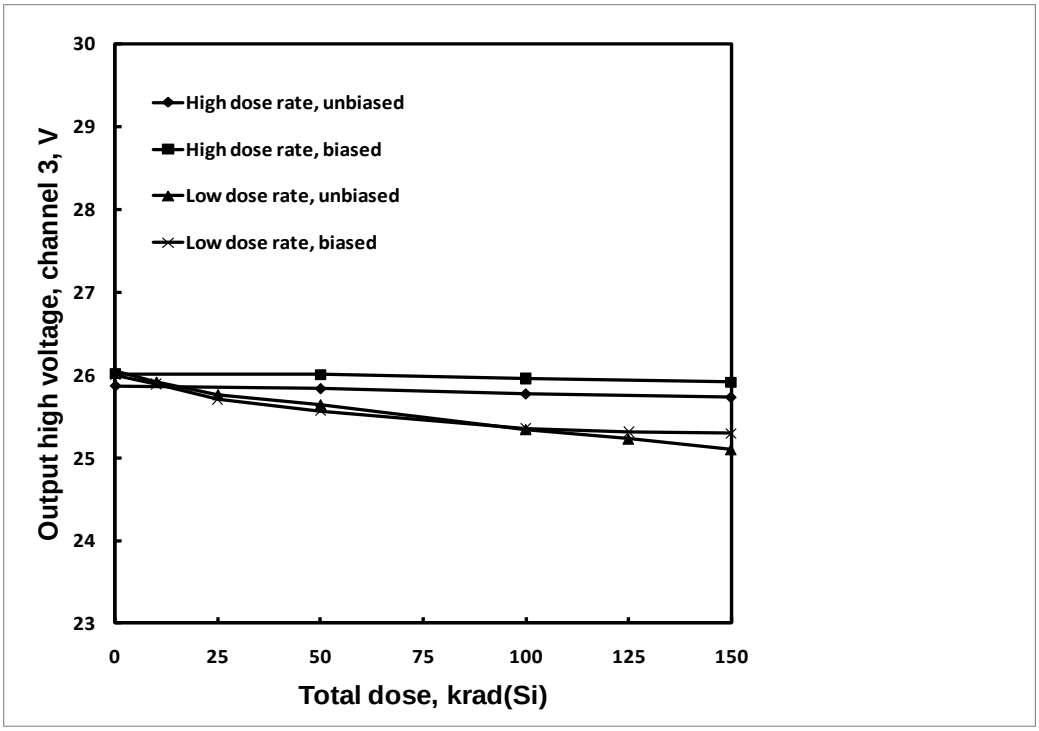

Figure 29: ISL7124SRH output high voltage, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 23V minimum.

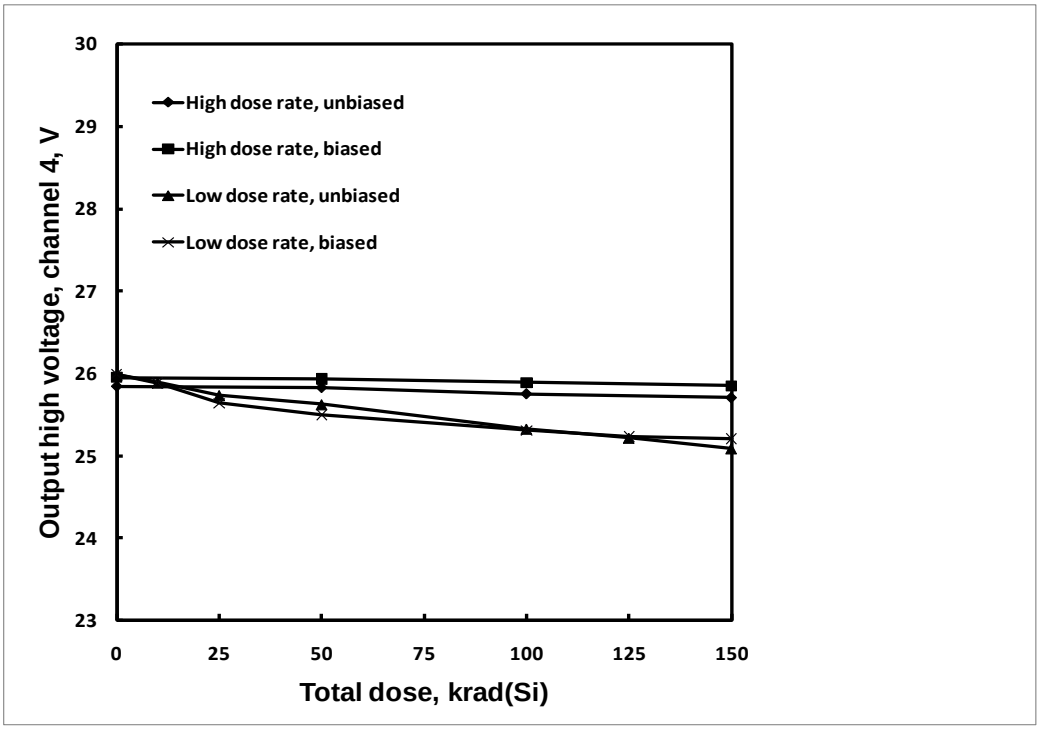

Figure 30: ISL7124SRH output high voltage, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 23V minimum.

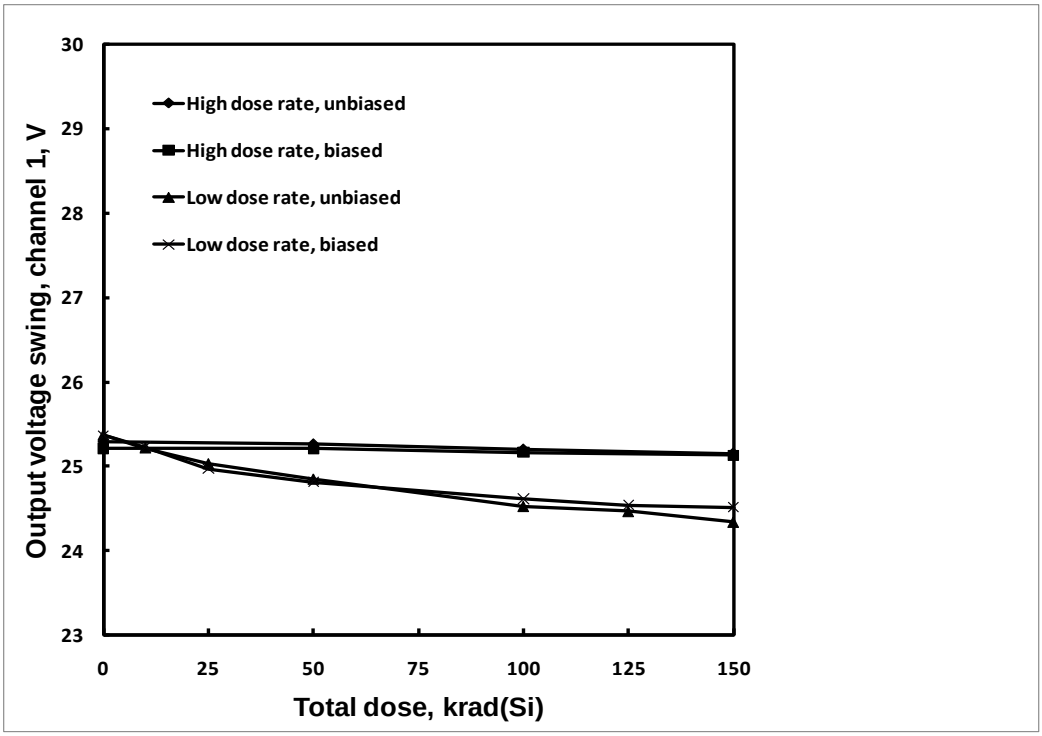

Figure 31: ISL7124SRH output voltage swing, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 22V minimum.

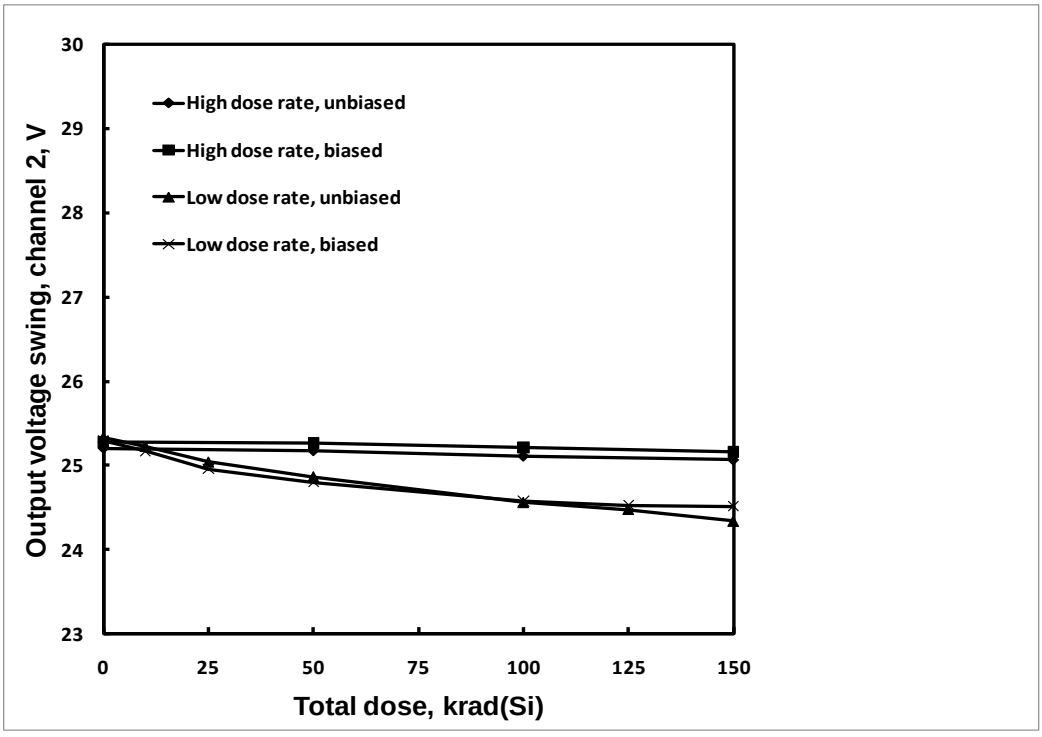

Figure 32: ISL7124SRH output voltage swing, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 22V minimum.

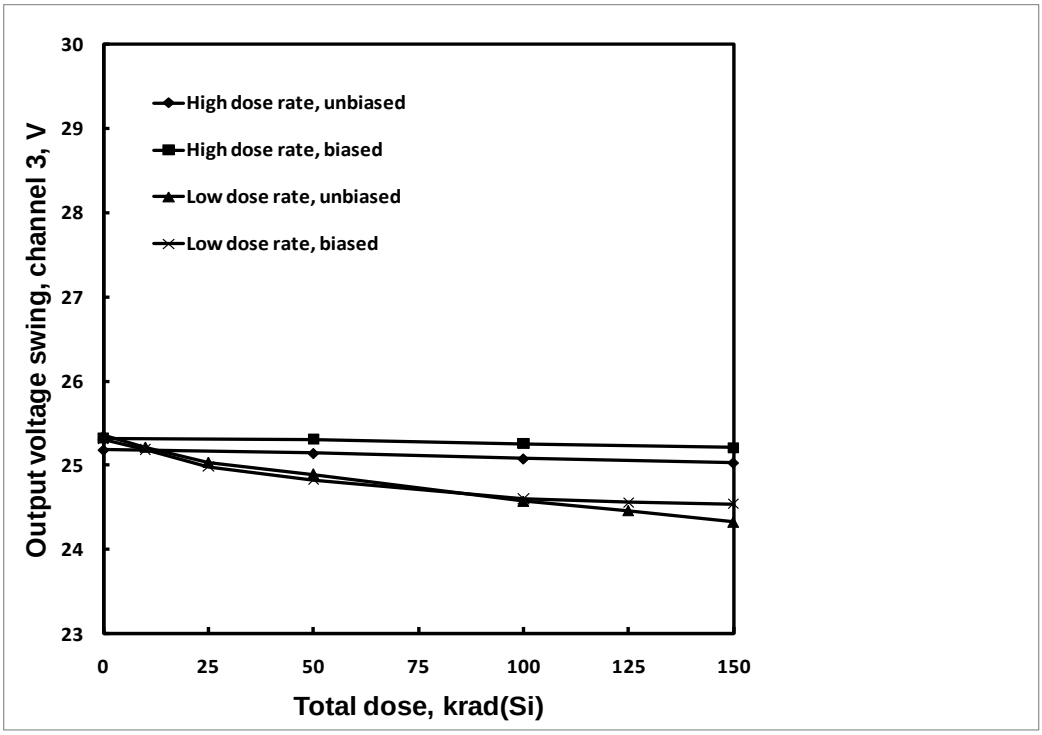

Figure 33: ISL7124SRH output voltage swing, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 22V minimum.

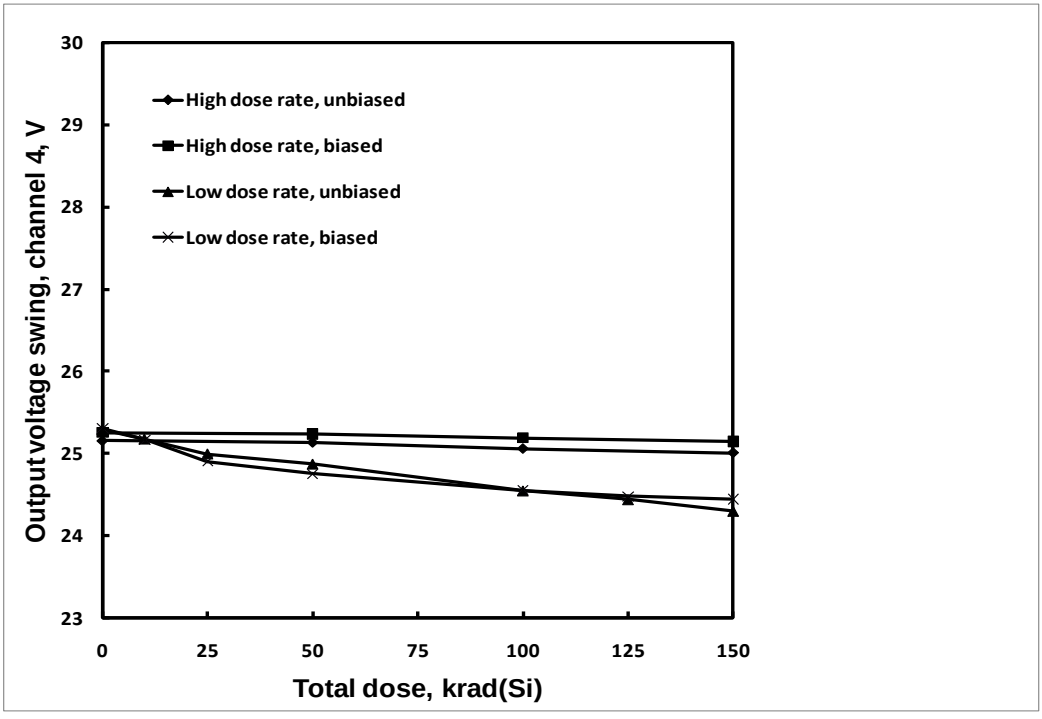

Figure 34: ISL7124SRH output voltage swing, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 22V minimum.

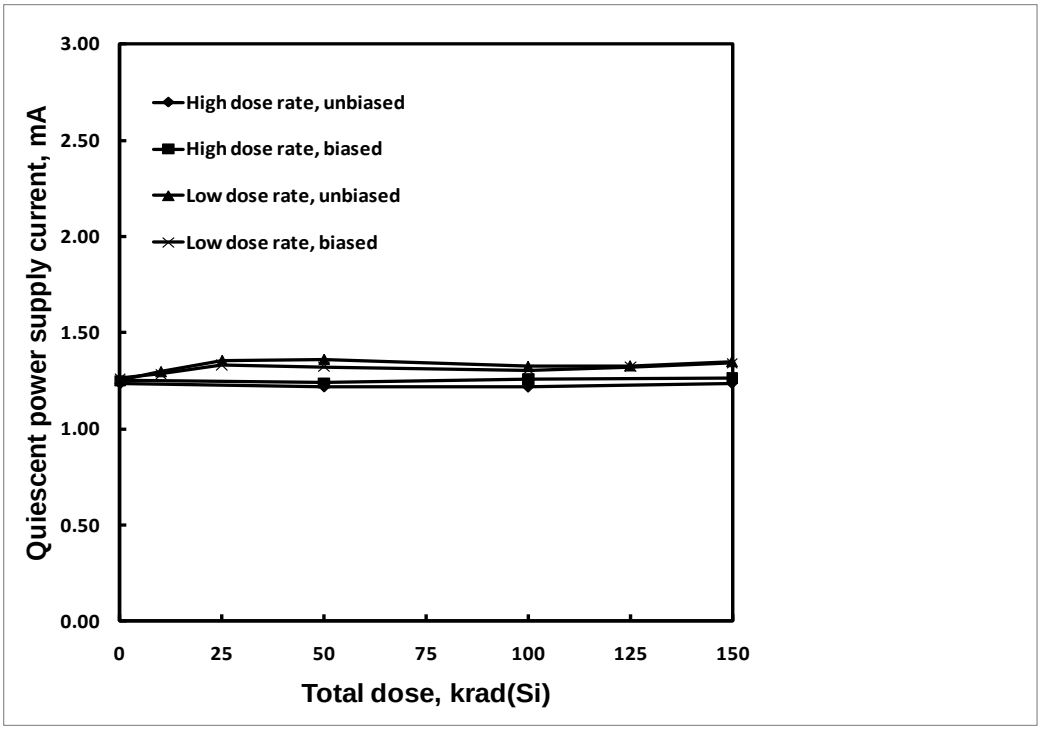

Figure 35: ISL7124SRH quiescent power supply current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 3mA maximum.

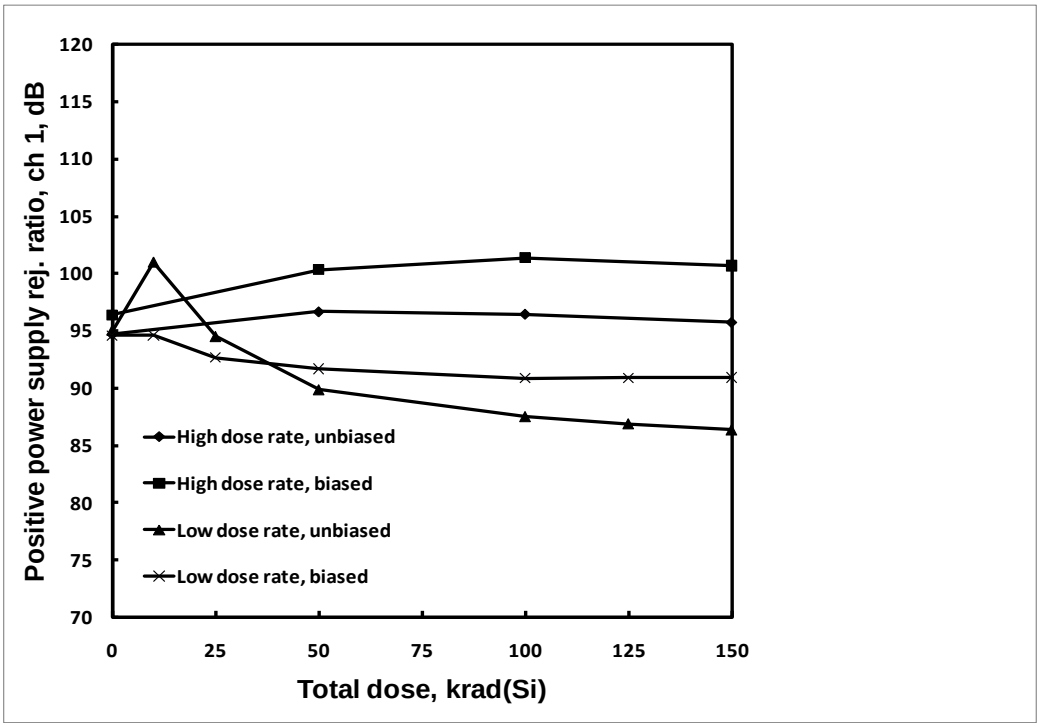

Figure 36: ISL7124SRH positive power supply rejection ratio, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 70dB minimum.

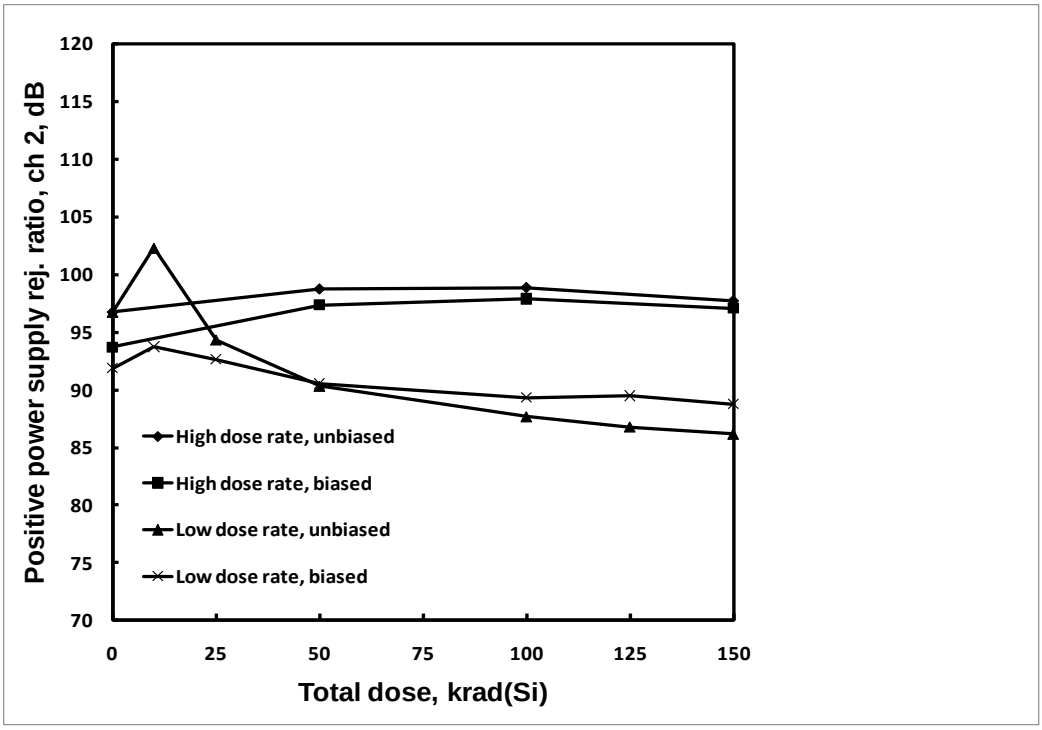

Figure 37: ISL7124SRH positive power supply rejection ratio, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 70dB minimum.

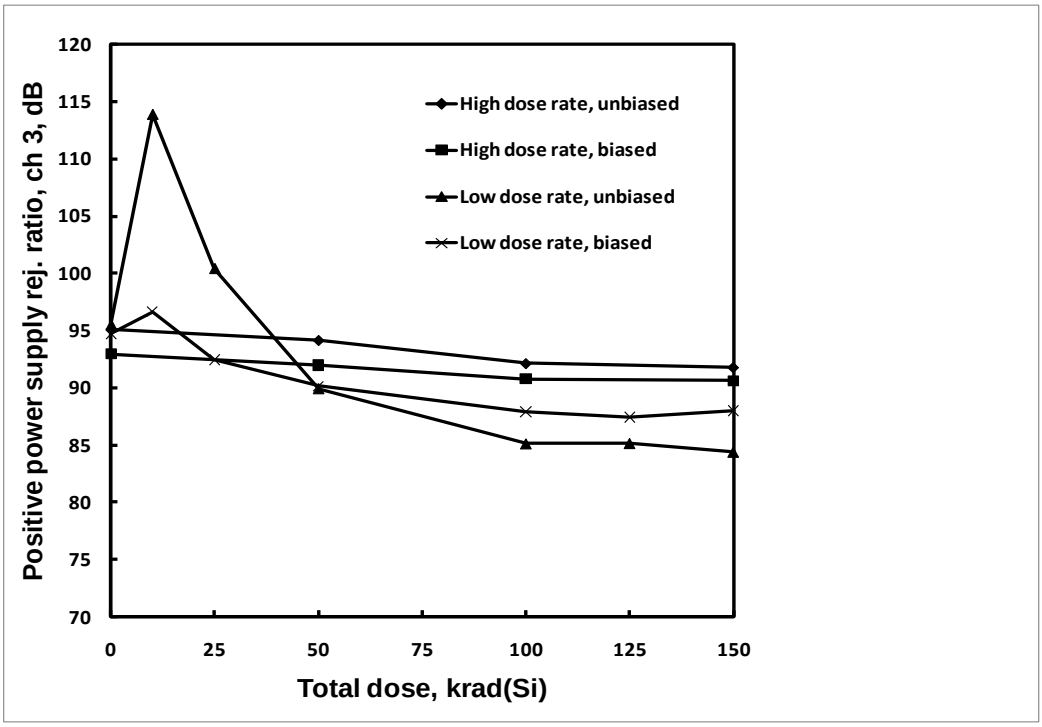

Figure 38: ISL7124SRH positive power supply rejection ratio, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 70dB minimum.

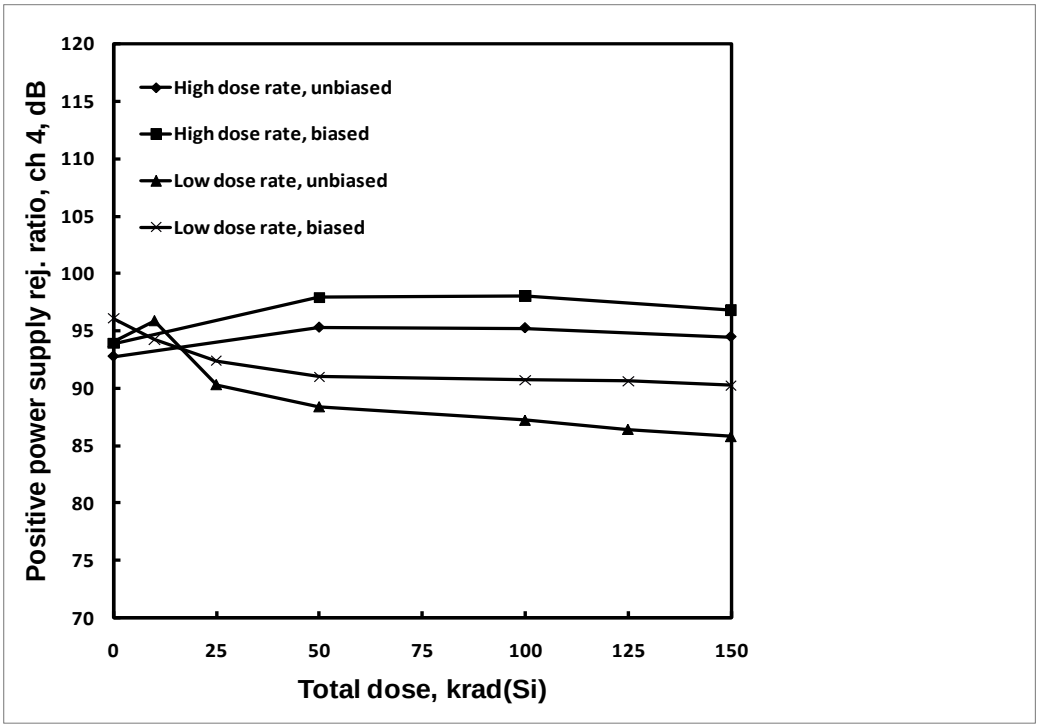

Figure 39: ISL7124SRH positive power supply rejection ratio, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 70dB minimum.

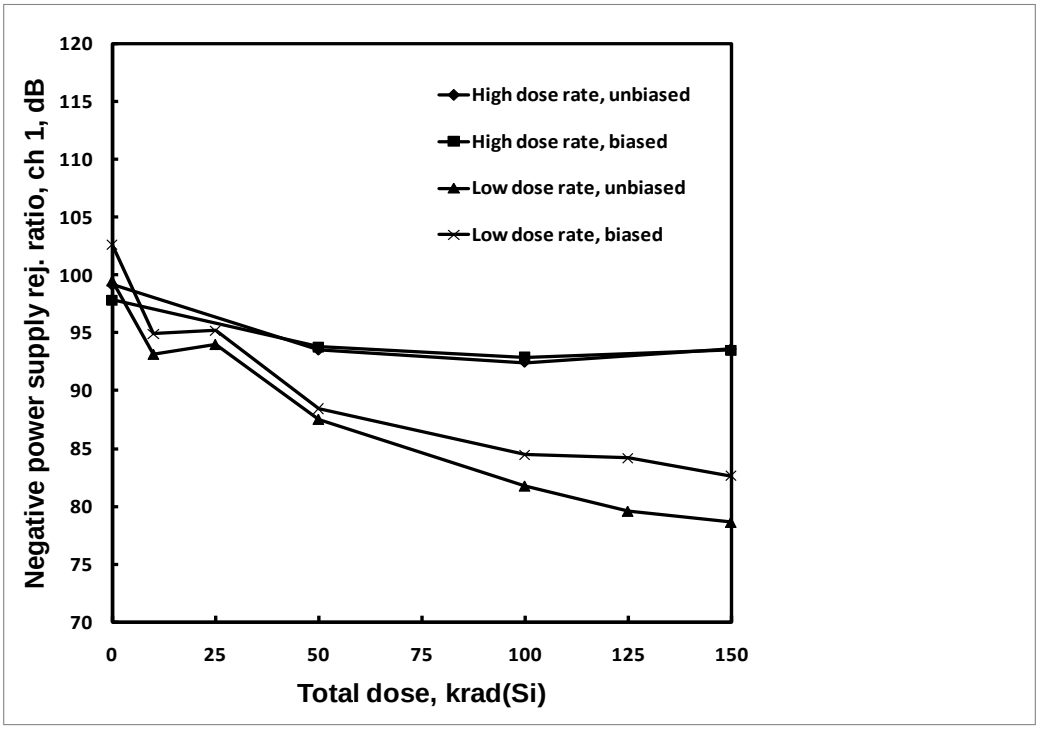

Figure 40: ISL7124SRH negative power supply rejection ratio, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 70dB minimum.

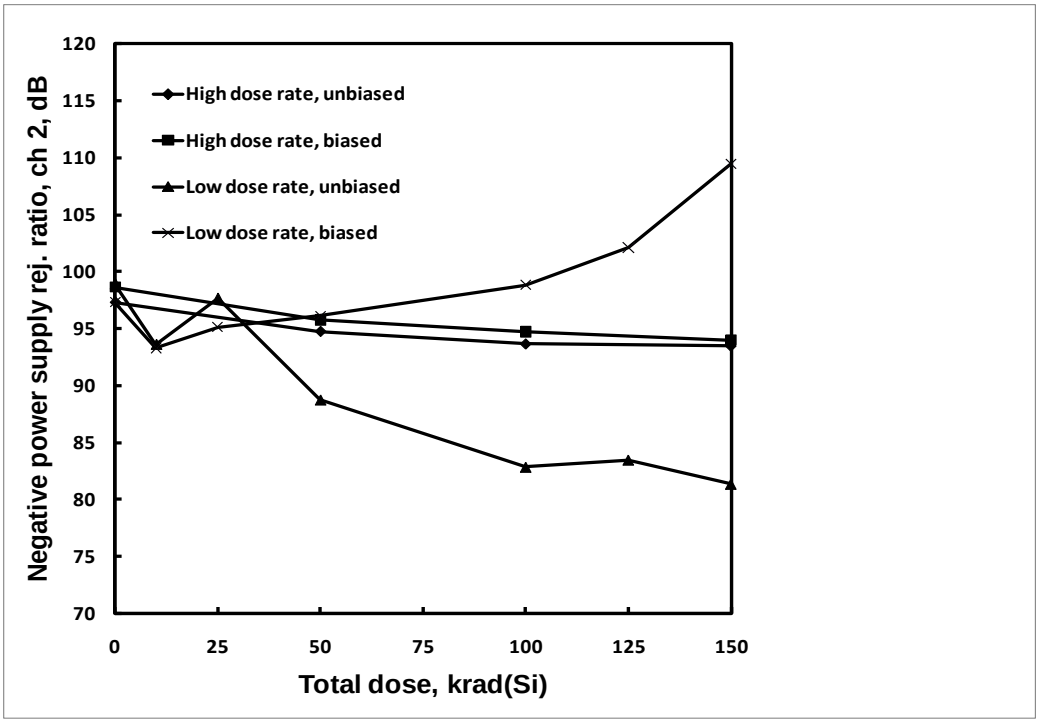

Figure 41: ISL7124SRH negative power supply rejection ratio, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 70dB minimum.

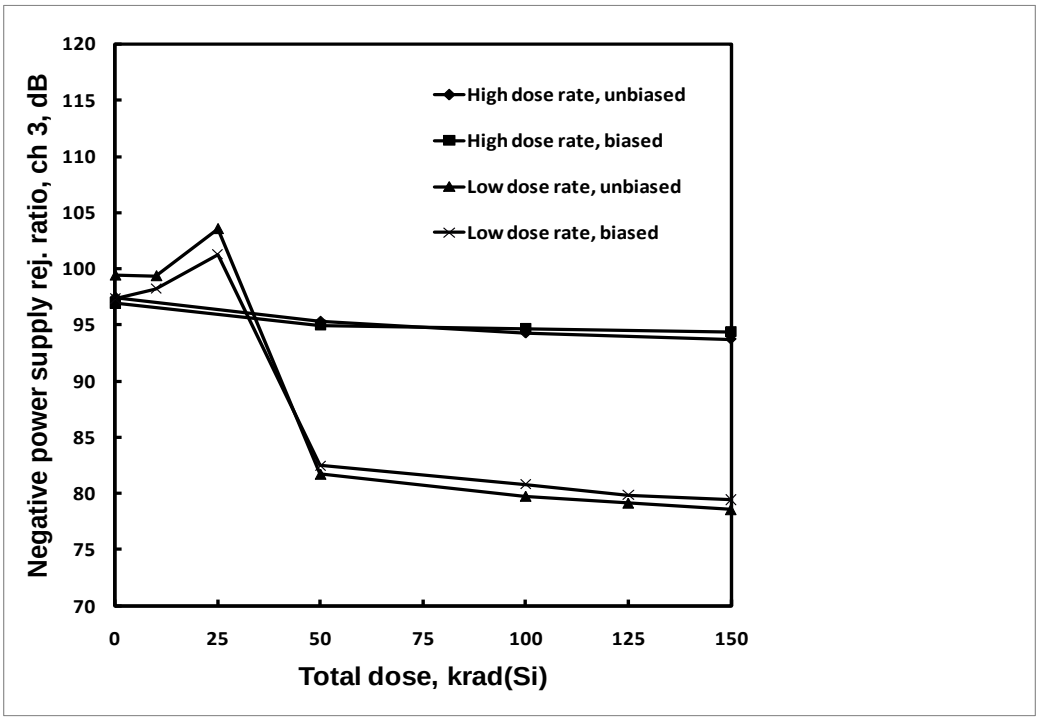

Figure 42: ISL7124SRH negative power supply rejection ratio, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 70dB minimum.

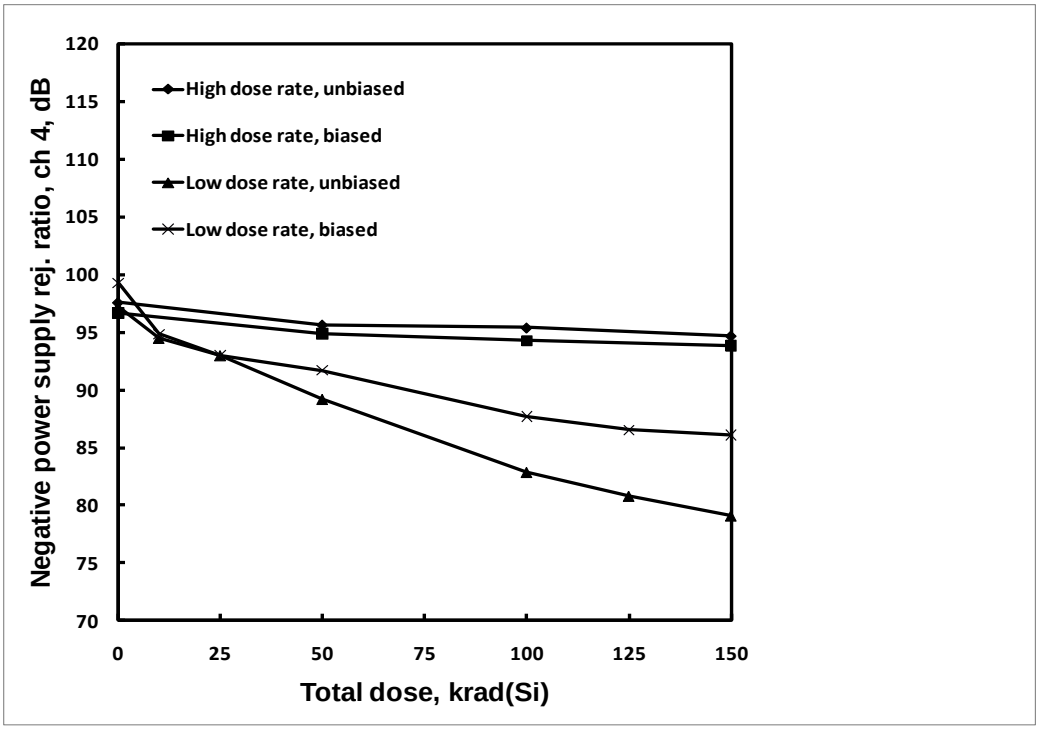

Figure 43: ISL7124SRH negative power supply rejection ratio, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 70dB minimum.

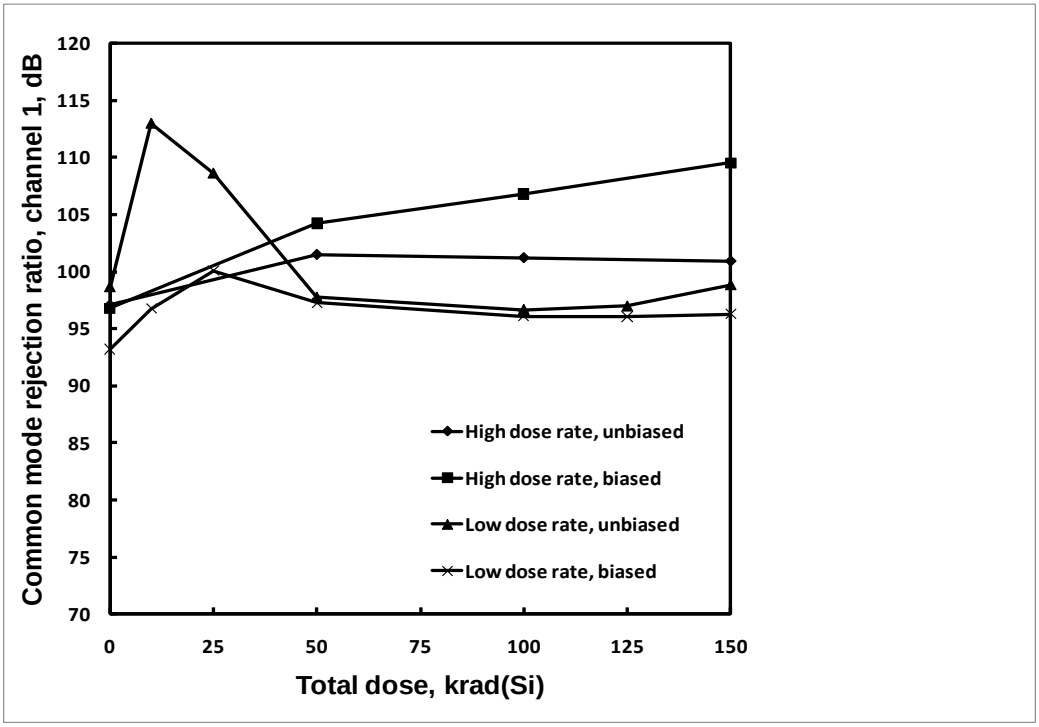

Figure 44: ISL7124SRH common mode rejection ratio, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 70dB minimum.

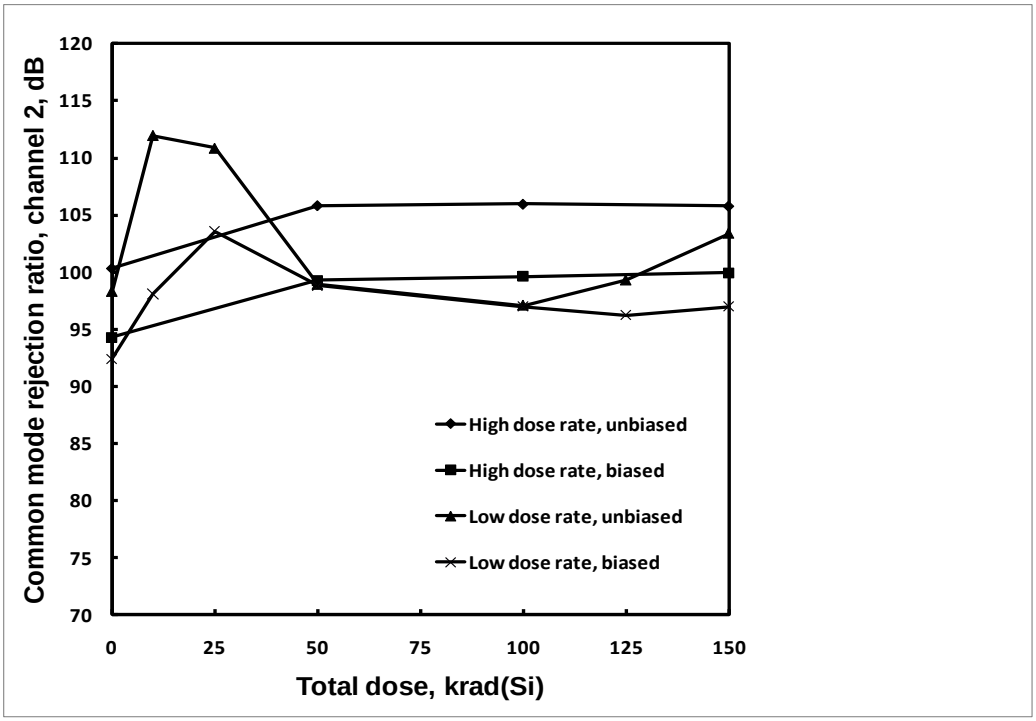

Figure 45: ISL7124SRH common mode rejection ratio, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 70dB minimum.

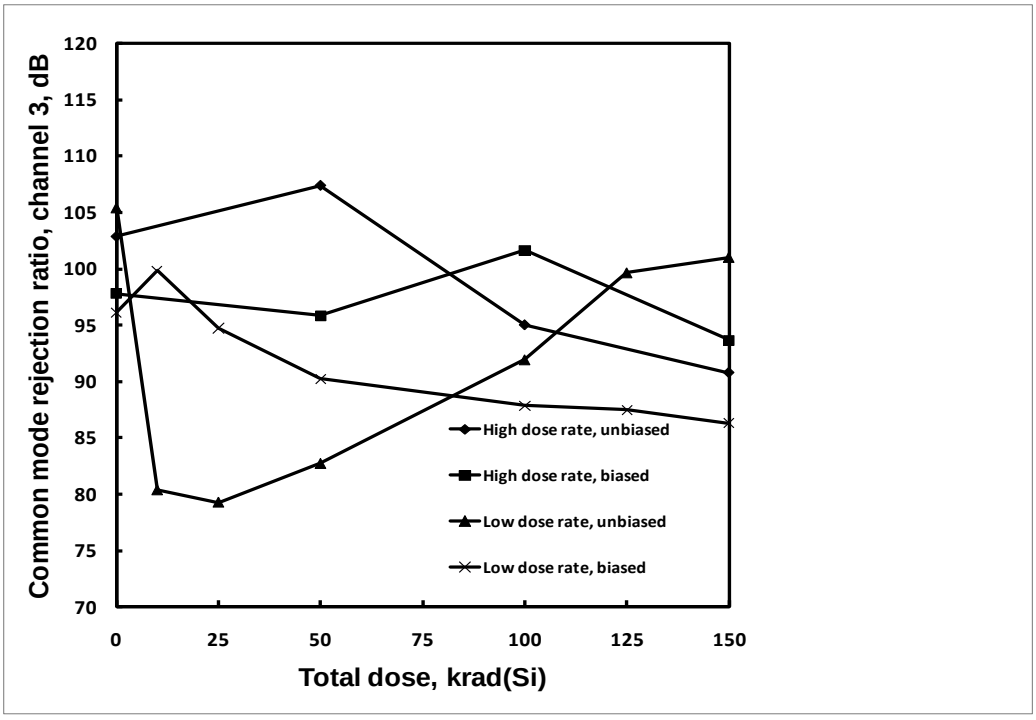

Figure 46: ISL7124SRH common mode rejection ratio, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 70dB minimum.

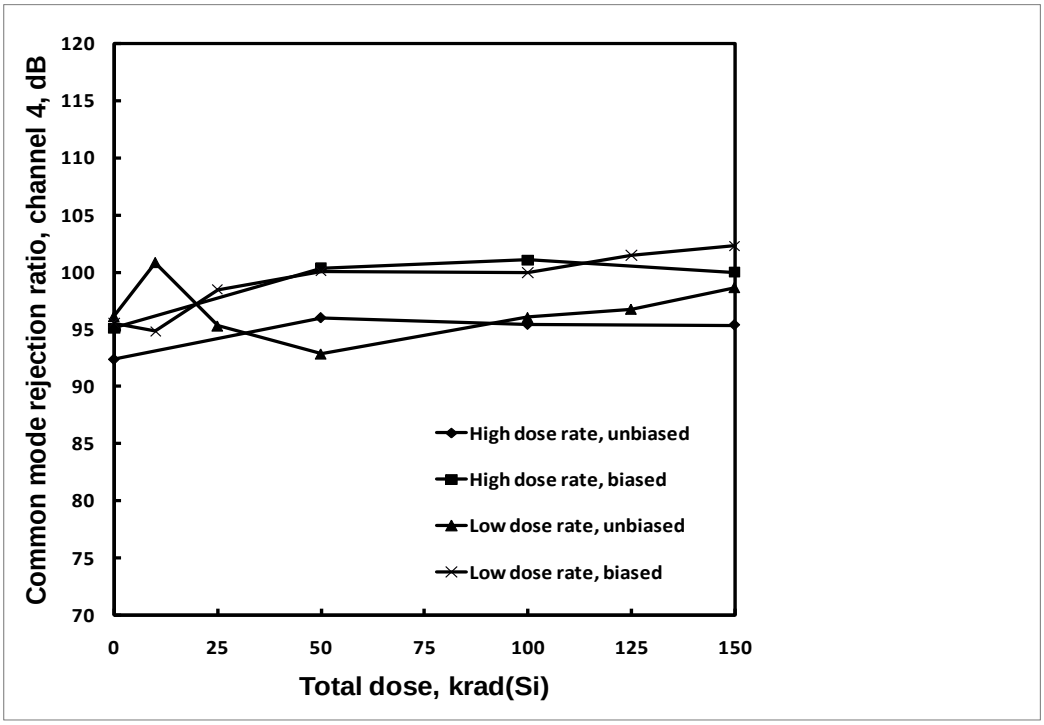

Figure 47: ISL7124SRH common mode rejection ratio, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 70dB minimum.

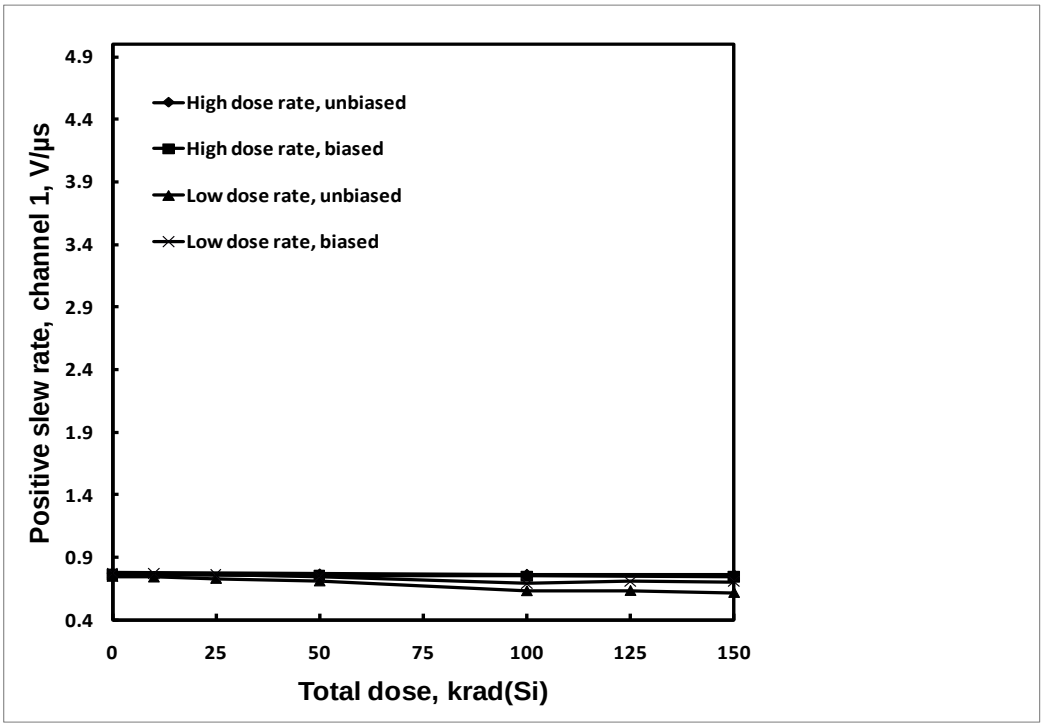

Figure 48: ISL7124SRH positive slew rate, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is .4V/µs.

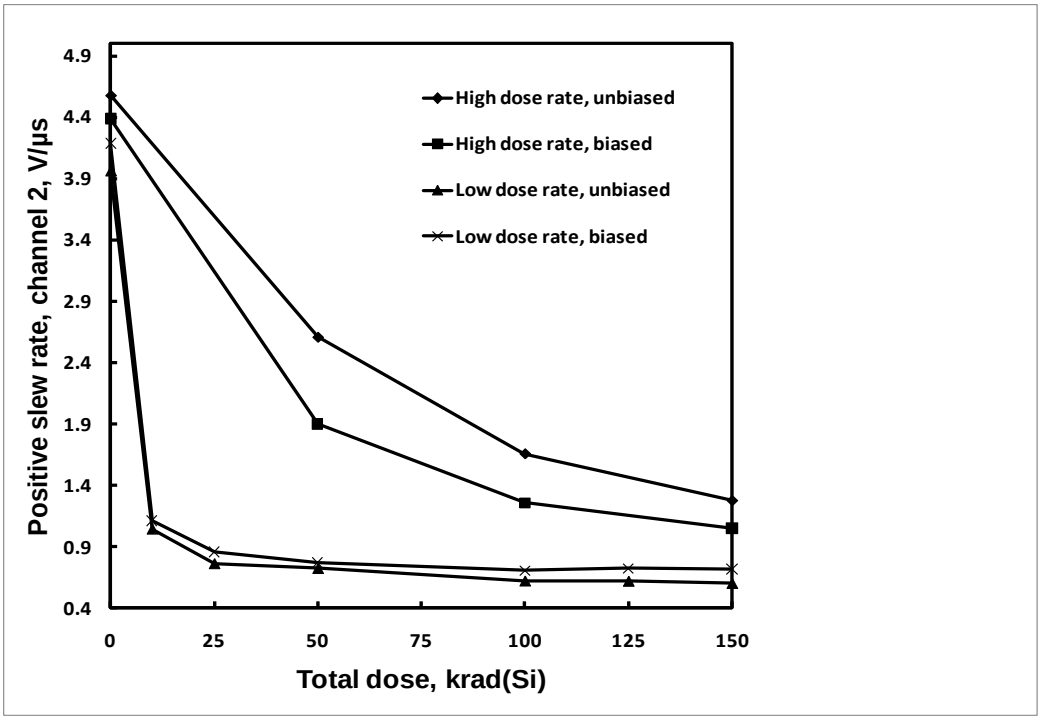

Figure 49: ISL7124SRH positive slew rate, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is .4V/µs.

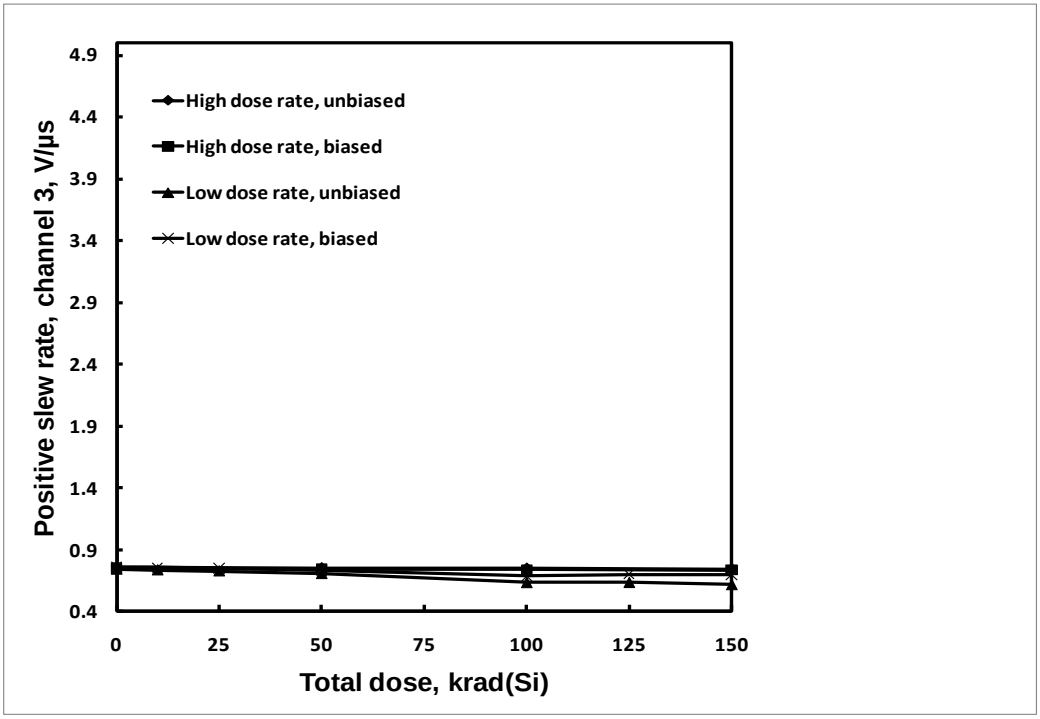

Figure 50: ISL7124SRH positive slew rate, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is .4V/µs.

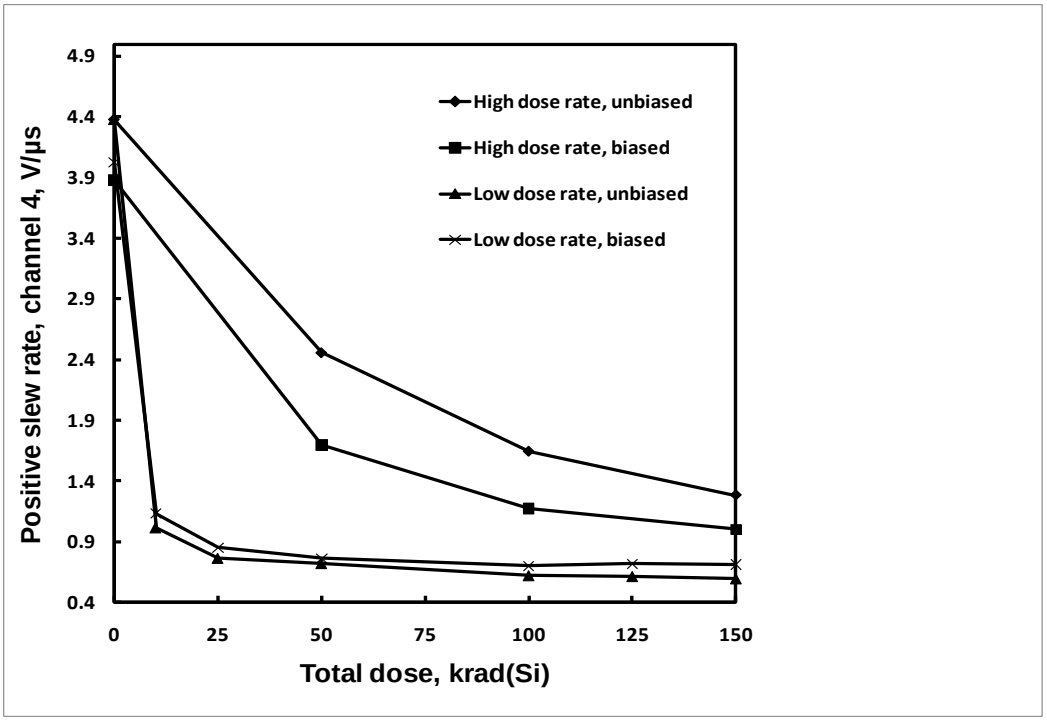

Figure 51: ISL7124SRH positive slew rate, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is .4V/µs.

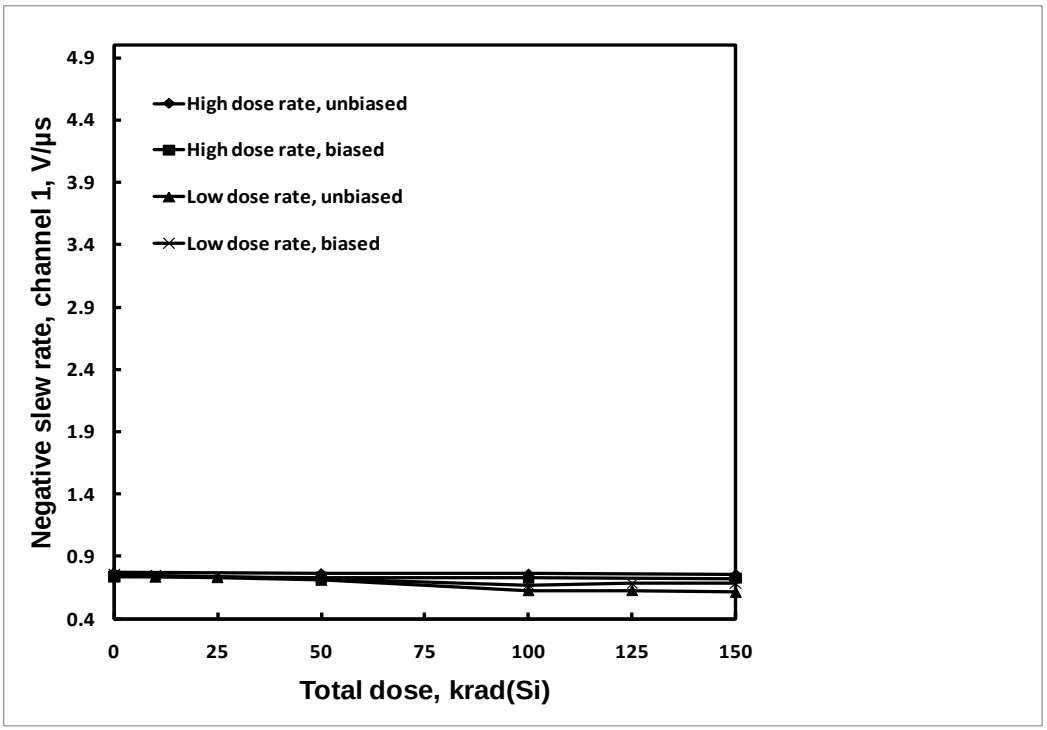

Figure 52: ISL7124SRH negative slew rate, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is .4V/µs.

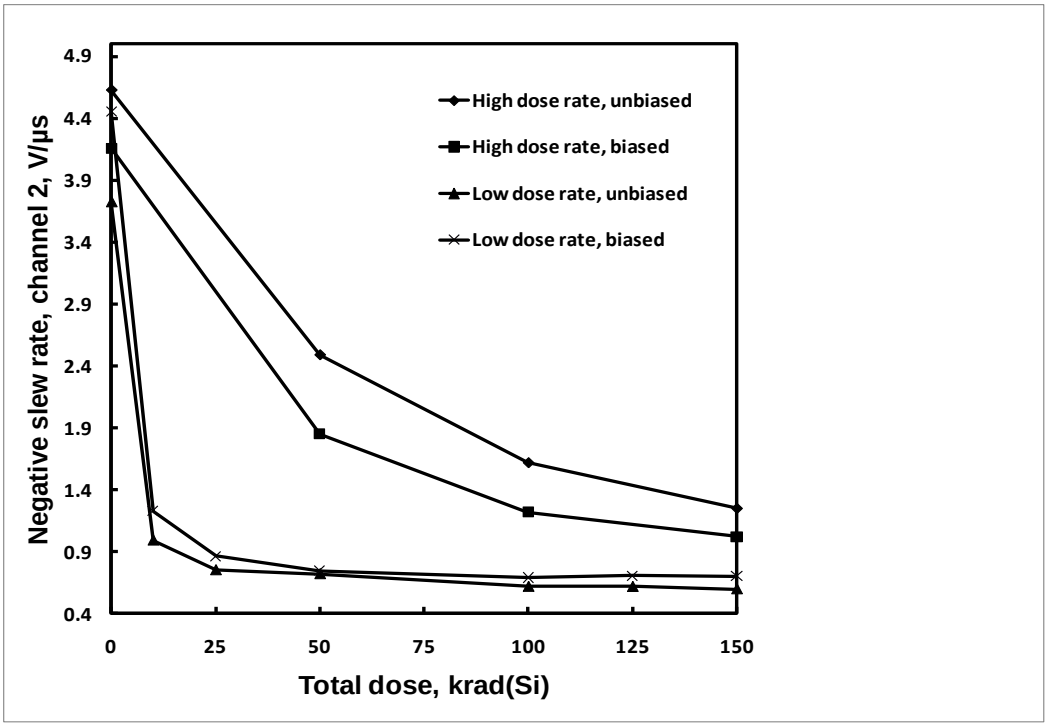

Figure 53: ISL7124SRH negative slew rate, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is .4V/µs.

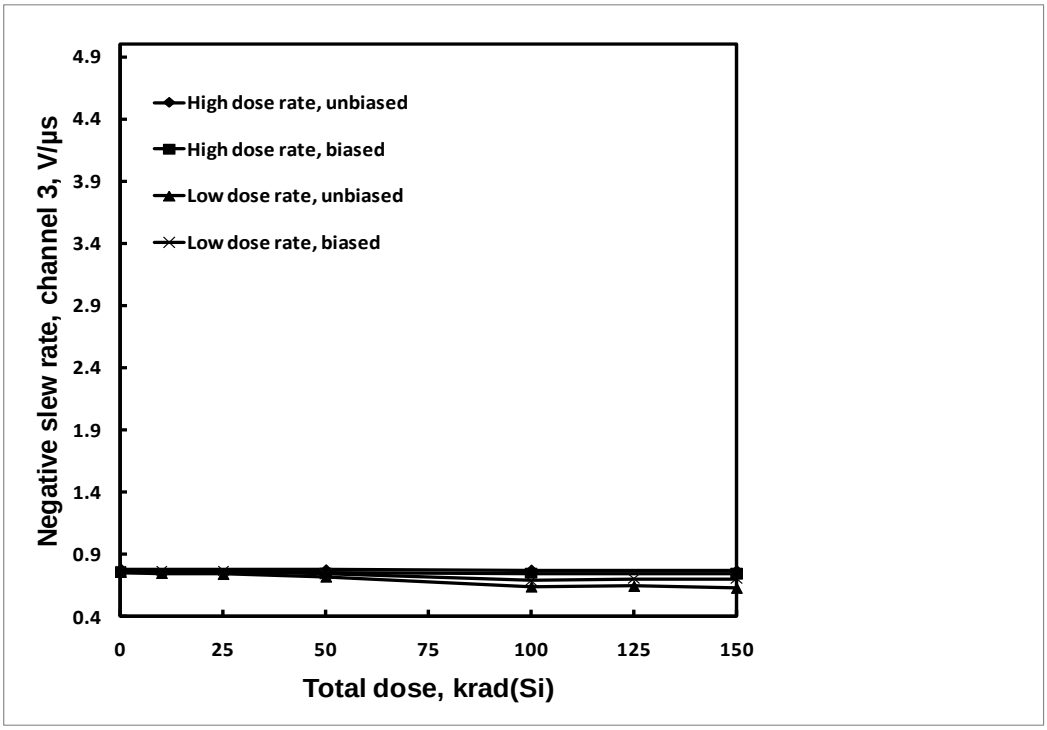

Figure 54: ISL7124SRH negative slew rate, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is .4V/µs.

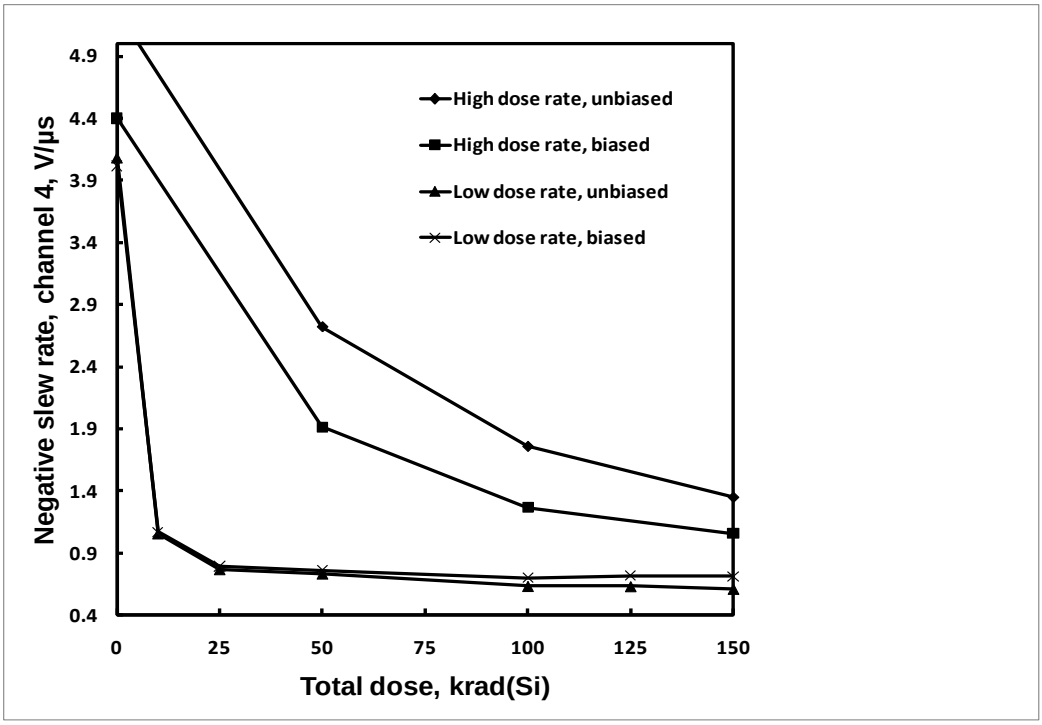

Figure 55: ISL7124SRH negative slew rate, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is .4V/µs.

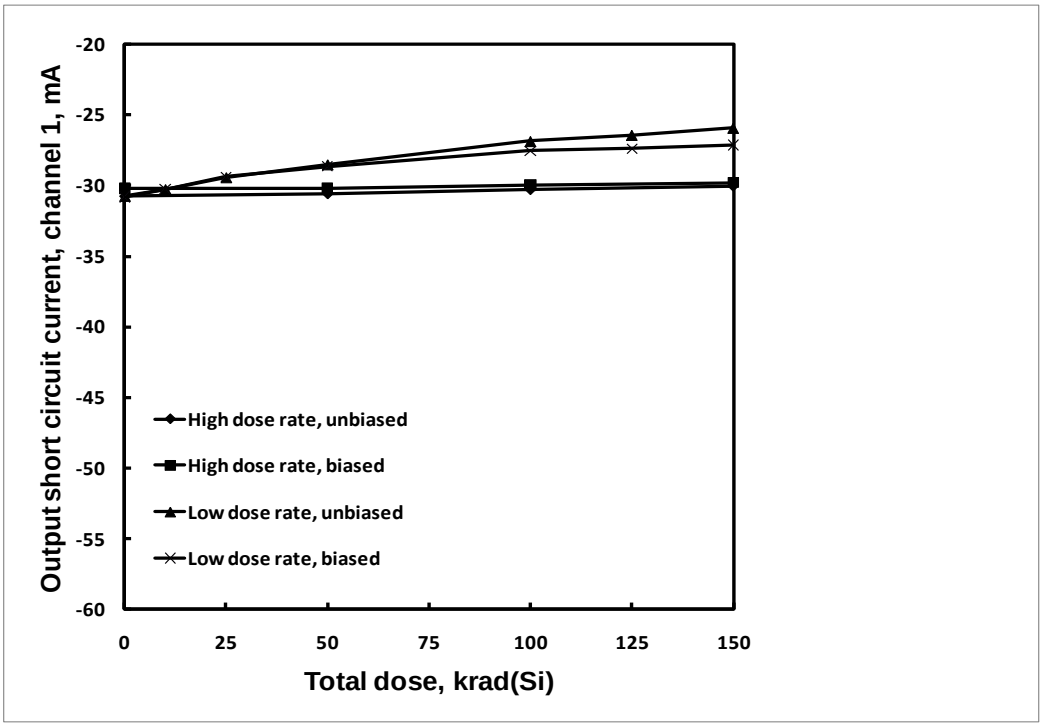

Figure 56: ISL7124SRH output short circuit current, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is -60mA maximum.

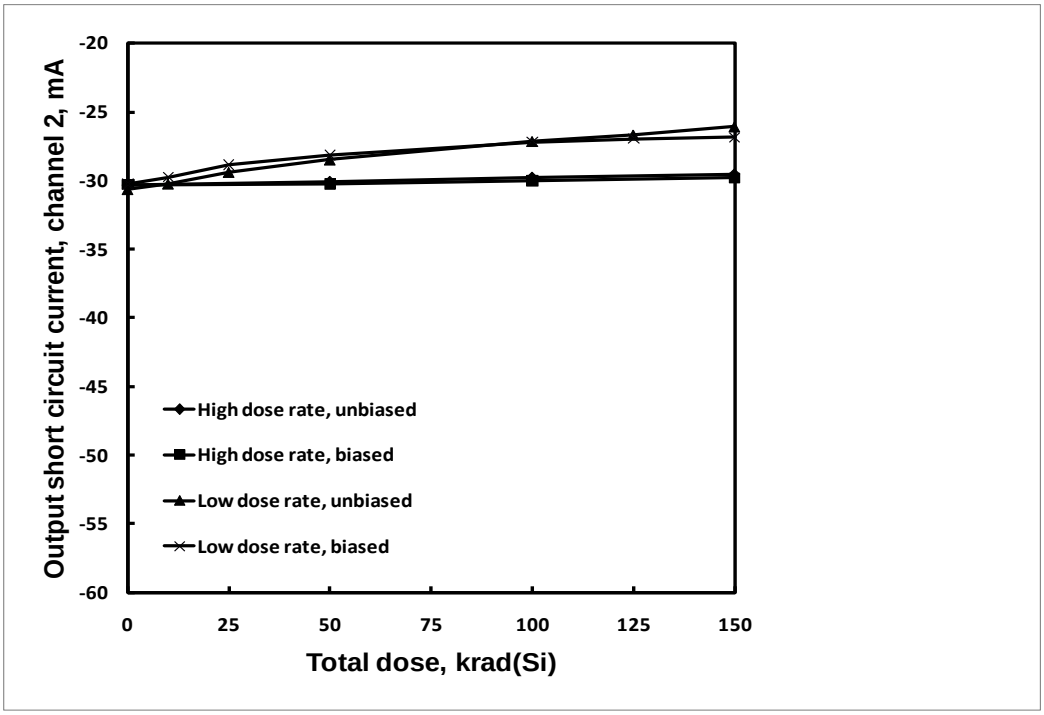

Figure 57: ISL7124SRH output short circuit current, channel 2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is -60mA maximum.

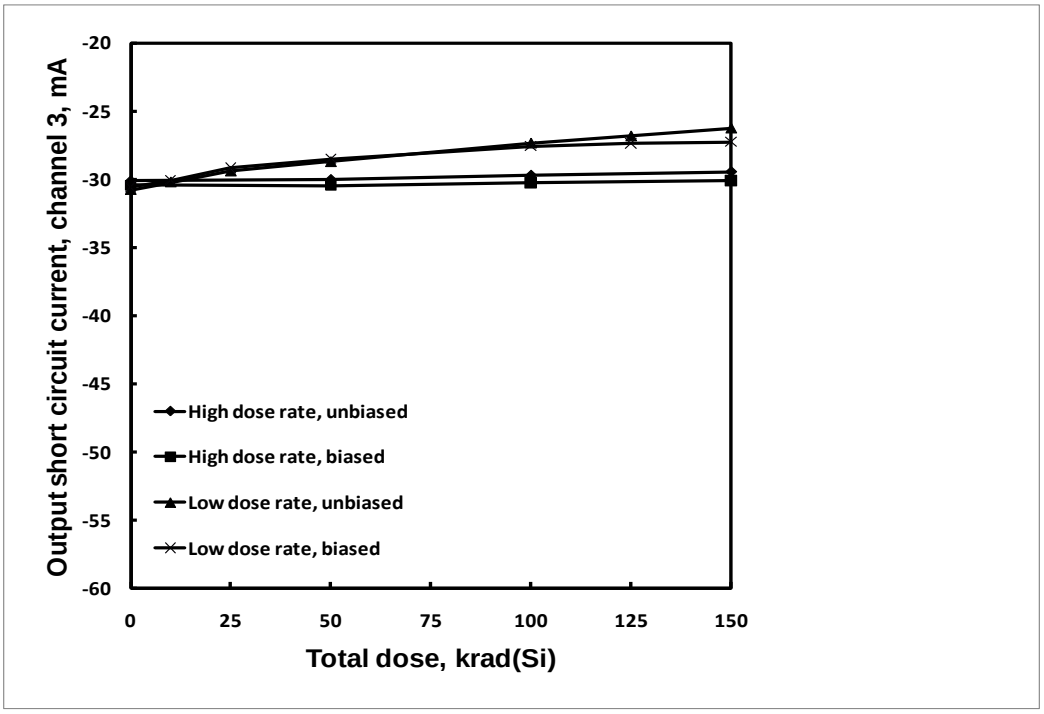

Figure 58: ISL7124SRH output short circuit current, channel 3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is -60mA maximum.

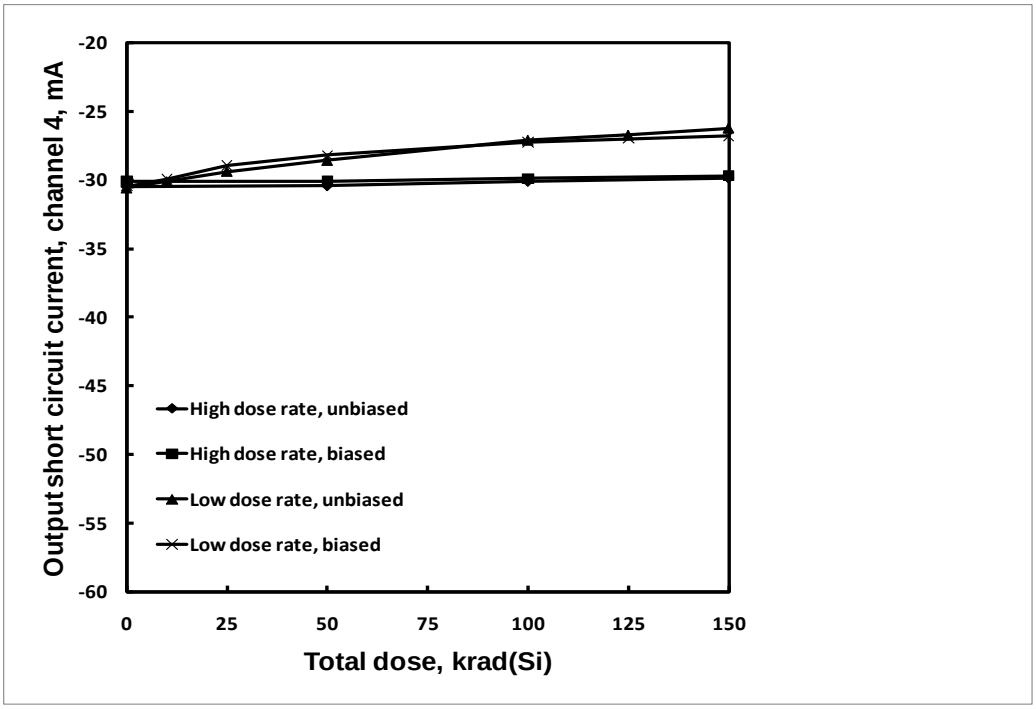

Figure 59: ISL7124SRH output short circuit current, channel 4, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is -60mA maximum.

6: Conclusion

This document reports results of a total dose test of the ISL7124SRH quad operational amplifier. Parts were tested at low and high dose rate under biased and unbiased conditions as outlined in MIL-STD-883 Test Method 1019.7, to a maximum total dose of 150krad(Si).

The part was found to be dose rate sensitive, with unbiased low dose rate irradiation worst case as expected. The input offset voltage was outside the +/-10mV SMD post-irradiation specification at the 100krad(Si) downpoint. The positive input bias current was close to the +/-400nA post-irradiation limit at the 125krad(Si) downpoint but recovered somewhat at 150krad(Si). The cause of the bias current degradation is considered to be the gradually degradation of the gain ('beta') of the input PNP transistor pair. The negative input bias current was outside the +/-400nA limit after 125krad(Si). The input offset current remained very stable, indicating that the input pair gain remains well-matched in spite of the degradation in absolute value.

Open-loop voltage gain was outside the 20V/mV (86dB) limit at the 100krad(Si) downpoint. Common-mode rejection ratio data for Channel 3 was of doubtful quality, as was the positive and negative slew rate data for Channels 2 and 4. We have plotted this anomalous data for information only.

The part is considered low dose rate sensitive but remains within the SMD post-irradiation limits to a maximum of 50krad(Si) in this environment. Similarly, we observed some bias sensitivity in the low dose rate results.

7: Appendices

7.1: Reported parameters.

Figure	Parameter	Limit, low	Limit, high	Units	Notes
3	Input offset voltage	-10	+10	mV	Channel 1
4	Input offset voltage	-10	+10	mV	Channel 2
5	Input offset voltage	-10	+10	mV	Channel 3
6	Input offset voltage	-10	+10	mV	Channel 4
7	Positive input bias current	-400	+400	nA	Channel 1
8	Positive input bias current	-400	+400	nA	Channel 2
9	Positive input bias current	-400	+400	nA	Channel 3
10	Positive input bias current	-400	+400	nA	Channel 4
11	Negative input bias current	-400	+400	nA	Channel 1
12	Negative input bias current	-400	+400	nA	Channel 2
13	Negative input bias current	-400	+400	nA	Channel 3
14	Negative input bias current	-400	+400	nA	Channel 4
15	Input offset current	-150	+150	nA	Channel 1
16	Input offset current	-150	+150	nA	Channel 2
17	Input offset current	-150	+150	nA	Channel 3
18	Input offset current	-150	+150	nA	Channel 4
19	Large signal voltage gain	20		dB	Channel 1
20	Large signal voltage gain	20		dB	Channel 2
21	Large signal voltage gain	20		dB	Channel 3
22	Large signal voltage gain	20		dB	Channel 4
23	Output low voltage		900	mV	Channel 1
24	Output low voltage		900	mV	Channel 2
25	Output low voltage		900	mV	Channel 3
26	Output low voltage		900	mV	Channel 4
27	Output high voltage	23		V	Channel 1
28	Output high voltage	23		V	Channel 2
29	Output high voltage	23		V	Channel 3
30	Output high voltage	23		V	Channel 4
31	Output voltage swing	24		V	Channel 1
32	Output voltage swing	24		V	Channel 2
33	Output voltage swing	24		V	Channel 3
34	Output voltage swing	24		V	Channel 4
35	Quiescent power supply current		3	mA	
36	Positive power supply rejection ratio	70		dB	Channel 1
37	Positive power supply rejection ratio	70		dB	Channel 2
38	Positive power supply rejection ratio	70		dB	Channel 3

39	Positive power supply rejection ratio	70		dB	Channel 4
40	Negative power supply rejection ratio	70		dB	Channel 1
41	Negative power supply rejection ratio	70		dB	Channel 2
42	Negative power supply rejection ratio	70		dB	Channel 3
43	Negative power supply rejection ratio	70		dB	Channel 4
44	Common mode rejection ratio	70		dB	Channel 1
45	Common mode rejection ratio	70		dB	Channel 2
46	Common mode rejection ratio	70		dB	Channel 3
47	Common mode rejection ratio	70		dB	Channel 4
48	Positive slew rate	0.4		V/µs	Channel 1
49	Positive slew rate	0.4		V/µs	Channel 2
50	Positive slew rate	0.4		V/µs	Channel 3
51	Positive slew rate	0.4		V/µs	Channel 4
52	Negative slew rate	0.4		V/µs	Channel 1
53	Negative slew rate	0.4		V/µs	Channel 2
54	Negative slew rate	0.4		V/µs	Channel 3
55	Negative slew rate	0.4		V/µs	Channel 4
56	Output short circuit current	-60		mA	Channel 1
57	Output short circuit current	-60		mA	Channel 2
58	Output short circuit current	-60		mA	Channel 3
59	Output short circuit current	-60		mA	Channel 4

Note 1: Limits are taken from Standard Microcircuit Drawing (SMD) 5962-02542.

8: Document revision history

Revision	Date	Pages	Comments
0	18 August 2010	All	Original issue