ISL75052SEH

Total Dose Test Report

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Introduction

This report discusses the results of low and high dose rate total dose testing and subsequent high temperature annealing of the ISL75052SEH low dropout regulator. These tests were conducted to assess the total dose hardness of the part and its response to accelerated annealing. All testing is complete at the time of this report. Parts were irradiated under bias and with all pins grounded at Low Dose Rate (LDR) and at High Dose Rate (HDR) to the 100krad(Si) total dose level specified in the datasheet. All samples were also taken out to the 50% overtest level (which is 150krad(Si) in this case, as the part is rated at 100krad(Si)) and subsequent anneal as described in MIL-STD-883 Test Method 1019. The high temperature anneals were performed under bias at an ambient temperature of +100°C for 168 hours.

The ISL75052SEH is acceptance tested on a wafer-by-wafer basis to 100krad(Si) at HDR (50 – 300rad(Si)/s) and to 50krad(Si) at LDR (0.01rad(Si)/s), ensuring hardness to the specified level for both dose rates. The SMD total dose specifications are 100krad(Si) (HDR) and 50krad(Si) (LDR). Although this report is written for the ISL75052SEH, it applies equally to the ISL73052SEH as they are the same design and silicon, differing only in radiation assurance testing.

The ISL75052SEH showed good performance over low and HDR irradiation. All samples passed the post-irradiation at all down points and following the accelerated anneal procedure. The output voltage showed some rebound after the accelerated anneal, but in no case did the parametric values exceed the post-irradiation limits. We observed no significant dose rate sensitivity, and in fact the output voltage data shows HDR irradiation to be somewhat worst case, not an unexpected result for a largely CMOS component. No measurable differences in total dose response were noted between biased and grounded irradiation for any parameters.

Related Literature

For a full list of related documents, visit our website:

- ISL75052SEH, ISL73052SEH device pages
- MIL-STD-883 test method 1019

Product Description

The ISL75052SEH is a radiation hardened, single output low dropout regulator (LDO) specified for an output current of 1.5A. The device operates from an input voltage range of 4.0V to 13.2V and an output voltage range of 0.6V to 12.7V. The output voltage is adjustable based on an external resistor divider setting. Dropout voltages as low as 75mV (at 0.5A) typical can be realized, allowing you to improve system efficiency by lowering V_{IN} to nearly V_{OUT}. An Enable feature allows the part to be placed into a low shutdown current mode of 165µA (typical). When enabled, the ISL75052SEH operates with a low ground current of 11mA (typical), which provides operation with low quiescent power consumption. The device has superior transient response and is designed for predictable operation in the Single Event Effects (SEE) environment, including reduced Single Event Transient (SET) magnitude seen on the output. There is no need for additional SET protection diodes and filters.

The compensation (COMP) pin enables the use of external compensation. This is achieved by connecting a resistor and capacitor from the COMP pin to ground. The device is stable with tantalum capacitors as low as 47µF (KEMET T525 series) and provides excellent voltage regulation from no load to full load. The programmable soft-start function allows you to program the inrush current with the decoupling capacitor used on the Bypass (BYP) pin. The overcurrent protection (OCP) pin allows the short-circuit output current limit threshold to be programmed with a resistor from the OCP pin to ground. The OCP setting range is from 0.16A minimum to 3.2A maximum.

The thermal shutdown function disables the output if the device temperature exceeds a specified value; the ISL75052SEH subsequently enters an ON/OFF (hiccup) cycle until the fault is removed. The ISL75052SEH is available in a 16 Ld hermetic ceramic flatpack and in die form. The part offers assured performance across the full -55°C to +125°C military temperature range.

Key Features and Specifications

- Input supply voltage range: 4.0V to 13.2V
- Output current, T_J = +150°C: 1.5A
- Shutdown current: 165µA typical
- Output voltage accuracy: ±1.5%, Note 1
- Dropout voltage, 0.5A: 75mV typical
- Dropout voltage, 1.5A: 225mV typical
- Output noise voltage. 300 Hz-300kHz: 100μV_{RMS} typical
- Power supply rejection ratio, 1kHz: 65dB typical
- Enable, PGOOD, and programmable soft-start features
- Over-temperature shutdown and adjustable overcurrent protection
- Operating temperature range: -55°C to +125°C
- 16 Ld hermetic flatpack
- Total dose rating (50 – 300rad(Si)/s): 100krad(Si)
- Total dose rating (0.01rad(Si)/s): 100krad(Si)
- SET/SEL/SEB linear energy transfer rating: 86MeV•cm^2/mg

Note:
1. The output voltage accuracy of ±1.5% is specified over line, load, and temperature.

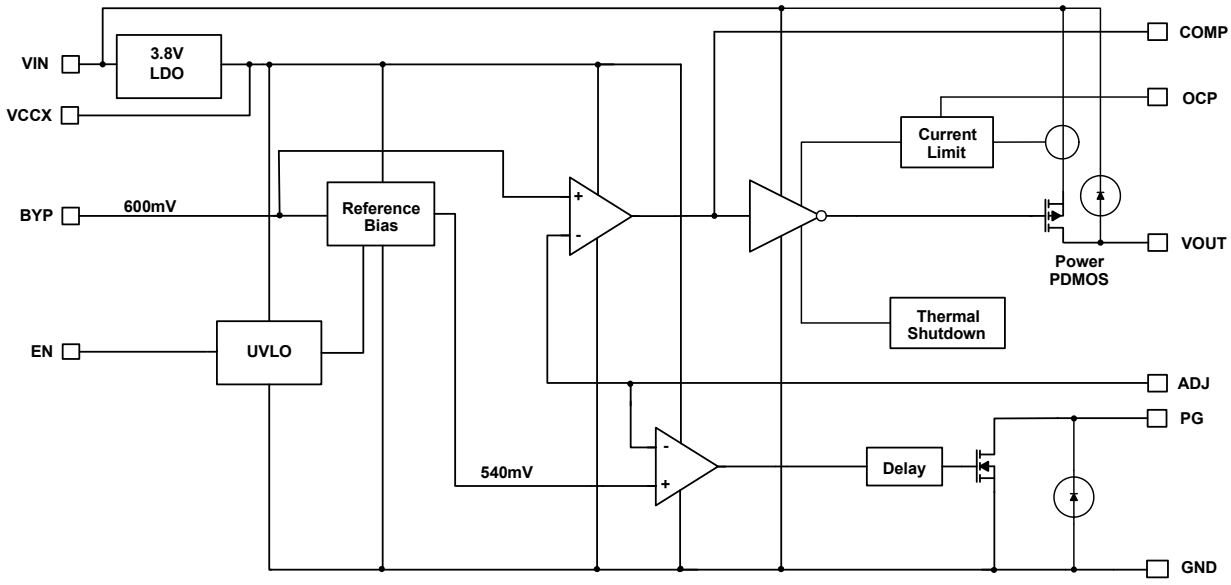

Figure 1. ISL75052SEH Block Diagram

1. Test Description

1.1 Irradiation Facilities

HDR testing was performed at 71.9rad(Si)/s using a Gammacell 220 ^{60}Co irradiator located in the Palm Bay, Florida Renesas facility. LDR testing was performed at 0.01rad(Si)/s using the Renesas Palm Bay N40 panoramic LDR ^{60}Co irradiator. The post-irradiation biased anneal operations were performed at +100°C in a small temperature chamber.

1.2 Test Fixturing

Figure 2 shows the configuration used for biased irradiation. The grounded irradiations were performed in the same fixture type with all pins hardwired to ground.

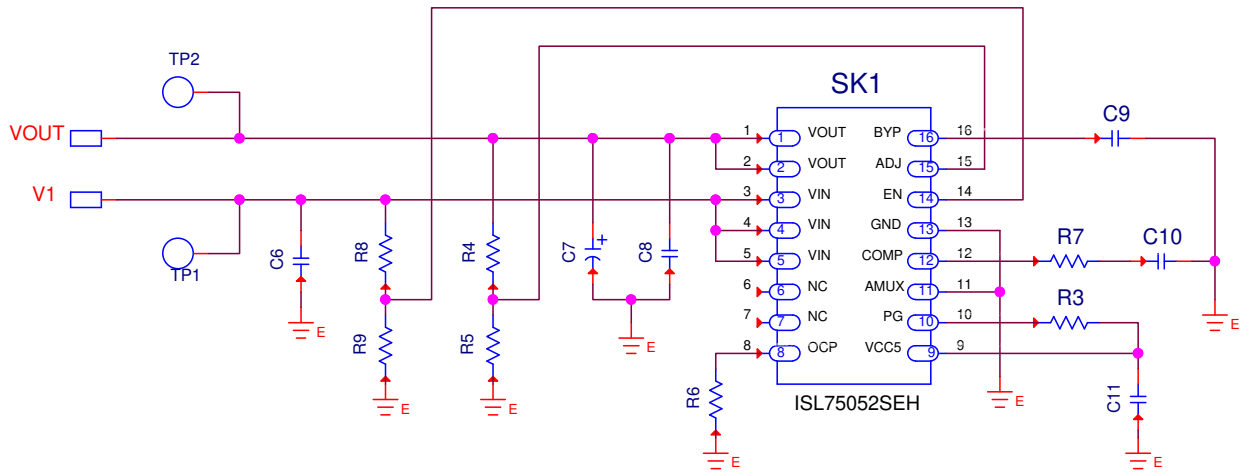

Figure 2. Biased and Unbiased (Grounded) Irradiation Bias Configurations for the ISL75052SEH

1.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with data logging at each down point. All down point electrical testing was performed at room temperature. Three control units were used to improve repeatability.

1.4 Experimental Matrix

The experimental matrix consisted of 18 samples irradiated at LDR under bias, 20 samples irradiated at LDR with all pins grounded, 7 samples irradiated at HDR under bias, and 5 samples irradiated at HDR with all pins grounded. Samples of the ISL75052SEH were drawn from preproduction lot WXT5J and were packaged in the hermetic 16 Ld ceramic flatpack (package code KCG) package, which has an electrically grounded lid and a metallized bottom. Samples were processed through the standard burn-in cycle before irradiation, as required by MIL-STD-883, and were screened to the ATE limits at room temperature prior to the test.

1.5 Down Points

Down points for the low and HDR tests were zero, 25, 50, 100, and 150krad(Si) followed by a 168-hour anneal under bias at +100°C. All testing is complete at this time.

2. Results

2.1 Attributes Data

Table 1 shows the attributes data to date for the test. No rejects to the post-irradiation SMD limits were encountered at any down point including the high temperature anneals.

Table 1. ISL75052SEH Total Dose Test Attributes Data

Dose Rate (rad(Si)/s)	Bias	Sample Size	Down Point	Pass (Note 2)	Rejects
0.01	Figure 2	18	0	18	0
			25krad(Si)	18	0
			50krad(Si)	18	0
			100krad(Si)	18	0
			150krad(Si)	18	0
			Anneal, 168h at +100°C	18	0
0.01	Grounded	20	0	20	0
			25krad(Si)	20	0
			50krad(Si)	20	0
			100krad(Si)	20	0
			150krad(Si)	20	0
			Anneal, 168h at +100°C	20	0
71.9	Figure 2	7	0	7	0
			25krad(Si)	7	0
			50krad(Si)	7	0
			100krad(Si)	7	0
			150krad(Si)	7	0
			Anneal, 168h at +100°C	7	0
71.9	Grounded	5	0	5	0
			25krad(Si)	5	0
			50krad(Si)	5	0
			100krad(Si)	5	0
			150krad(Si)	5	0
			Anneal, 168h at +100°C	5	0

Notes:
2. 'Pass' indicates a sample that passes all post-irradiation SMD limits.
3. The 168-hour anneal was performed at +100°C under bias as shown in Figure 2.

2.2 Variables Data

The plots in Figures 3 through 25 show data at all down points including the post-anneal data. The plots show the response to total dose irradiation at LDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded) and at HDR for the biased cases (Figure 2) and unbiased cases. In addition the plots show the response of the samples to a post-irradiation anneal at +100°C for 168 hours. We chose to plot the median for these parameters due to the relatively small sample sizes. "Discussion and Conclusion" on page 16 provides individual discussion of the figures.

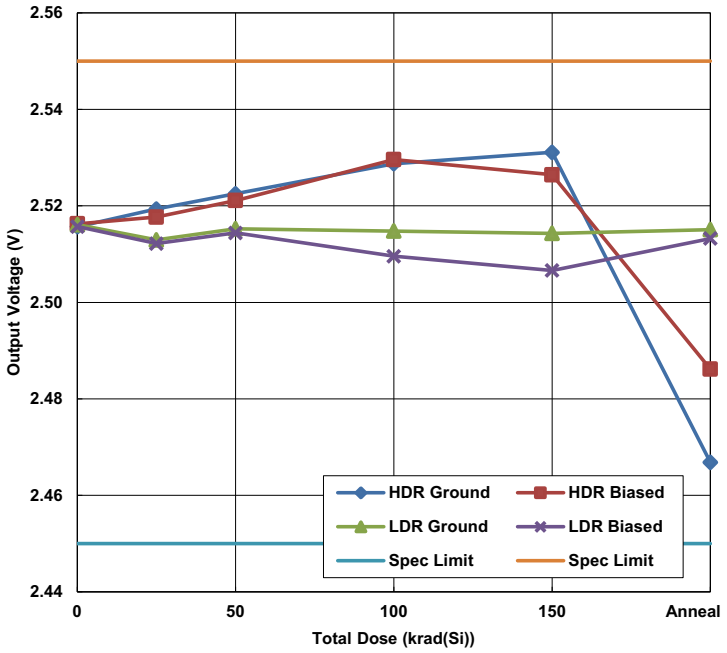

Figure 3. ISL75052SEH output voltage accuracy, 4.0V_{IN}, 2.5V_{OUT}, no load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limits are 2.45V to 2.55V.

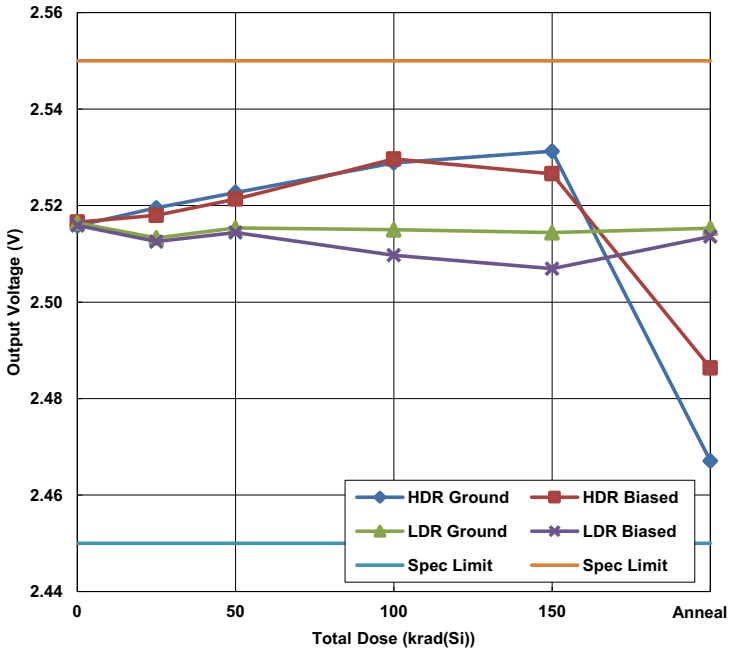

Figure 4. ISL75052SEH output voltage accuracy, 4.0V_{IN}, 2.5V_{OUT}, 1.5A load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limits are 2.45V to 2.55V.

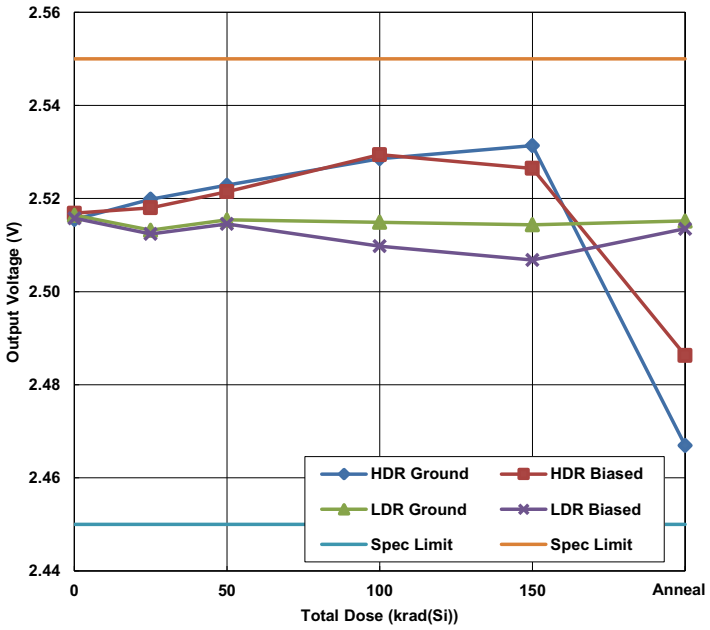

Figure 5. ISL75052SEH output voltage accuracy, 5.0V_{IN}, 2.5V_{OUT}, no load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limits are 2.45V to 2.55V.

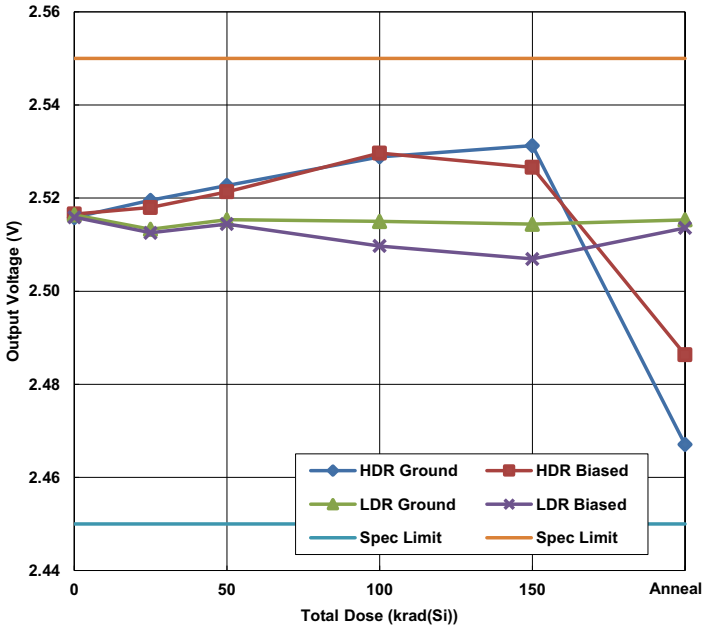

Figure 6. ISL75052SEH output voltage accuracy, 5.0V_{IN}, 2.5V_{OUT}, 1.5A load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limits are 2.45V to 2.55V.

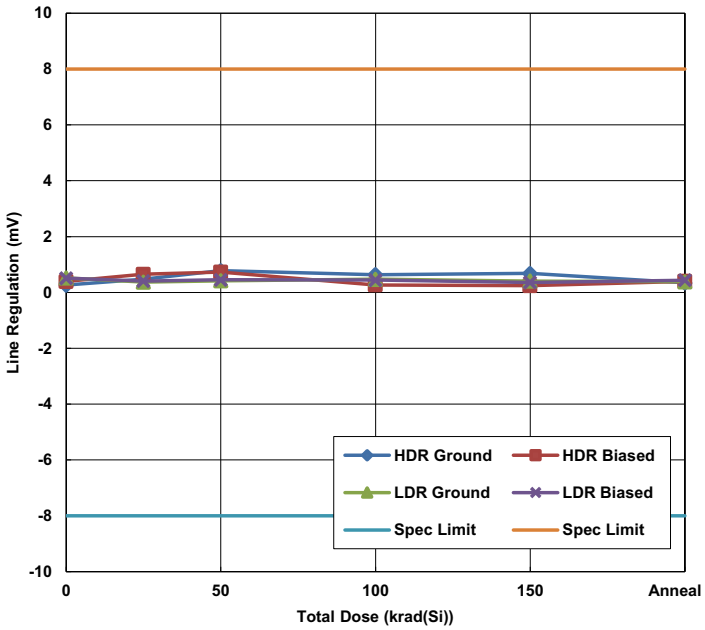

Figure 7. ISL75052SEH line regulation, 2.5V_{OUT}, 4.0V<V_{IN}<13.2V, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limits are -8.0mV to 8.0mV.

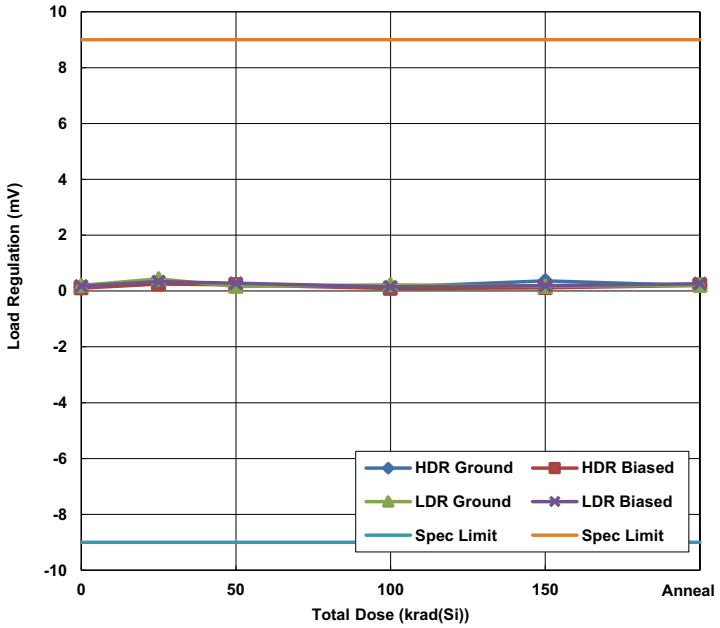

Figure 8. ISL75052SEH load regulation, 2.5V_{OUT}, 0A<I_{LOAD}<1.5A, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limits are -9.0mV to 9.0mV.

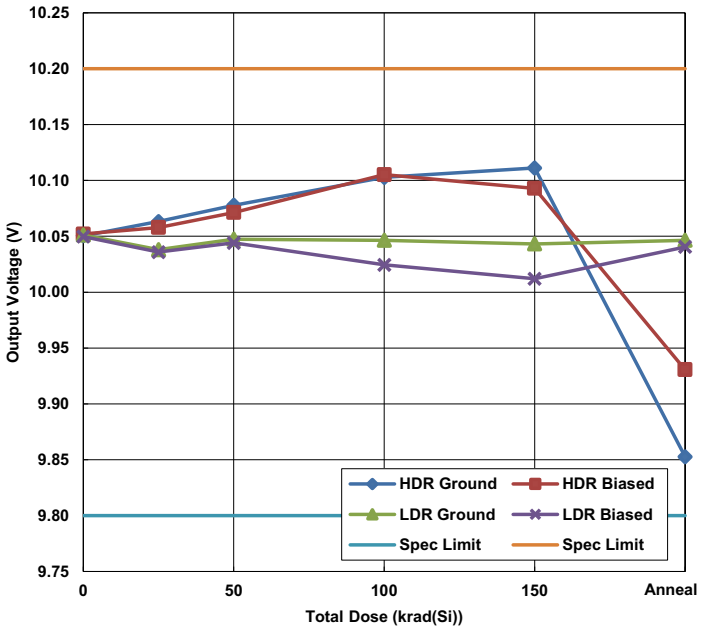

Figure 9. ISL75052SEH output voltage accuracy, 10.5V_{IN}, 10.0V_{OUT}, no load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limits are 9.8V to 10.2V.

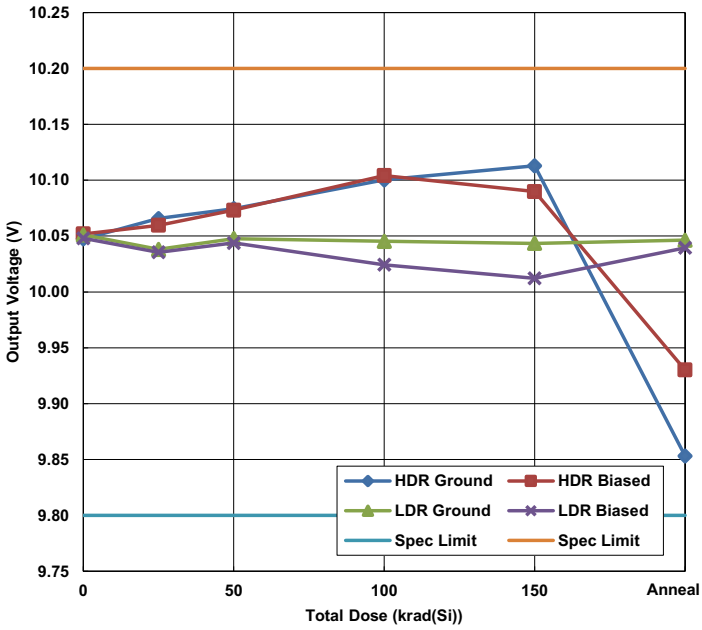

Figure 10. ISL75052SEH output voltage accuracy, 10.5V_{IN}, 10.0V_{OUT}, 1.5A load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limits are 9.8V to 10.2V.

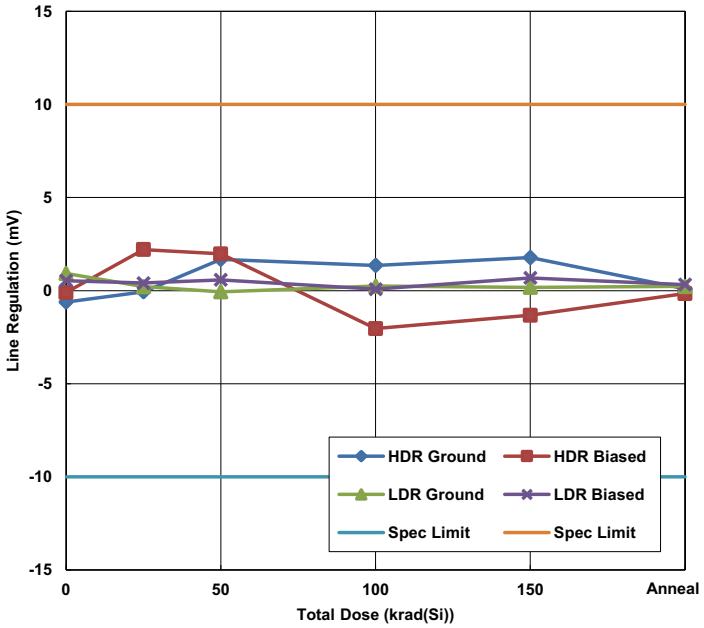

Figure 11. ISL75052SEH line regulation, 10.0V_{OUT}, 10.5V<V_{IN}<13.2V, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limits are -10.0mV to 10.0mV.

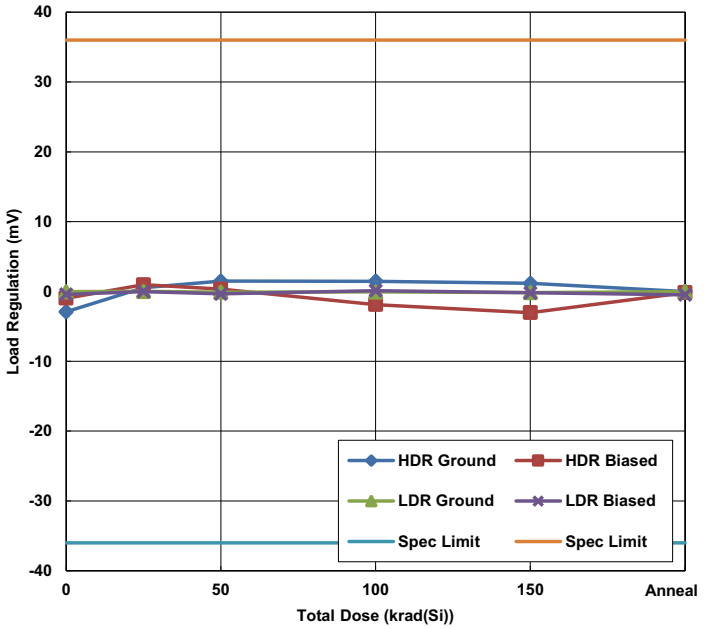

Figure 12. ISL75052SEH load regulation, 10.0V_{OUT}, 0A<I_{LOAD}<1.5A, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limits are -36.0mV to 36.0mV.

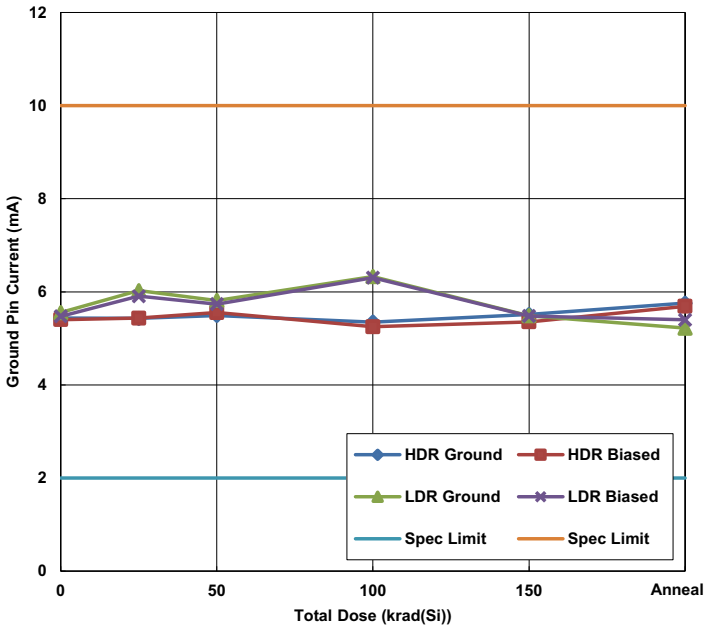

Figure 13. ISL75052SEH ground pin current, 4.0V_{IN}, 2.5V_{OUT}, no load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limit is 10.0mA maximum; the 2.0mA specification is an ATE limit.

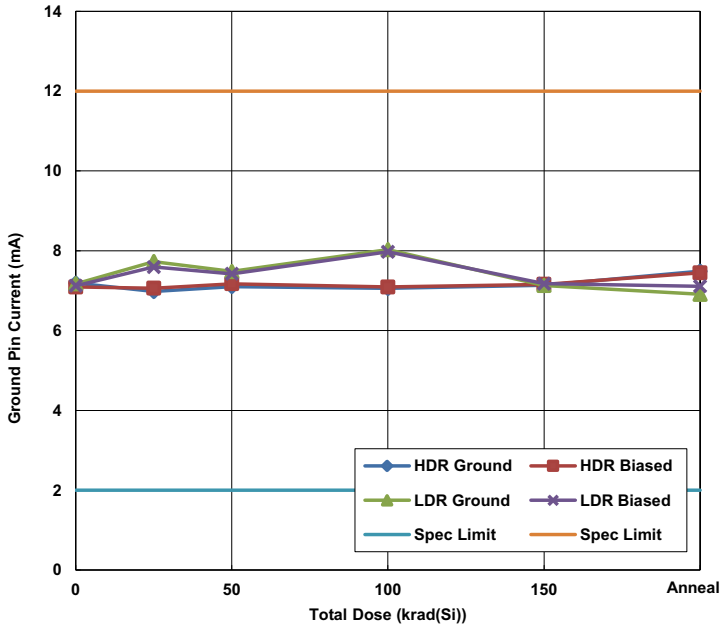

Figure 14. ISL75052SEH ground pin current, 4.0V_{IN}, 2.5V_{OUT}, 1.5A load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limit is 12.0mA maximum; the 2.0mA specification is an ATE limit.

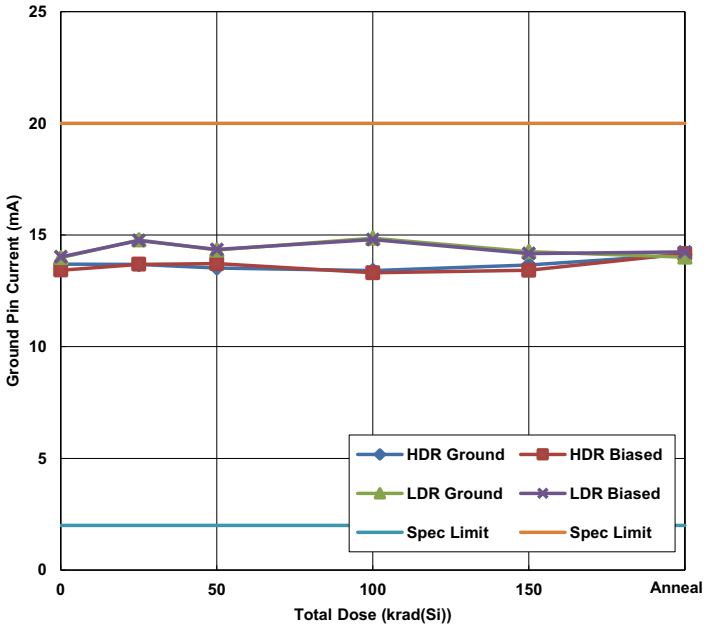

Figure 15. ISL75052SEH ground pin current, 10.5V_{IN}, 10.0V_{OUT}, no load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limit is 20.0mA maximum; the 2.0mA specification is an ATE limit.

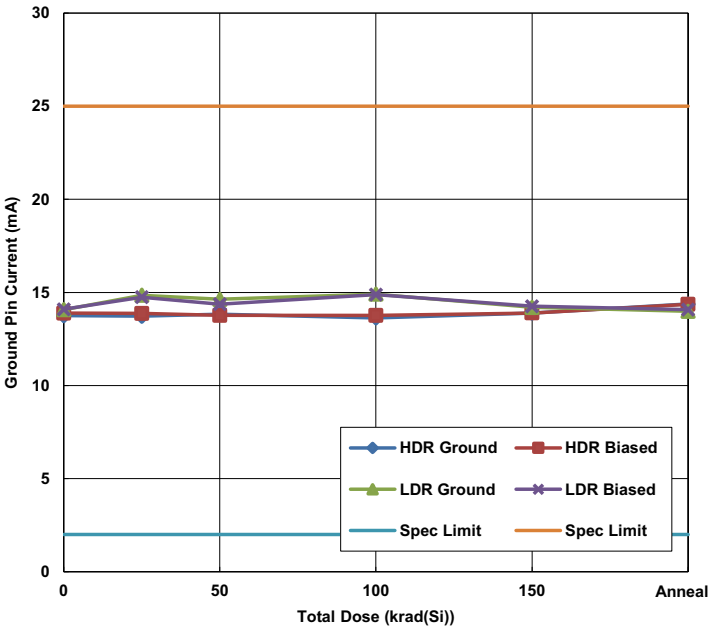

Figure 16. ISL75052SEH ground pin current, 10.5V_{IN}, 10.0V_{OUT}, 1.5A load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limit is 25.0mA maximum; the 2.0mA specification is an ATE limit.

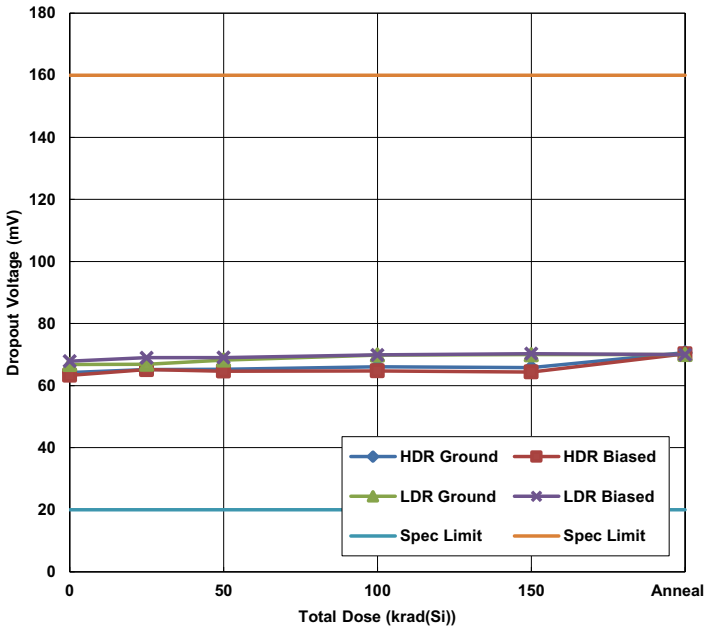

Figure 17. ISL75052SEH dropout voltage, 3.6V_{OUT}, 500mA load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limit is 160.0mV maximum; the 20mV specification is an ATE limit.

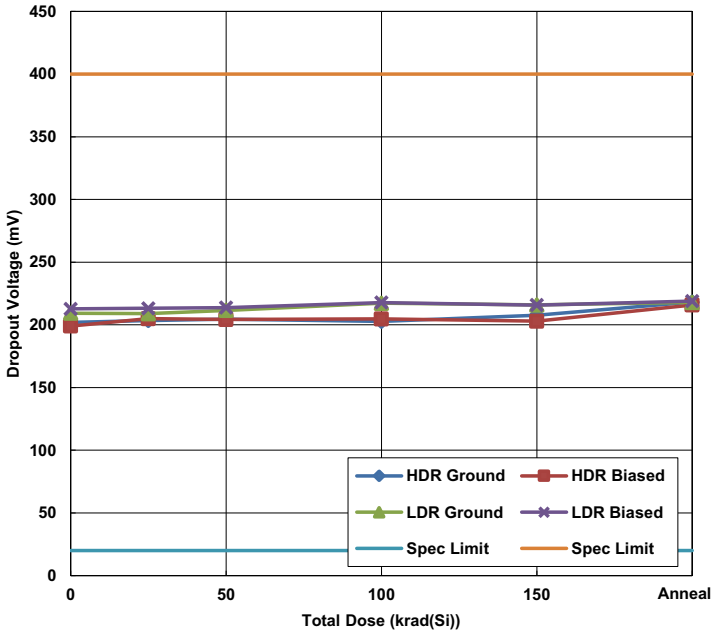

Figure 18. ISL75052SEH dropout voltage, 3.6V_{OUT}, 1500mA load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limit is 400.0mV maximum; the 20mV specification is an ATE limit.

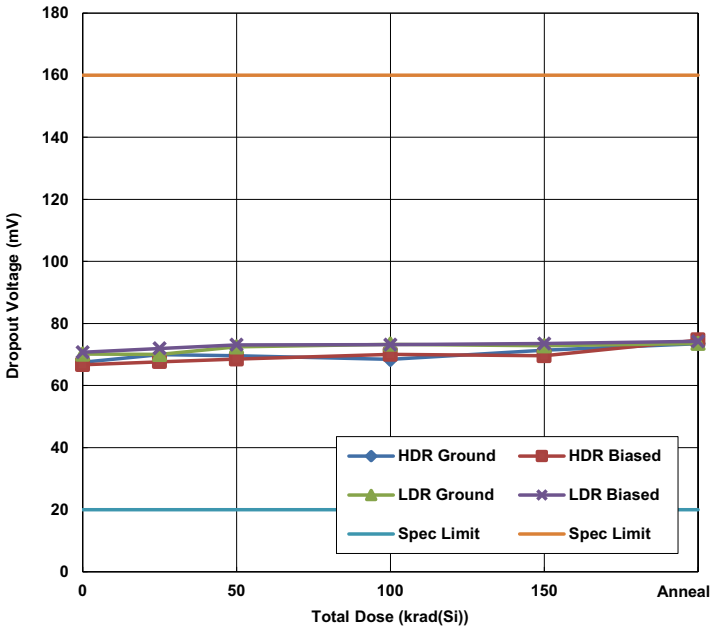

Figure 19. ISL75052SEH dropout voltage, 12.7V_{OUT}, 500mA load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limit is 160.0mV maximum; the 20mV specification is an ATE limit.

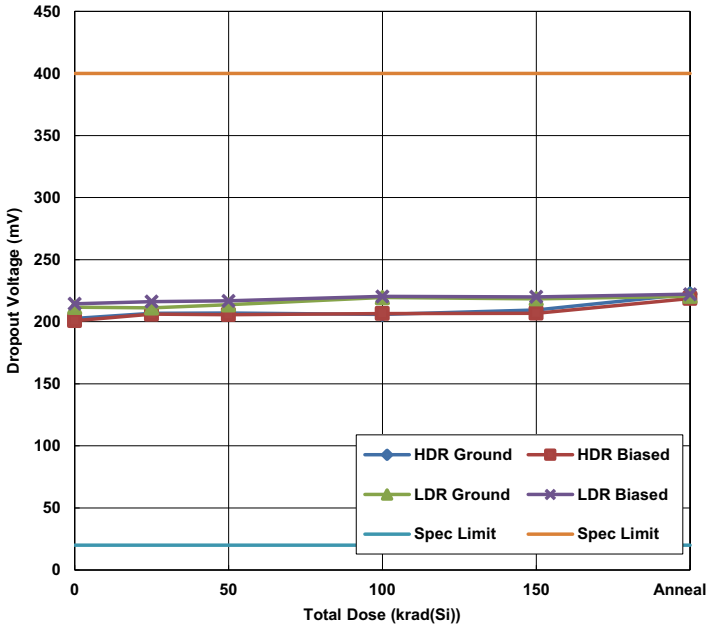

Figure 20. ISL75052SEH dropout voltage, 12.7V_{OUT}, 1500mA load, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limit is 400.0mV maximum; the 20mV specification is an ATE limit.

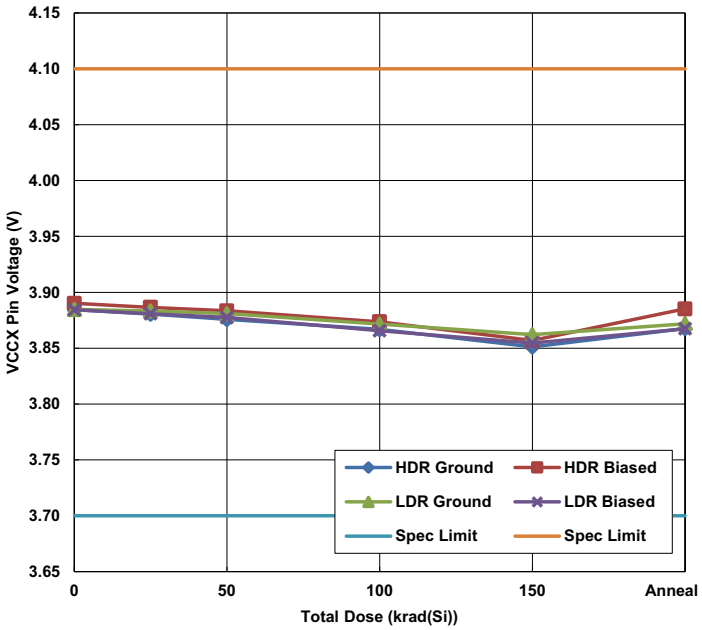

Figure 21. ISL75052SEH VCCX pin voltage, 4.0V input, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limits are 3.7V to 4.1V.

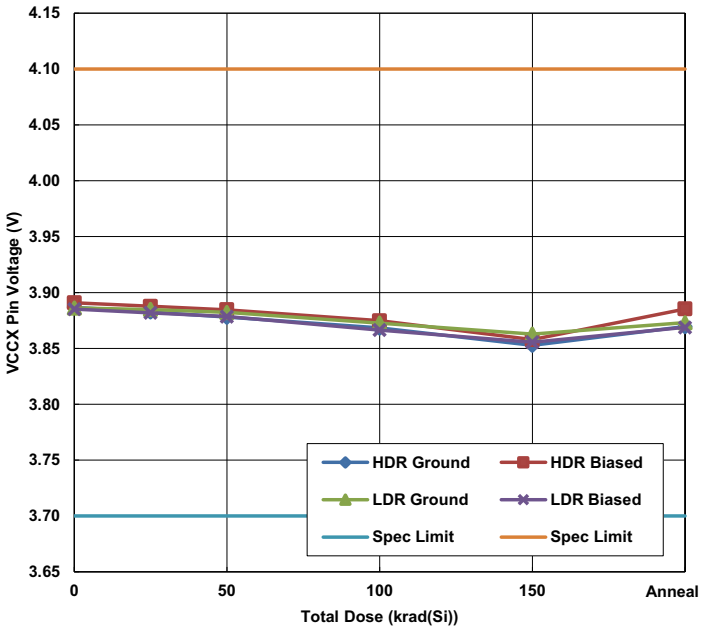

Figure 22. ISL75052SEH VCCX pin voltage, 13.2V_{IN}put, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limits are 3.7V to 4.1V.

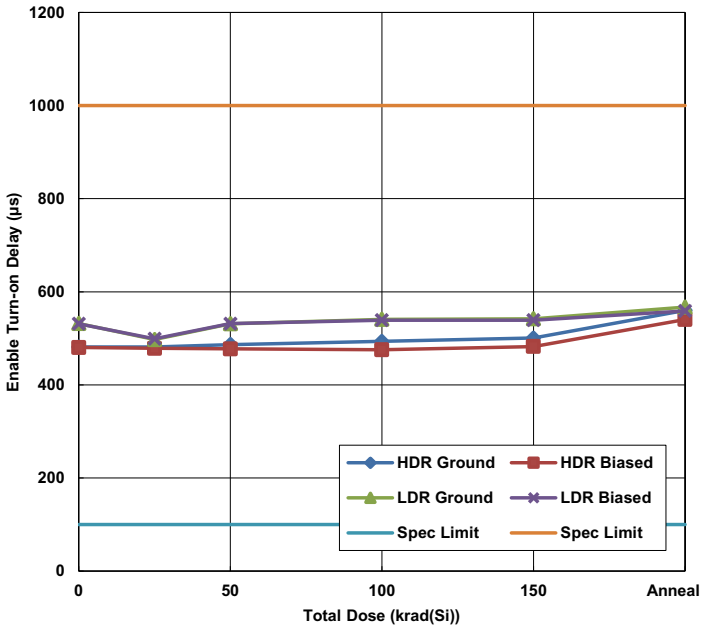

Figure 23. ISL75052SEH enable turn-on delay as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limit is 1000.0µs (1.0ms) maximum; the 100.0µs specification is an ATE limit.

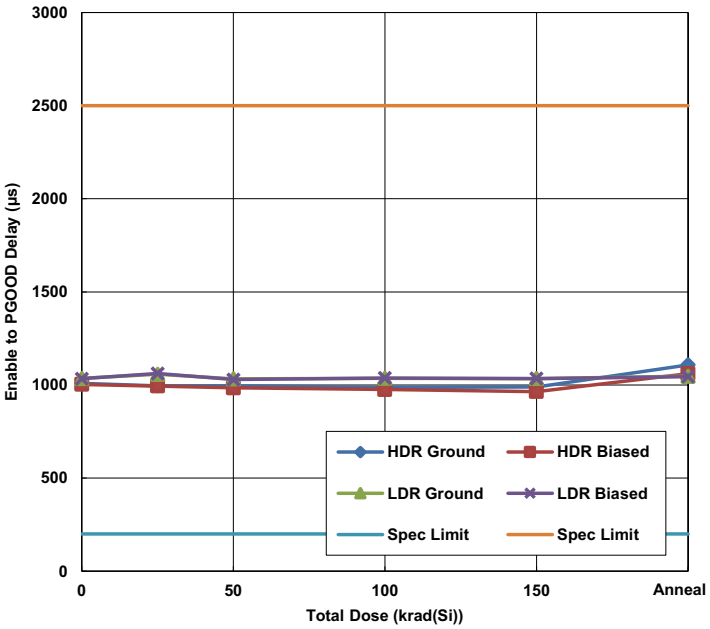

Figure 24. ISL75052SEH enable to PGOOD delay, 22µF output capacitor, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limit is 2500.0µs (2.5ms) maximum; the 200.0µs specification is an ATE limit.

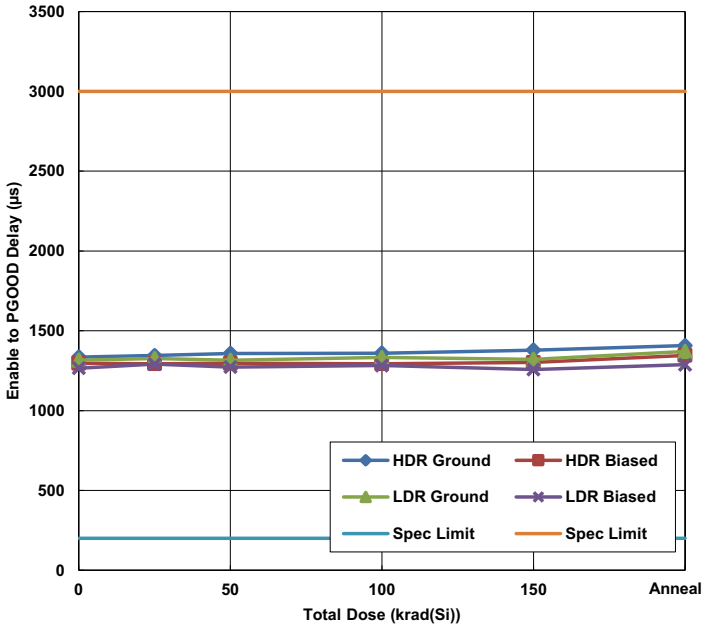

Figure 25. ISL75052SEH enable to PGOOD delay, 200µF output capacitor, as a function of total dose irradiation at LDR and HDR for the biased cases (per Figure 2) and unbiased cases (all pins grounded). The dose rate was 0.01rad(Si)/s for LDR irradiation and 71.9rad(Si)/s for HDR irradiation. The irradiations were followed by a biased anneal for 168 hours at +100°C. Sample sizes were 18 at LDR under bias, 20 at LDR with all pins grounded, 7 at HDR under bias, and 5 at HDR with all pins grounded. The SMD post-irradiation specification limit is 3000.0µs (3.0ms) maximum; the 200.0µs specification is an ATE limit.

3. Discussion and Conclusion

This document reports the results of LDR and HDR testing of the ISL75052SEH low dropout regulator. Parts were irradiated under bias and with all pins grounded at LDR and HDR in accordance with the MIL-STD-883 Test Method 1019.7 dose rate sensitivity protocol, at 0.01rad(Si)/s and 71.9rad(Si)/s respectively. All irradiations were followed by a high temperature anneal under bias at +100°C for 168 hours. All parameters remained within the SMD and datasheet post-irradiation limits at all down points. The part has a large number of measured parameters, so we have summarized the results in Table 1 on page 4 followed by a limited number of curves of interest ("Variables Data" on page 4, Figures 3 through 25). The following discusses each of the figures separately.

Figures 3 through 6 show the output voltage of the regulator for the $4.0V_{IN}/2.5V_{OUT}$/no load, the $4.0V_{IN}/2.5V_{OUT}$/1.5A load, $5.0V_{IN}/2.5V_{OUT}$/no load, and $5.0V_{IN}/2.5V_{OUT}$/1.5A load cases. All four plots show excellent stability over LDR through 150krad(Si), with a minimal anneal response for the biased samples and no anneal response for the grounded samples. The HDR curves show good stability over the 150krad(Si) irradiation but then show a substantial rebound of some 60mV over the +100°C/168h anneal. The grounded irradiation is worst case by a small margin. This 'rebound' behavior over high temperature biased anneal is typical of CMOS technology, and the ISL75052SEH is largely implemented in CMOS.

Quoting from MIL-STD-883 Test Method 1019: *'The accelerated annealing test provides an estimate of worst-case degradation of MOS microcircuits in LDR environments.'* The annealing test requirements includes a 50% overtest: *'Irradiate each test device to an additional 0.5-times the specified dose using the standard test conditions (3.1 through 3.10). Note that no electrical testing is required at this time.'*

While this language is not specific as to the exact (low) dose rate of interest in this estimation procedure, it is noted that the ISL75052SEH has been thoroughly tested at the TM1019 LDR of 0.01rad(Si)/s (see this report, with sample sizes of 18 and 20, respectively, for the biased and unbiased cases), and that there is hence no real need for 'estimates' of the LDR response. Additionally, the part is acceptance tested in production at LDR and HDR on a wafer-by-wafer basis, providing further radiation hardness assurance. Finally, TM1019 does not specify what constitutes a pass or fail situation for this procedure, which implies that it serves informational purposes only. We further note that the post-

rebound parametric values for the ISL75052SEH in no case exceeded the SMD post-radiation limits during these tests. The claimed utility of using post HDR anneals as a predictor of LDR performance is not confirmed by these results.

Figures 7 and 8 show line and load regulation at 2.5V output voltage, with the line voltage varying from 4.0V to 13.2V and the load current varying from 0A to 1.5A. Both parameters showed excellent stability with no measurable differences in response between the two dose rates and no anneal responses.

Figures 9 and 10 show the output voltage for the $10.5V_{IN}/10.0V_{OUT}$/no load and the $10.5V_{IN}/10.0V_{OUT}$/1.5A load cases and negative input bias current. As in Figures 3 through 6 we note the same substantial post HDR rebound of some 60mV over the +100°C/168h anneal. The LDR data showed excellent stability.

Figures 11 and 12 show line and load regulation at 10.0V output voltage, with the line voltage varying from 10.5V to 13.2V and the load current varying from 0A to 1.5A. Both parameters showed excellent stability with no measurable differences in response between the two dose rates and no anneal responses.

Figures 13 through 16 show the ground pin current for the $4.0V_{IN}/2.5V_{OUT}$/no load, the $4.0V_{IN}/2.5V_{OUT}$/1.5A load, $10.5V_{IN}/10.0V_{OUT}$/no load, and $10.5V_{IN}/10.0V_{OUT}$/1.5A load cases. This is a key parameter in LDO performance as it represents the operating current of the device and directly affects efficiency. The parameter showed excellent stability for all four conditions, with no measurable differences in response between the two dose rates and no annealing effects.

Figures 17 through 20 show the dropout voltage at $3.6V_{OUT}$/500 mA load current, $3.6V_{OUT}$/1500mA load current, $12.7V_{OUT}$/500mA load current, and $12.7V_{OUT}$/1500mA load current. This is again a key specification as it directly affects operating conditions and efficiency. The parameters showed excellent stability for all four conditions with no measurable differences in response between the two dose rates and no anneal responses.

Figures 21 and 22 show the VCCX pin voltage at $4.0V_{IN}$ and $13.2V_{IN}$, which represents the range of recommended input voltages. The VCCX pin represents the output of the on-chip 3.8V low dropout regulator used to provide a stable supply voltage for the rest of the chip's circuitry. See Figure 1 on page 2. Both parameters showed excellent stability with no measurable differences in response between the two dose rates. Interestingly, both the HDR and LDR samples showed a small anneal following irradiation.

Figure 23, enable turn-on delay: This plot shows the propagation delay from a 1.2V enable step to V_{OUT} = 100mV, representing the turn-on time of the regulator. The measurement is taken at $4.5V_{IN}$, $4.0V_{OUT}$, and 1.5A load current, with a load capacitor of 22µF and a bypass capacitor of 0.2µF. The parameter showed excellent stability with no measurable differences in response between the two dose rates and no annealing effects.

Figures 24 and 25, enable to PGOOD delay: These two plots show the propagation delay from enable to the PGOOD status flag, again measured at $4.5V_{IN}$, $4.0V_{OUT}$, and 1.5A load current, with a load capacitor of 22µF (Figure 20) or 200 µF (Figure 21) and a bypass capacitor of 0.2µF for both cases. Both parameters showed excellent stability with no measurable differences in response between the two dose rates and no annealing effects.

In conclusion, the ISL75052SEH showed good performance over LDR and HDR irradiation. All samples passed the post-irradiation specification limits at all down points including the accelerated anneal procedure. The output voltage showed some rebound after the accelerated anneal, but in no case did the post-anneal parametric values exceed the post-irradiation SMD limits. The part is acceptance tested on a wafer-by-wafer basis to 100krad(Si) at HDR (50 - 300rad(Si)/s) and to 50krad(Si) at LDR (0.01rad(Si)/s), ensuring hardness to the specified level for both dose rates. We observed no significant dose rate sensitivity, and in fact the output voltage data shows HDR to be somewhat worst case, which should not be an unexpected result for a largely CMOS component. No measurable differences in the total dose response were noted between biased and grounded irradiation for any parameters. Anneal responses were seen only in the HDR irradiated samples; the LDR samples showed no anneal response at all.

4. Appendices

Table 2. Reported Parameters and their Post-Irradiation Limits

Fig #	Parameter	Limit, Low	Limit, High	Unit	Notes
3	Output voltage, 4.0V_{IN}, 2.5V_{OUT}, no load	2.45	2.55	V	
4	Output voltage, 4.0V_{IN}, 2.5V_{OUT}, 1.5A load	2.45	2.55	V	
5	Output voltage, 5.0V_{IN}, 2.5V_{OUT}, no load	2.45	2.55	V	
6	Output voltage, 5.0V_{IN}, 2.5V_{OUT}, 1.5 load	2.45	2.55	V	
7	Line regulation, 2.5V_{OUT}	-8.0	8.0	mV	4.0V<V_{IN}<13.2V
8	Load regulation, 2.5V_{OUT}	-9.0	9.0	mV	0A<I_{LOAD}<1.5A
9	Output voltage, 10.5V_{IN}, 10.0V_{OUT}, no load	2.45	2.55	V	
10	Output voltage, 10.5V_{IN}, 10.0V_{OUT}, 1.5A load	2.45	2.55	V	
11	Line regulation, 10.0V_{OUT}	-10.0	10.0	mV	10.5V<V_{IN}<13.2V
12	Load regulation, 10.0V_{OUT}	-36.0	36.0	mV	0A<I_{LOAD}<1.5A
13	Ground pin current, 4.0V_{IN}, 2.5V_{OUT}, no load	-	10.0	mA	
14	Ground pin current, 4.0V_{IN}, 2.5V_{OUT}, 1.5A load	-	12.0	mA	
15	Ground pin current, 10.5V_{IN}, 10.0V_{OUT}, no load	-	20.0	mA	
16	Ground pin current, 10.5V_{IN}, 10.0V_{OUT}, 1.5A load	-	25.0	mA	
17	Dropout voltage, 3.6V_{OUT}, 500mA	-	160.0	mV	
18	Dropout voltage, 3.6V_{OUT}, 1500mA	-	400.0	mV	
19	Dropout voltage, 12.7V_{OUT}, 500mA	-	160.0	mV	
20	Dropout voltage, 12.7V_{OUT}, 1500mA	-	400.0	mV	
21	VCCX pin voltage, 4.0V_{IN}	3.7	4.1	V	
22	VCCX pin voltage, 13.2V_{IN}	3.7	4.1	V	
23	Enable turn-on delay	-	1000.0	µs	
24	Enable to PGOOD delay	-	2500.0	µs	C_{OUT} = 22µF
25	Enable to PGOOD delay	-	3000.0	µs	C_{OUT} = 200µF

5. Revision History

Rev.	Date	Description
1.00	Dec 12, 2018	Applied new formatting. Added reference to ISL73052SEH. Corrected sample sizes throughout the document. Add final low dose rate data throughout the document. Added Disclaimer
0.00	Jun 10, 2013	Initial release

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