ISL75054SLH

Single Event Effects (SEE) Testing of the ISL75054SLH Ultra Low Noise LDO

Introduction

The intense proton and heavy-ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Latch-Up (SEL), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of the SEE testing performed on the ISL75054SLH product. The ISL75054SLH is offered with radiation assurance screening to 75krad(Si) at 10mrad(Si)/s.

SEE Summary

SEE testing was performed with normal incidence gold for an LET of 86.3MeV·cm^2/mg at the surface of the device. The LET in the active silicon layer ranged from 88.7MeV·cm^2/mg to 90.9MeV·cm^2/mg. The range to Bragg peak was 51µm.

Additional testing was performed with normal incidence silver for an LET of 45.8MeV·cm^2/mg at the surface of the device. The LET in the active silicon layer ranged from 48.1MeV·cm^2/mg to 50.5MeV·cm^2/mg. The range to Bragg peak was 67.6µm.

The ISL75054SLH proved to be free of Destructive Single Event Effects (DSEE) under the following maximal parameter set at a die temperature of 125°C: V_{IN} = 27V, V_{PG} = 27V, and I_{OUT} = 1.1A at 86.3MeV·cm^2/mg and V_{IN} = 32V, V_{PG} = 32V, and I_{OUT} = 1.1A at 45.8MeV·cm^2/mg.

The LDO did not exhibited any V_{OUT} SET events during which V_{OUT} deviated beyond ±2% of its operating value.

A device was considered to have exhibited a PG SET when PG pulled low but the device did not enter fast-start and there was no hold time on PG. The device exhibited PG SETs with an average cross-section of 927.5µm^2 at 86.3MeV·cm^2/mg. PG, which operates at 5V, was less than 4.5V for at most 8.4µs during an event. The device did not exhibit PG SETs at 45.8MeV·cm^2/mg.

A SEFI was defined as an event in which PG pulled low and there was a loss of regulation in V_{OUT}. The ISL75054SLH did not exhibit SEFIs.

The results of this report apply to both the ISL75054SLHMF (ceramic) and the ISL75054SLHMVZ (plastic) as the parts were unpackaged for testing such that the bare silicon was exposed to the heavy ion beam.

Product Description

The ISL75054SLH is a radiation-hardened low dropout linear regulator with ultra-low noise, and high PSRR intended for ADC, RF, and other noise sensitive applications. The device has an operating supply voltage range of 2.7V to 30V and an output voltage range of 0.5V to VIN - VDO. The device supplies up to 1.0A of current at a typical 379mV dropout voltage. Built-in protection includes foldback, internal and externally programmable current limit, and over temperature protection. The ISL75054SLH features excellent noise performance and PSRR for radiation-hardened LDOs, with ultra-low RMS noise of 4µVRMS from 10Hz to 100kHz and ultrahigh PSRR of 101.5dB at 120Hz.

The ISL75054SLHMF is offered in a 10 Ld CDFP, and the ISL75054SLHMVZ is offered in a 16 LD HTSSOP. Both versions operate across the full-range military temperature of -55°C to +125°C

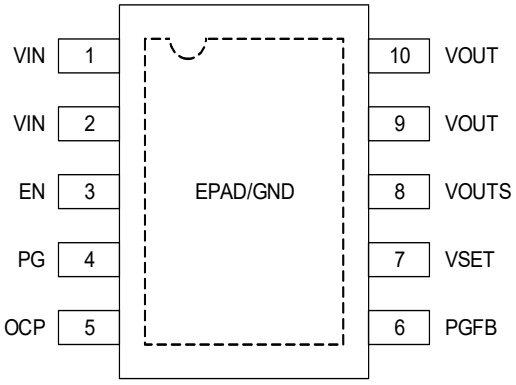

Figure 1. ISL75054SLHMF Pin Assignments

Table 1. ISL75054SLHMF Pin Descriptions

Pin Number	Pin Name	Description
1, 2	VIN	Input supply pins. V_{IN} range is from 2.7V to 30V. This pin requires sufficient input capacitance from V_{IN} to GND, 30µF is recommended and should be placed close to the device pins.
3	EN	Enable pin. When set above 1.14V nominally, the device is enabled.
4	PG	Power-Good output. This output is open-drain logic, connect a pull-up resistor to a logic supply or V_{IN}. For SEE mitigation, connect a 150pF capacitor from PG to GND. PG stays low and fast start-up functionality is disabled by connecting PGFB to V_{IN}.
5	OCP	Overcurrent protection. OCP allows the current limit to be programmed with an external resistor, R_{OCP}, between a typical range of 0.2A to 1.4A. Connect OCP directly to GND to set the maximum current limit. *Note*: The OCP pin sources a 530:1 ratio of the current out of V_{OUT}.
6	PGFB	Power-good feedback. To enable fast start-up functionality and power-good detection, connect an external resistor divider from V_{OUT} so that 665mV is provided to PGFB at the nominal output voltage. For SEE mitigation, connect a 470pF capacitor from V_{OUT} to PGFB. Connect PGFB to V_{IN} to disable fast start-up and PG functions when not required.
7	VSET	Voltage set. V_{SET} sources a precision 100µA current that flows through the external R_{SET} resistor to GND. V_{SET} sets the soft-start output voltage ramp rate through an external capacitor, C_{SET}, to GND. C_{SET} also provides filtering to internal device noise. Renesas recommends selecting C_{SET} between 0.47µF and 10µF.
8	VOUTS	Output voltage sense. V_{OUTS} is the non-inverting input to the error amplifier. Connect V_{OUTS} directly to the output capacitor.
9, 10	VOUT	Output voltage pins. A capacitance is required from V_{OUT} to GND, 30µF is recommended. V_{OUT} is set through a resistor from the V_{SET} pin to GND and can range from 0.5V to V_{IN} - V_{DO}.
-	EPAD	Ground. The EPAD is the electrical connection to GND and is additionally used as a heatsink.

Contents

1. SEE Testing

1.1 Objective

The testing was planned to find the limit of the input voltage set by the onset of DSEE at a LET of 86.3MeV·cm^2/mg (normal incidence gold) and 45.8MeV·cm^2/mg (normal incidence silver). Additional testing was planned to identify and quantify SETs and SEFIs occurring in the output voltage or on the PG pin of the ISL75054SLH. The SET studies included irradiation with normal incidence gold (86.3MeV·cm^2/mg). Testing was also performed at an LET of 45.8MeV·cm^2/mg (normal incidence silver) to determine the PG SET onset LET.

1.2 Facility

SEE testing was done at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute in College Station, Texas. This facility is coupled with a K500 superconducting cyclotron that can supply a wide range of ion species and flux. The SEE testing in this report was performed on October 17, 2024.

2. Results

2.1 DSEE Results

DSEE testing was performed to determine the maximum input supply voltage (V_{IN}) free from DSEEs at a die temperature of 125°C. The test board was laid out such that two parts could be irradiated simultaneously. During each run, the devices were exposed to heavy ions to a fluence of 1E7ions/cm^2. Testing was conducted in two sections, one with EN high and one with EN grounded.

For DSEE testing with EN high, I_{OUT} was set to 1.1A. V_{IN} was initially set to 26V and V_{OUT} was initially set to 25V. The values of V_{IN} and V_{OUT} were simultaneously increased by 1V following each run until a DSEE was observed or V_{IN} reached 32V and V_{OUT} reached 31V. Figure 2 shows the test schematic used for DSEE testing. To increase VIN and VOUT without making a board modification between runs V_{OUT} was set using an external power supply connected to V_{SET}. Due to this, PG and fast-start functionalities were disabled, however their circuit blocks were still on and had the opportunities to exhibit DSEE. A device was considered to have exhibited a DSEE if the output voltage at no load deviated by ±1%, the current on V_{IN} or PG at no load deviated by ±5%, or there was a loss of functionality.

DSEE testing was also performed with EN grounded to apply the maximum stress to the pass transistor as blocking mode is the worst-case condition for testing MOSFETs. For this testing, V_{OUT} was tied to ground and there was no load. The voltage on V_{IN} was increased by 1V following each run until a DSEE was observed or V_{IN} reached 32V. A device was considered to have exhibited a DSEE if the current on V_{IN} deviated by ±10%.

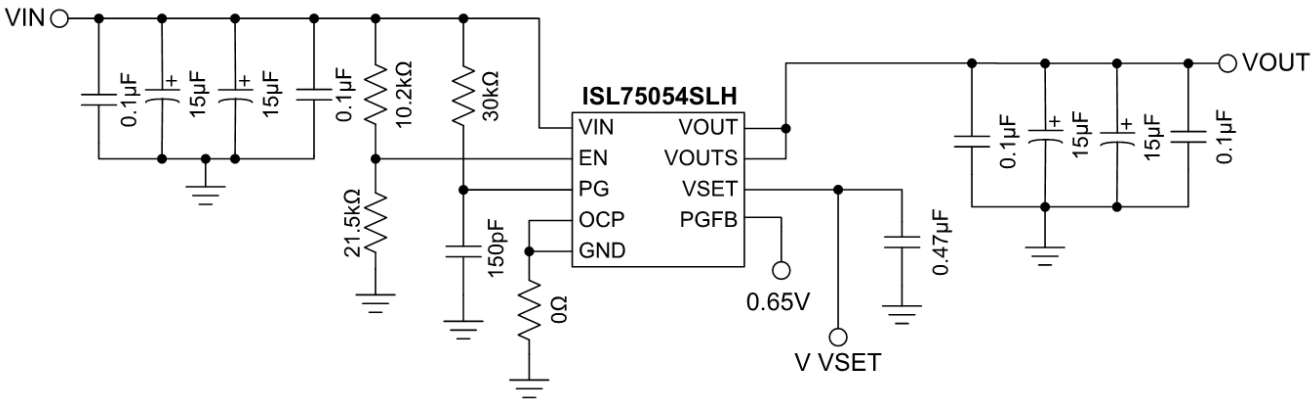

Figure 2. ISL75054SLH DSEE Test Schematic

2.1.1 LET = 86.3MeV·cm²/mg

Table 2 shows the results of DSEE testing with EN high at 86.3MeV·cm²/mg. Two of the four devices exhibited DSEEs when operated with V_{IN} = 28V. Those devices no longer regulated while under a load. DSEE testing indicates that the device should be operated with the following maximum parameter set to be robust against DSEE: V_{IN} = 27V, V_{PG} = 27V, and I_{OUT} = 1.1A at 125°C.

Table 2. ISL75054SLH DSEE with EN High Test Results at 86.3MeV·cm²/mg

V_{IN} / V_{PG} (V)	V_{OUT} (V)	I_{OUT} (A)	DUT #	Result	Notes	V_{OUT} (±1%)			I_{VIN} at I_{OUT} = 0A (±5%)			I_{PG} (±5%)		
						Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
26	25	1.1	1	Pass	-	24.98	24.99	0.02	2.16	2.16	0.00	0.133	0.133	0.00
			2	Pass	-	24.98	24.98	0.02	2.17	2.17	0.00	0.136	0.136	0.00
			3	Pass	-	24.98	24.98	0.00	2.14	2.14	0.00	0.137	0.137	0.00
			4	Pass	-	24.98	24.98	0.02	2.16	2.15	-0.46	0.137	0.137	0.00
27	26	1.1	1	Pass	-	25.99	25.98	0.00	2.34	2.32	-0.85	0.165	0.165	0.00
			2	Pass	-	25.98	25.98	0.00	2.21	2.19	-0.90	0.168	0.169	0.60
			3	Pass	-	25.98	25.98	0.00	2.16	2.16	0.00	0.169	0.170	0.59
			4	Pass	-	25.98	25.98	0.00	2.19	2.19	0.00	0.169	0.169	0.00
28	27	1.1	1	Fail	Does not regulate under load	26.98	26.98	0.00	2.84	2.95	3.91	0.198	0.197	-0.5
			2	Fail	Does not regulate under load	26.98	26.98	0.00	2.24	2.20	-1.79	0.201	0.201	0.00
			3	Pass	-	26.98	26.98	0.00	2.18	2.19	0.46	0.202	0.202	0.00
			4	Pass	-	26.98	26.98	0.00	2.21	2.22	0.45	0.202	0.202	0.00

Table 3 displays the results of DSEE testing with EN grounded for the ISL75054SLH. All four devices exhibited DSEEs when operated with V_{IN} = 28V. The devices had large increases in supply current. DSEE testing indicates that the device should be operated with the following maximum parameter set to be robust against DSEE: V_{IN} = 27V with EN = 0V at 125°C.

Table 3. ISL75054SLH DSEE with EN=0V Test Results at 86.3MeV·cm²/mg

V_{IN} (V)	V_{OUT} (V)	DUT #	Result	I_{VIN} (±10%)		
				Pre (µA)	Post (µA)	Δ (%)
25	Tied to GND	5	Pass	163	165	1.23
		6	Pass	171	173	1.17
		7	Pass	243	247	1.65
		8	Pass	401	398	-0.75
27	Tied to GND	5	Pass	169	165	-2.34
		6	Pass	176	166	-5.68
		7	Pass	246	249	1.22
		8	Pass	403	403	0.00
28	Tied to GND	5	Fail	168	15,000	8,828.57
		6	Fail	171	53,000	30,894.15
		7	Fail	252	28,000	11,011.11
		8	Fail	406	13,800	3,299.01

DSEE testing indicates that the ISL75054SLH should be operated with a maximum of V_{IN} = 27V, V_{PG} = 27V, and I_{OUT} = 1.1A at 125°C regardless of whether EN is high or low at 86.3MeV·cm²/mg.

2.1.2 LET = 45.8MeV·cm²/mg

Table 4 displays the results of DSEE testing with EN high at 45.8MeV·cm²/mg. All four devices passed when operated with V_{IN} = 32V. DSEE testing indicates that the device should be operated with the following maximum parameter set to be robust against DSEE: V_{IN} = 32V, V_{PG} = 32V, and I_{OUT} = 1.1A at 125°C.

Table 4. ISL75054SLH DSEE with EN High Test Results at 86.3MeV·cm²/mg

V_{IN} / V_{PG} (V)	V_{OUT} (V)	I_{OUT} (A)	DUT #	Result	V_{OUT} (±1%)			I_{VIN} at I_{OUT} = 0A(±5%)			I_{PG} (±5%)		
					Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
28	27	1.1	17	Pass	26.98	26.98	0.00	3.50	3.40	-2.86	0.203	0.203	0.00
			18	Pass	26.99	26.98	0.00	3.20	3.20	0.00	0.202	0.202	0.00
29	28	1.1	17	Pass	27.98	27.99	0.01	3.71	3.69	-0.54	0.235	0.235	0.00
			18	Pass	27.98	27.99	0.01	3.63	3.59	-1.10	0.235	0.235	0.00
30	29	1.1	17	Pass	28.99	28.99	0.00	3.72	3.73	0.27	0.267	0.267	0.00
			18	Pass	28.98	28.98	0.00	3.65	3.65	0.00	0.267	0.267	0.00
31	30	1.1	17	Pass	29.98	29.98	0.00	3.79	3.80	0.26	0.299	0.300	0.33
			18	Pass	29.98	29.98	0.00	3.72	3.76	1.08	0.299	0.301	0.67
			19	Pass	29.98	29.98	0.00	3.65	3.65	0.00	0.298	0.209	0.00
			20	Pass	29.98	29.98	0.00	3.71	3.71	0.00	0.300	0.300	0.00
32	31	1.1	17	Pass	30.98	30.98	0.00	3.82	3.83	0.26	0.323	0.323	0.00
			18	Pass	30.98	30.93	-0.17	3.78	3.81	0.79	0.324	0.324	0.00
			19	Pass	30.98	30.98	0.00	3.69	3.72	0.81	0.343	0.343	0.00
			20	Pass	30.98	30.98	0.00	3.75	3.77	0.53	0.324	0.324	0.00

Table 5 displays the results of DSEE testing with EN grounded at 45.8MeV·cm^2/mg. All four devices passed with V_{IN} = 32V. DSEE testing indicates that the device should be operated with the following maximum parameter set to be robust against DSEE: V_{IN} = 32V with EN = 0V at 125°C.

Table 5. ISL75054SLH DSEE with EN=0V Test Results at 45.8MeV·cm^2/mg

V_{IN} (V)	V_{OUT} (V)	DUT #	Result	I_{VIN} (±10%)		
				Pre (µA)	Post (µA)	Δ (%)
31	Tied to GND	21	Pass	904	911	0.77
		22	Pass	955	957	0.21
		23	Pass	645	642	-0.47
		24	Pass	349	351	0.93
32	Tied to GND	21	Pass	914	914	0.00
		22	Pass	958	958	0.00
		23	Pass	646	652	0.93
		24	Pass	353	355	0.57

DSEE testing indicates that the ISL75054SLH should be operated with a maximum of V_{IN} = 32V, V_{PG} = 32V, and I_{OUT} = 1.1A at 125°C regardless of whether EN is high or low at 45.8MeV·cm^2/mg.

2.2 SET Results

2.2.1 LET = 86.3MeV·cm^2/mg

Figure 3 shows the test schematic used for SET testing. VOUT was set using the R_{SET} resistor, and PG and fast-start were enabled. The voltage on PG was pulled up to 5V and PGFB was set using a voltage divider. A 30kΩ pull-up resistor and 150pF capacitor to ground were applied to PG and a 470pF capacitor was connected from V_{OUT} to PGFB for SEE mitigation. The test board was laid out such that two parts could be irradiated simultaneously.

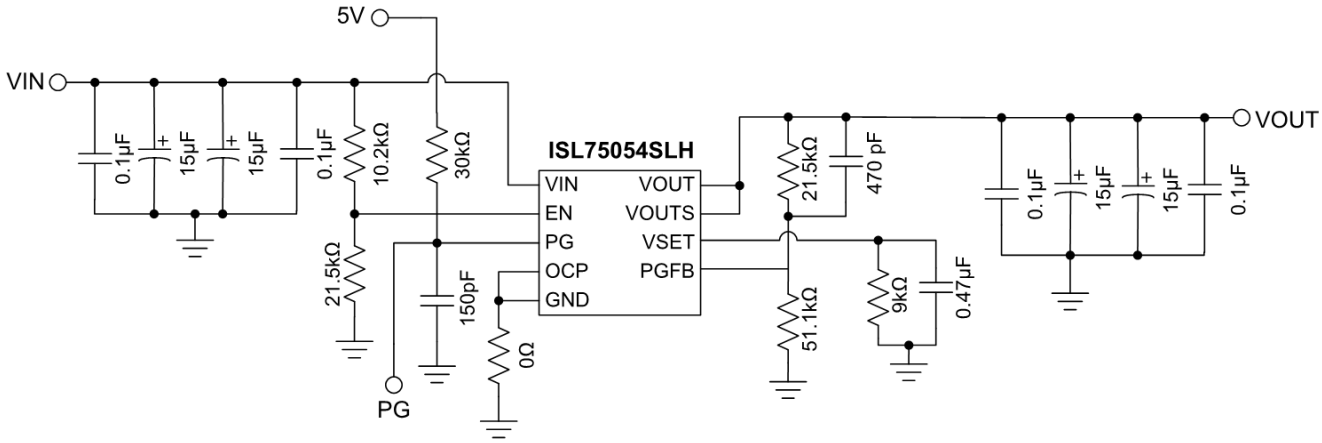

Figure 3. ISL75054SLH SET Test Schematic

For SET testing, devices were tested under three different test conditions as given in Table 6 at an ambient temperature of 25°C. During each run, the devices were exposed to heavy ions to a fluence of 1E7ions/cm^2. Devices were monitored for V_{OUT} SETs, PG SETs, and SEFIs. A device exhibited a V_{OUT} SET when V_{OUT} deviated beyond ±2% of its operating value. A device exhibited a PG SET when PG pulled low but the device did not enter fast-start and there was no hold time on PG. The device exhibited a SEFI when PG pulled low and there

was a loss of V_{OUT} regulation. The device then would spontaneously recover with a normal fast-start. V_{OUT} SETs were captured with a trigger set to capture events in which V_{OUT} deviated beyond ±2% of its operating value. PG SETs and SEFIs were captured with a trigger set to capture events in which PG dropped by 0.5V.

Table 6. ISL75054SLH SET Test Conditions

Test Condition	Number of Devices Tested	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (mA)
#1	4	2.7	0.9	1000
#2	4	5	0.9	440
#3	4	27	0.9	69

The results of SET testing for the ISL75054SLH are displayed in Table 7.

Table 7. ISL75054SLH SET Test Results at 86.3MeV·cm²/mg

Test Condition	V_{IN} (V)	DUT #	Fluence (ions/cm²)	# of V_{OUT} SETs	# of PG SETs	# of SEFIs
#1	2.7	9	1.0E7	0	0	0
		10	1.0E7	0	0	0
		11	1.0E7	0	0	0
		12	1.0E7	0	0	0
#2	5	9	1.0E7	0	93	0
		10	1.0E7	0	92	0
		11	1.0E7	0	105	0
		12	1.0E7	0	81	0
#3	27	9	1.0E7	0	0	0
		10	1.0E7	0	0	0
		11	1.0E7	0	0	0
		12	1.0E7	0	1	0

The results are summarized in Table 8.

Table 8. ISL75054SLH SET Test Summary at 86.3MeV·cm²/mg

Test Condition	# of DUTs	Total Fluence (ions/cm²)	# of V_{OUT} SETs	V_{OUT} SET σ (µm²)	# of PG SETs	PG SET σ (µm²)	# of SEFIs	SEFI σ (µm²)
#1	4	4.0E7	0	2.5	0	2.5	0	2.5
#2	4	4.0E7	0	2.5	371	927.5	0	2.5
#3	4	4.0E7	0	2.5	1	2.5	0	2.5

No V_{OUT} SETs or SEFIs were observed during testing.

Figure 4 shows an example of a typical PG SET capture. During all the PG SETs, PG pulled to GND and then recovered according to the RC time constant. V_{OUT} was unaffected by the event.

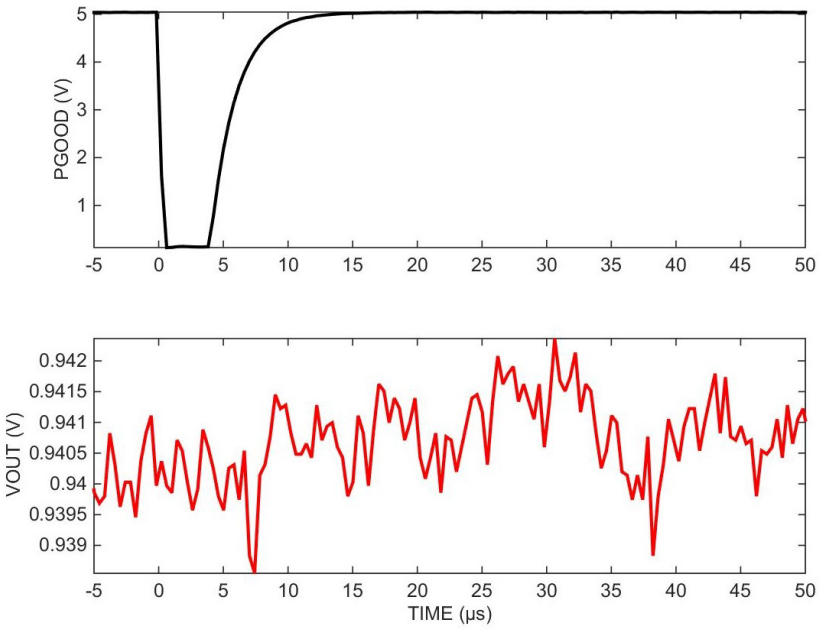

Figure 4. ISL75054SLH Typical PG SET Capture in TC #2

The PG SET recovery times, which were defined as the duration PG is less than 4.5V, for each event in TC #2 are displayed in Figure 5. The longest recovery time in TC #2 was 8.4µs.

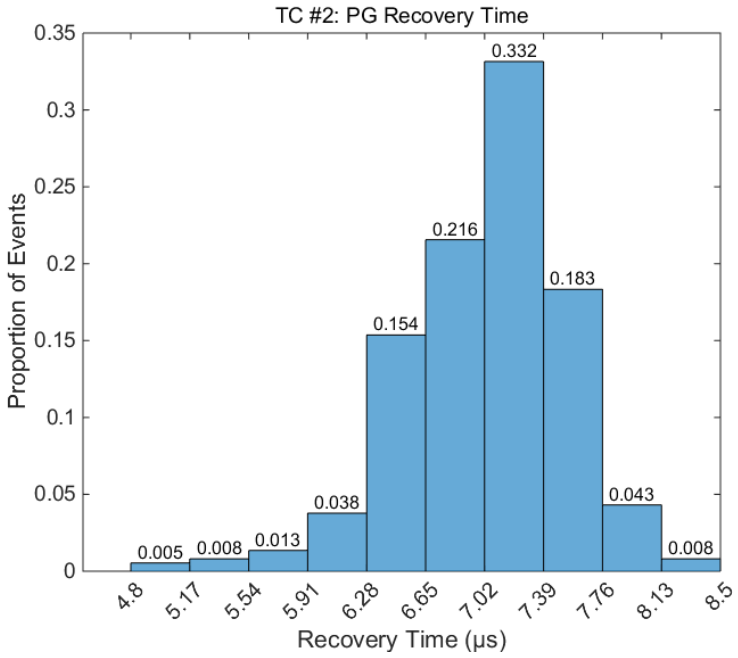

Figure 5. ISL75054SLH TC #2 PG SET Recovery Time

There was only one PG SET in TC #3. That event had a recovery time of 5.2µs.

2.2.2 LET = 45.8MeV·cm^2/mg

Additional SET testing was performed under the same three test conditions at an ambient temperature of 25°C and an LET of 45.8MeV·cm^2/mg to determine the PG SET onset LET. The results for the LET = 45.8MeV·cm^2/mg testing are displayed in Table 9.

Table 9. ISL75054SLH SET Test Results at 45.8MeV·cm^2/mg

Test Condition	V_{IN} (V)	DUT #	Fluence (ions/cm^2)	# of VOUT SETs	# of PG SETs	# of SEFIs
#1	2.7	13	1.0E7	0	0	0
		14	1.0E7	0	0	0
		15	1.0E7	0	0	0
		16	1.0E7	0	0	0
#2	5	13	1.0E7	0	0	0
		14	1.0E7	0	0	0
		15	1.0E7	0	0	0
		16	1.0E7	0	0	0
#3	27	13	1.0E7	0	0	0
		14	1.0E7	0	0	0
		15	1.0E7	0	0	0
		16	1.0E7	0	0	0

The results are summarized in Table 10.

Table 10. ISL75054SLH SET Test Summary at 45.8MeV·cm^2/mg

Test Condition	# of DUTs	Total Fluence (ions/cm^2)	# of VOUT SETs	VOUT SET σ (µm^2)	# of PG SETs	PG SET σ (µm^2)	# of SEFIs	SEFI σ (µm^2)
#1	4	4.0E7	0	2.5	0	2.5	0	2.5
#2	4	4.0E7	0	2.5	0	2.5	0	2.5
#3	4	4.0E7	0	2.5	0	2.5	0	2.5

Testing indicates that the onset LET for PG SETs is at least 45.8MeV·cm^2/mg. Overall, given the short duration of the events and the high onset LET, these PG SETs pose little risk to a system.

3. Discussion and Conclusion

SEE testing was performed with normal incidence gold for an LET of 86.3MeV·cm^2/mg and normal incidence silver for an of 45.8MeV·cm^2/mg.

Testing indicated that the maximal parameter set to be robust against DSEE is: V_{IN} = 27V, V_{PG} = 27V and I_{OUT} = 1.1A at 86.3MeV·cm^2/mg and V_{IN} = 32V, V_{PG} = 32V and I_{OUT} = 1.1A at 45.8MeV·cm^2/mg.

No V_{OUT} SETs or SEFIs were observed during testing.

PG SETs were observed when testing at 86.3MeV·cm^2/mg. The average cross-section for PG SETs was 927.5µm^2, and the longest duration event was 8.4µs. It was determined that onset LET for PG SETs was at least 45.8MeV·cm^2/mg. A worst-case error rate calculation using CREME96 for GEO during solar minimum and using 100mils of aluminum shielding can be performed using a step-function with a saturation value of 927.5µm^2 and a onset LET of 45.8MeV·cm^2/mg. This gives an error rate of one PG SET every 2,488 years. Given the short duration of the events and the rarity of the events occurring, PG SETs pose little risk to a system.

4. Revision History

Revision	Date	Description
1.00	Jul 23, 2025	Initial release.

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