ISL71840SEH, ISL73840SEH

Total Dose Testing

TR010
Rev.1.0
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Introduction

This document provides results of a Low Dose Rate (LDR) and High Dose Rate (HDR) total dose test of the ISL71840SEH and ISL73840SEH 16-channel analog multiplexers. The test was conducted in order to determine the sensitivity of the part to the total dose environment and to determine if any dose rate sensitivity exists. HDR testing under bias is complete through 150krad(Si) and the subsequent high temperature biased anneal while LDR testing with samples under bias and with all pins grounded is complete through 100krad(Si).

The ISL73840SEH is a ISL71840SEH variant that is total dose rated and acceptance tested for 50krad(Si) at LDR only. The data presented in this report applies equally to the ISL73840SEH, which differs in total dose rating and lot acceptance testing.

Reference Documents

- MIL-STD-883 test method 1019
- ISL71840SEH datasheet
- ISL73840SEH datasheet
- Standard Microcircuit Drawing (SMD) 5962-15219

Part Description

The ISL7x840SEH is a radiation hardened 16-channel analog multiplexer that is fabricated using Renesas' proprietary P6SOI (Silicon on Insulator) process to mitigate single-event effects and improve total ionizing dose performance. The part operates from a dual supply voltage ranging from ±10.8V to ±16.5V and has four address inputs and an ENABLE pin that can be driven with adjustable logic thresholds to select 1 of 16 available channels. An inactive channel is separated from an active channel by high impedance, which inhibits any interaction between them. The low switch ON-resistance (r_{ON}) of the ISL7x840SEH allows improved signal integrity and reduced power losses. The ISL7x840SEH is also designed for cold sparing making it suitable for high reliability applications that have redundancy requirements. The part is designed to provide a high impedance to the analog source while in a powered OFF condition, making it easy to add additional backup devices without loading signal sources. The ISL7x840SEH also incorporates input analog overvoltage protection up to ±35V, which disables the switch to protect downstream devices. All inputs are Electrostatic Discharge (ESD) protected to 8kV Human Body Model (HBM). The ISL7x840SEH is available in a 28 Ld flatpack or in die form and operates across the extended temperature range of -55°C to +125°C.

As the ISL7x840SEH is the third version of the part, a brief historical note may be in order. The first Renesas 16-channel multiplexer was the HS-1840RH. This part was built in an early dielectrically isolated metal gate CMOS process. The key to hardening a metal gate process at the time was the gate metal deposition, which must be performed using a flash evaporator. In the 1995 time frame this by then obsolete equipment became difficult to maintain and the metal gate process could no longer be supported. As a result the HS-1840RH was obsoleted.

The HS-1840RH was followed by the HS-1840ARH, which was designed in the later RSG process and was developed in order to continue supplying this very popular part, which performs a key function in many space systems. As part of the redesign the HS-1840ARH gained some functionality made possible by the bipolar devices available in RSG, which the metal gate process did not support. Bipolar circuit blocks in the HS-1840ARH included the on-chip voltage reference, the digital input ESD network and the VDD and VSS ESD nets.

The ISL7x840SEH is the subject of the present report and was designed as an updated version of the HS-1840ARH, with improvements in the switch ON-resistance and in cold sparing capabilities.

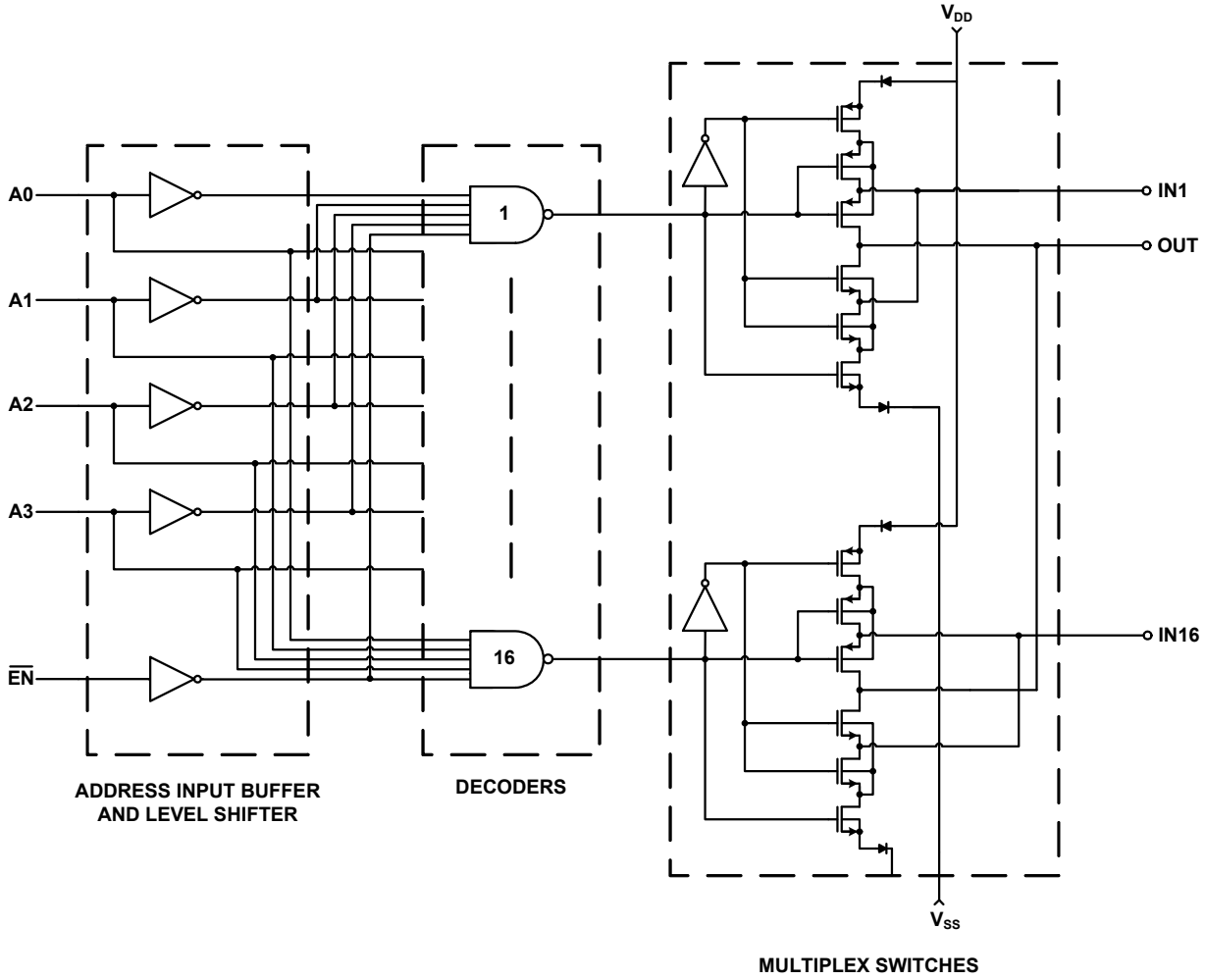

FIGURE 1. ISL7x840SEH BLOCK DIAGRAM

Test Description

Irradiation Facilities

HDR testing was performed using a Gamma cell 220 ^{60}Co irradiator located in the Palm Bay, Florida Renesas facility. LDR testing was performed using a Hopewell Designs N40 panoramic LDR ^{60}Co irradiator located in the same facility. The HDR irradiations were performed at 69.72rad(Si)/s and the LDR work was performed at 0.0089rad(Si)/s (8.9mrad(Si)/s), both in accordance with MIL-STD-883 Method 1019. The LDR exposures used a PbAl box to shield the test board and devices under test against low energy secondary gamma radiation.

Test Fixturing

Figure 2 on page 3 shows the configuration and power supply sequencing used for biased irradiation.

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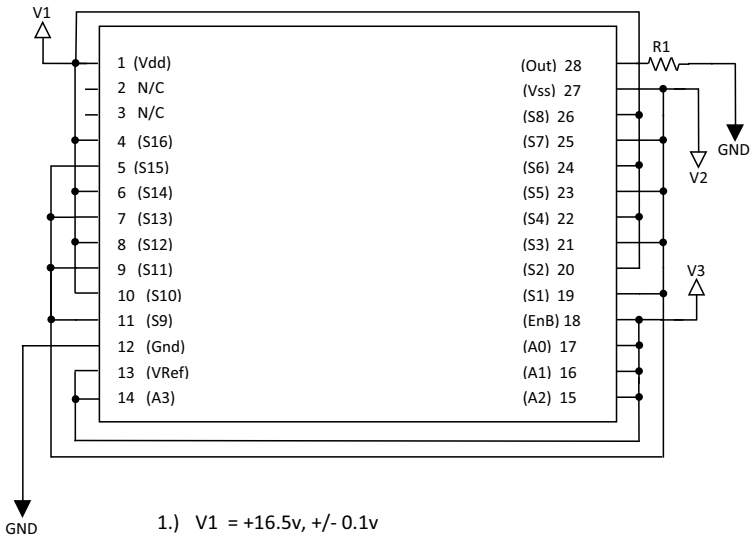
ISL71840 (HDR/LDR) Mask # 54252A01



1.) V1 = +16.5v, +/- 0.1v
2.) V2 = -16.5v, +/-0.1v
3.) V3 = +5.5v, +/-0.1v
4.) R1 = 1kOhm, +/-5%, ¼ Watt (Per socket)
5.) Socket is 28 pin flatpack (Sensata 628-0282315)
6.) Power up sequence is V1, V2, V3.
7.) Reverse order for power down(V3, V2, V1).

FIGURE 2. IRRADIATION BIAS CONFIGURATION AND POWER SUPPLY SEQUENCING FOR THE ISL7x840SEH

Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using production Automated Test Equipment (ATE) with data logging of all parameters at each downpoint. Downpoint electrical testing was performed at room temperature.

Experimental Matrix

Testing proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of four samples irradiated at HDR under bias, four samples irradiated at LDR with all pins grounded and four samples irradiated at LDR under bias, (three control units were used).

Samples of the ISL7x840SEH were drawn from development lot J67669 (wafers 1 and 2) as part of the routine wafer-by-wafer acceptance testing procedure and were packaged in the production hermetic 28-pin ceramic flatpack package outline K28.A. The samples were processed through the standard burn in cycle and were screened to the SMD 5962-15219 limits at room, low and high temperatures before irradiation.

Downpoints

Downpoints to date for the LDR tests were zero, 10krad(Si), 30krad(Si), 50krad(Si), 75krad(Si) and 100krad(Si). Downpoints for the HDR test were zero, 30krad(Si), 50krad(Si), 100krad(Si) and 150krad(Si). The HDR samples were subjected to a high temperature biased anneal for 168 hours at 100°C following irradiation.

Results

Attributes Data

Testing at HDR under bias of the ISL7x840SEH is complete and showed no reject devices after irradiation to 150krad(Si) or after the post-150krad(Si) irradiation anneal. Testing at LDR under bias and grounded is complete through 100krad(Si) and showed no reject devices after irradiation to that level. Table 1 on page 4 summarizes the results.

TABLE 1. ISL7x840SEH TOTAL DOSE TEST ATTRIBUTES DATA

DOSE RATE	BIAS	SAMPLE SIZE	DOWNPOINT	BIN 1	REJECTS
0.0089rad(Si)/s	Figure 2	4	Preirradiation	4	
			10krad(Si)	4	0
			30krad(Si)	4	0
			50krad(Si)	4	0
			75krad(Si)	4	0
			100krad(Si)	4	0
0.0089rad(Si)/s	Grounded	4	Preirradiation	4	
			10krad(Si)	4	0
			30krad(Si)	4	0
			50krad(Si)	4	0
			75krad(Si)	4	0
			100krad(Si)	4	0
69.72rad(Si)/s	Figure 2	4	Preirradiation	4	
			30krad(Si)	4	0
			50krad(Si)	4	0
			100krad(Si)	4	0
			150krad(Si)	4	0
			Anneal, 168 hours at 100°C	4	0

NOTES:

1. Bin 1 indicates a device that passes all pre-irradiation specification limits.
2. The 168 hours anneal was performed at 100°C using the bias configuration shown in Figure 2.

Variables Data

The plots in Figures 3 through 41 show data at all downpoints to date. The plots show the median of key parameters as a function of total dose for each of the four irradiation conditions. Many of the plots show the total dose response of the average of parameters such as ON resistance and the various leakage parameters for each of the 16 channels in order to facilitate the interpretation of the results as well as managing the length of this report. All samples showed excellent stability over irradiation, with no observed dose rate sensitivity. See the conclusion on page 25 for further discussion.

Variables Data Plots

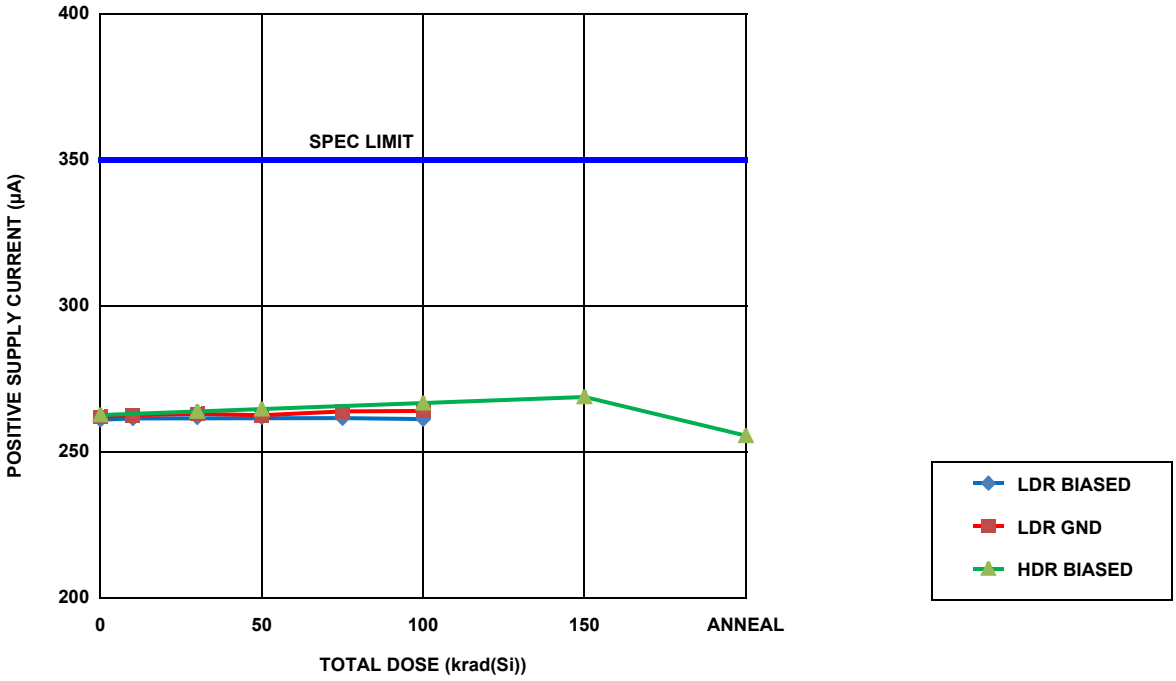


FIGURE 3. ISL7x840SEH positive supply current as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 350µA maximum.

Variables Data Plots (Continued)

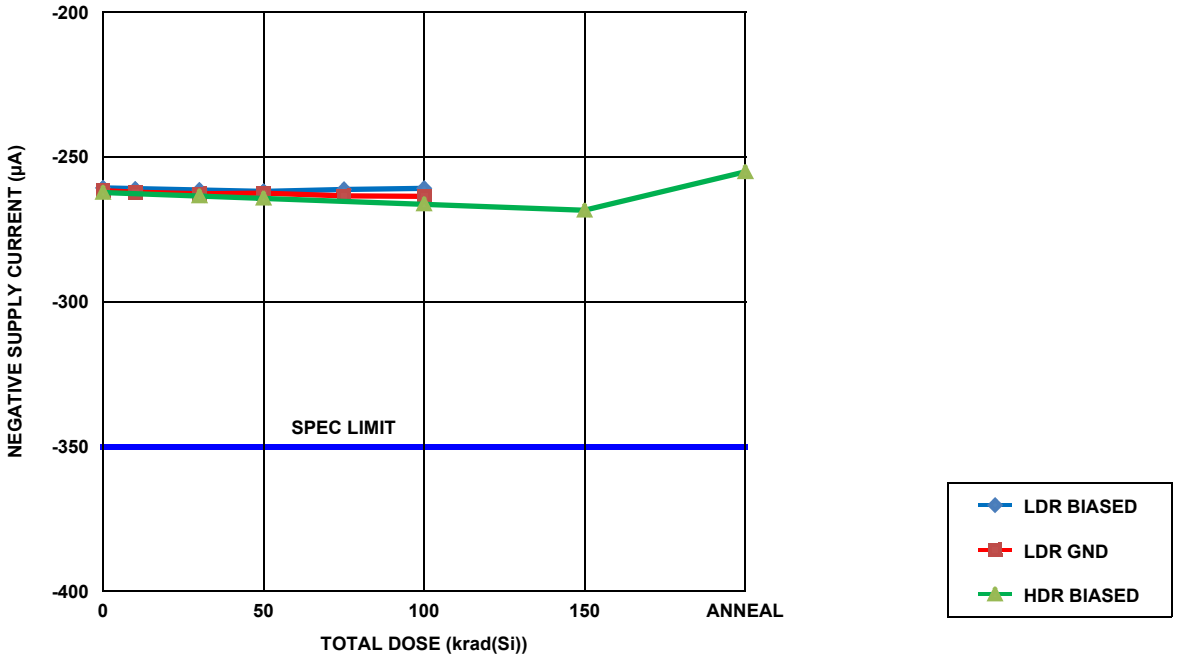


FIGURE 4. ISL7x840SEH negative supply current as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is -350µA minimum.

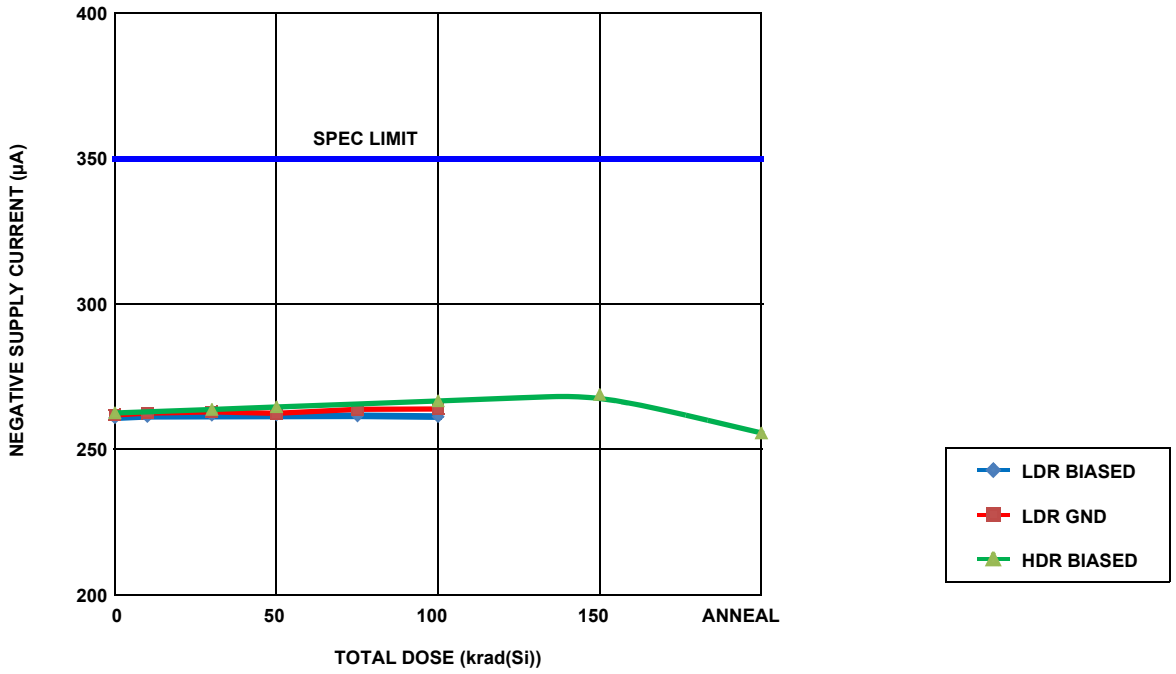


FIGURE 5. ISL7x840SEH positive standby current as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 350µA maximum.

Variables Data Plots (Continued)

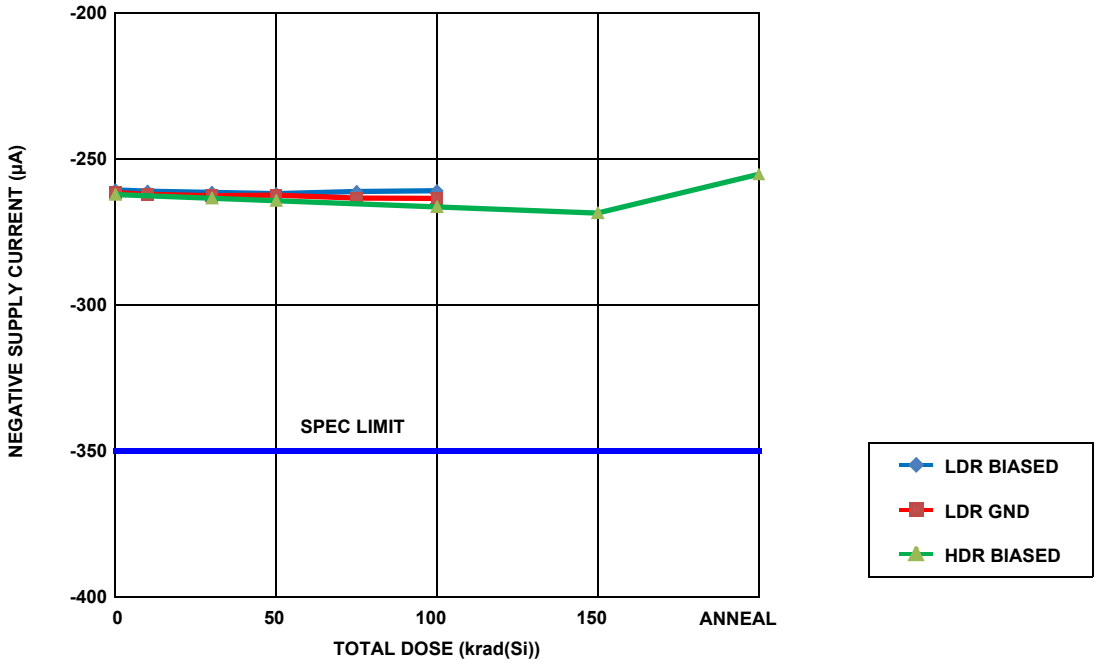


FIGURE 6. ISL7x840SEH negative standby current as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is -350µA minimum.

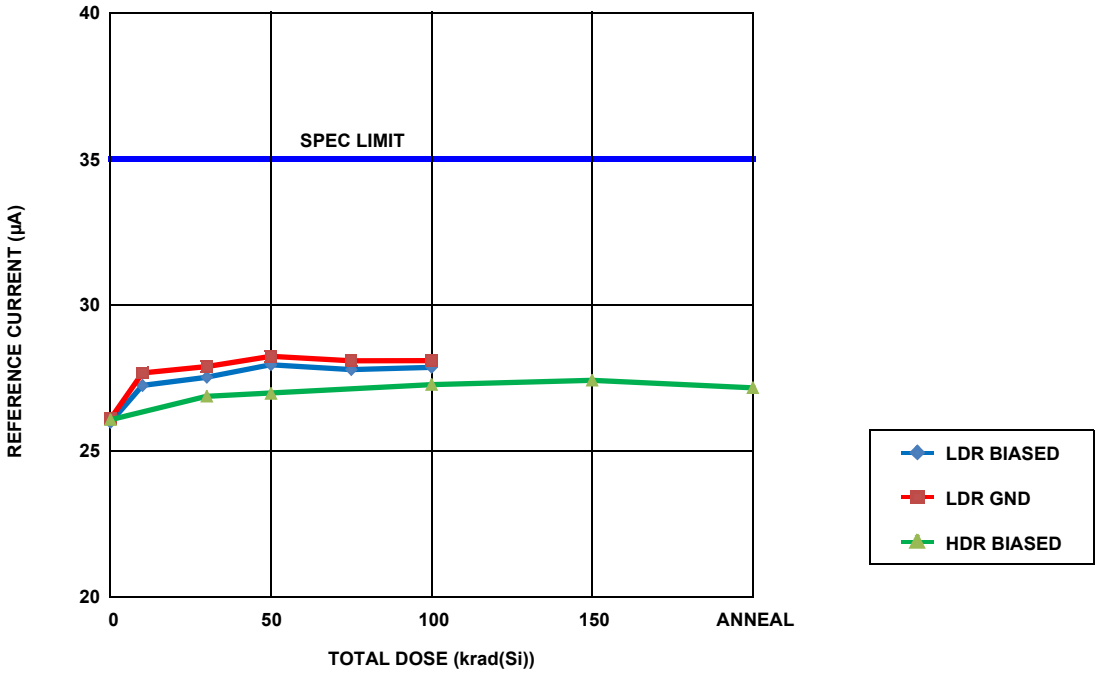


FIGURE 7. ISL7x840SEH reference current as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 35µA maximum.

Variables Data Plots (Continued)

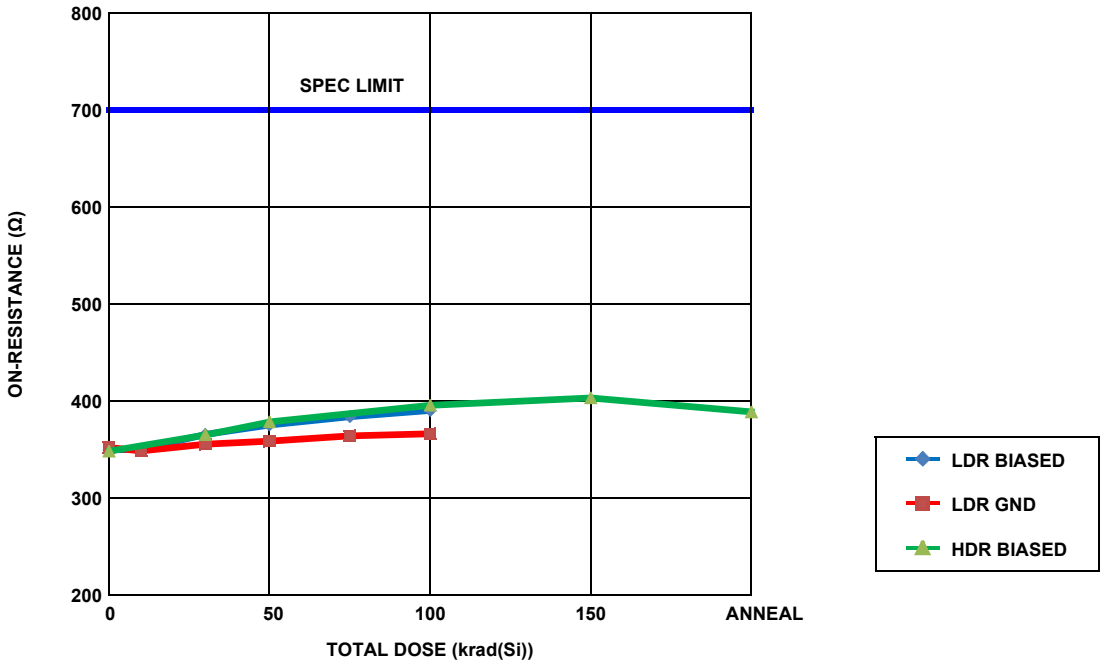


FIGURE 8. ISL7x840SEH ON-resistance, average of all 16 channels, ±15V supplies, 1.0mA output current, 5V input voltage, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 700Ω maximum.

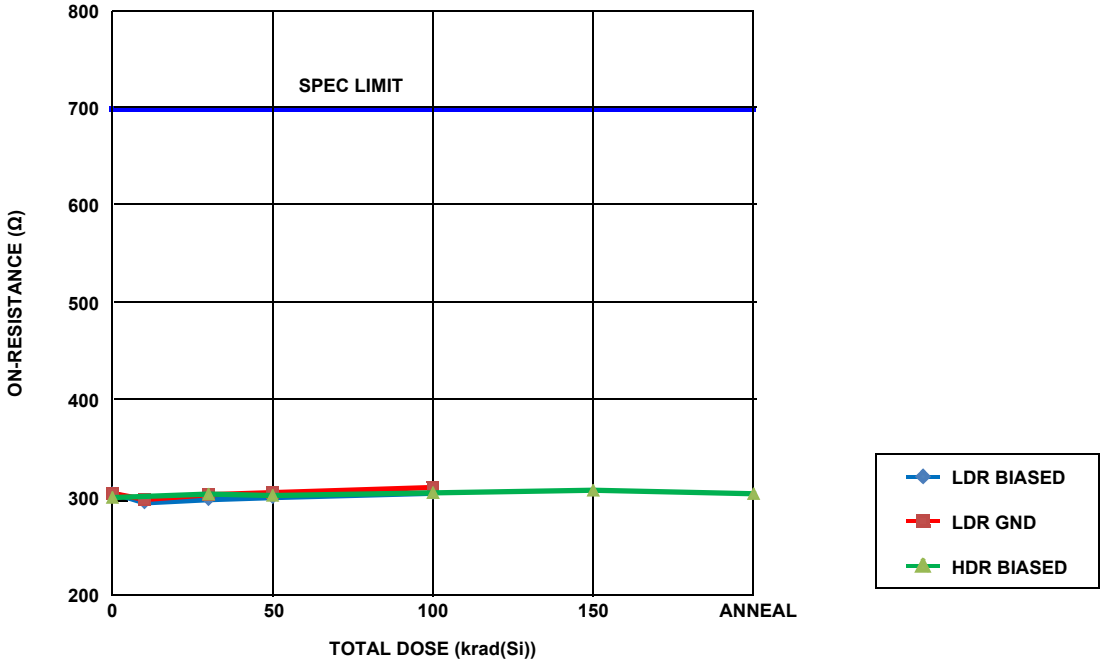


FIGURE 9. ISL7x840SEH ON-resistance, average of all 16 channels, ±15V supplies, 1mA output current, -5V input voltage, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 700Ω maximum.

Variables Data Plots (Continued)

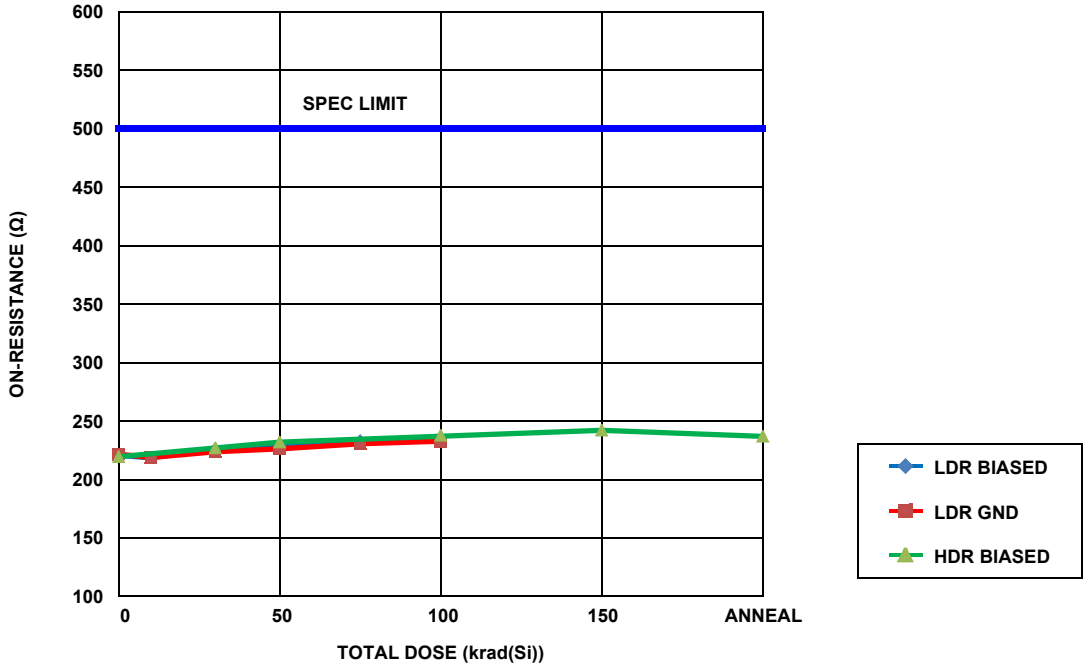


FIGURE 10. ISL7x840SEH ON-resistance, average of all 16 channels, ±15V supplies, 1mA output current, 15V input voltage, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 500Ω maximum.

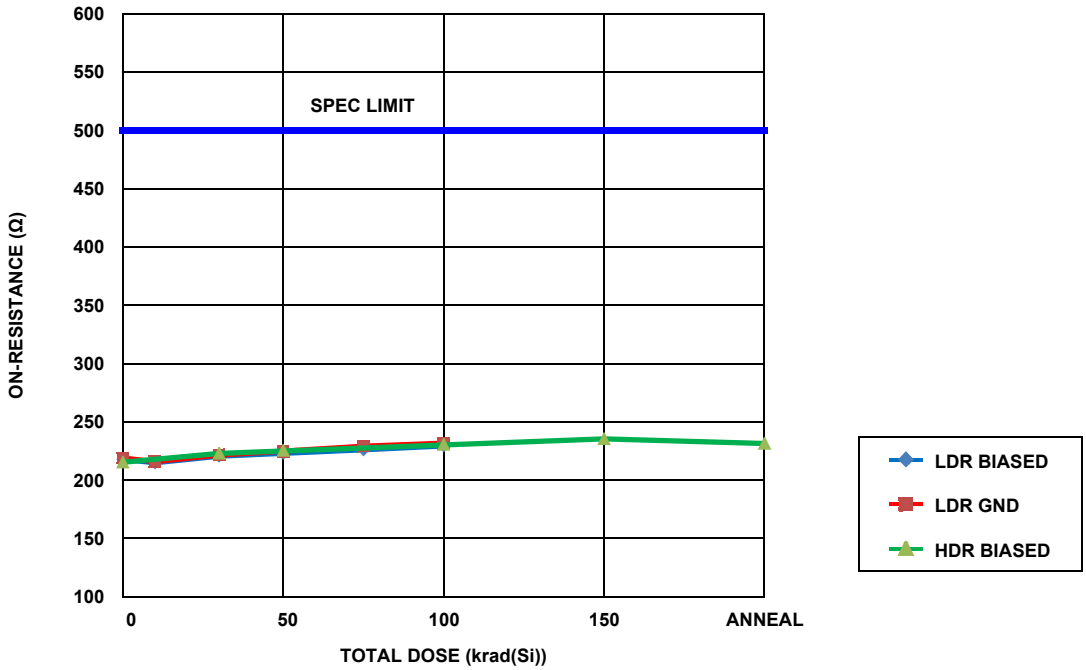


FIGURE 11. ISL7x840SEH ON-resistance, average of all 16 channels, ±15V supplies, 1mA output current, -15V input voltage, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 500Ω maximum.

Variables Data Plots (Continued)

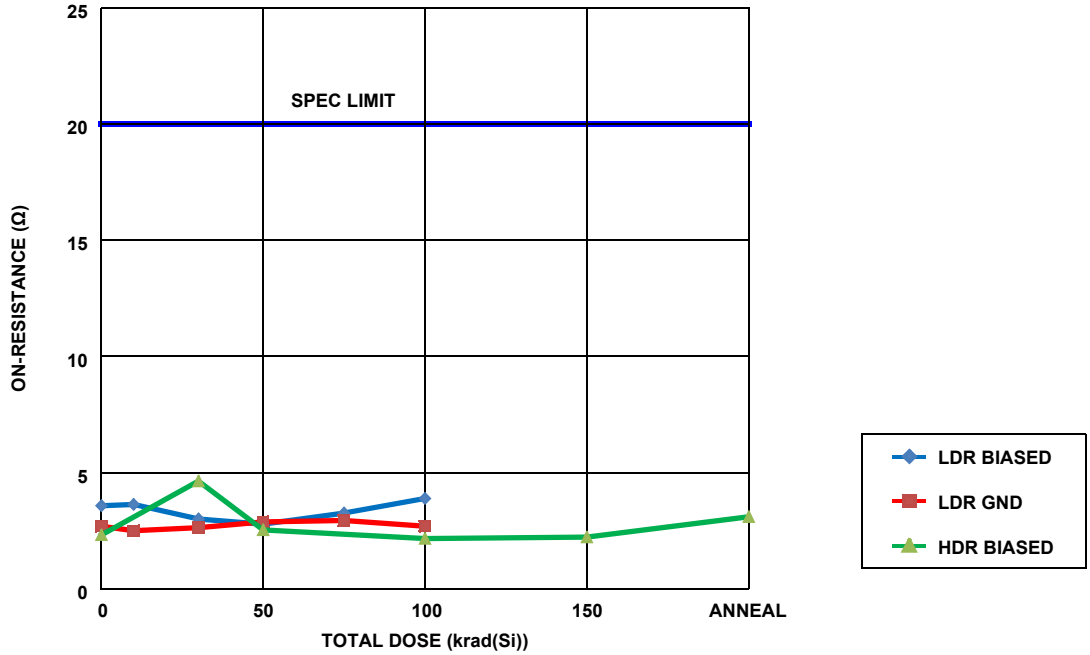


FIGURE 12. ISL7x840SEH ON-resistance match, average of all 16 channels, ±15V supplies, -1mA output current, +5V input voltage, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 20Ω maximum.

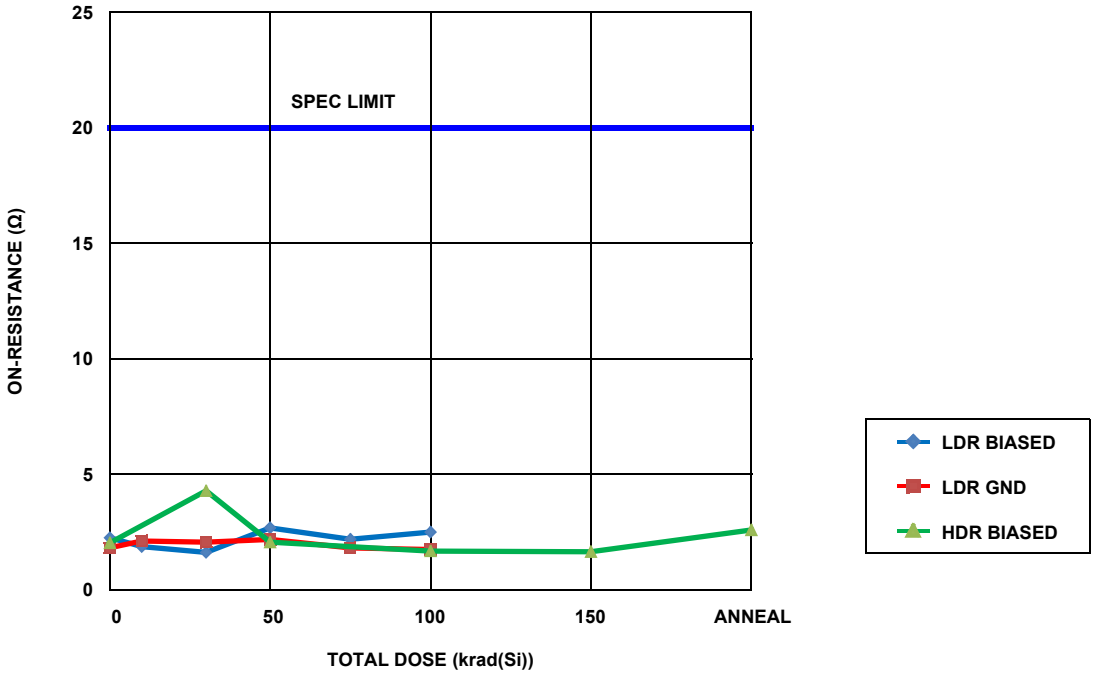


FIGURE 13. ISL7x840SEH ON-resistance match, average of all 16 channels, ±15V supplies, -1mA output current, -5V input voltage, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 20Ω maximum.

Variables Data Plots (Continued)

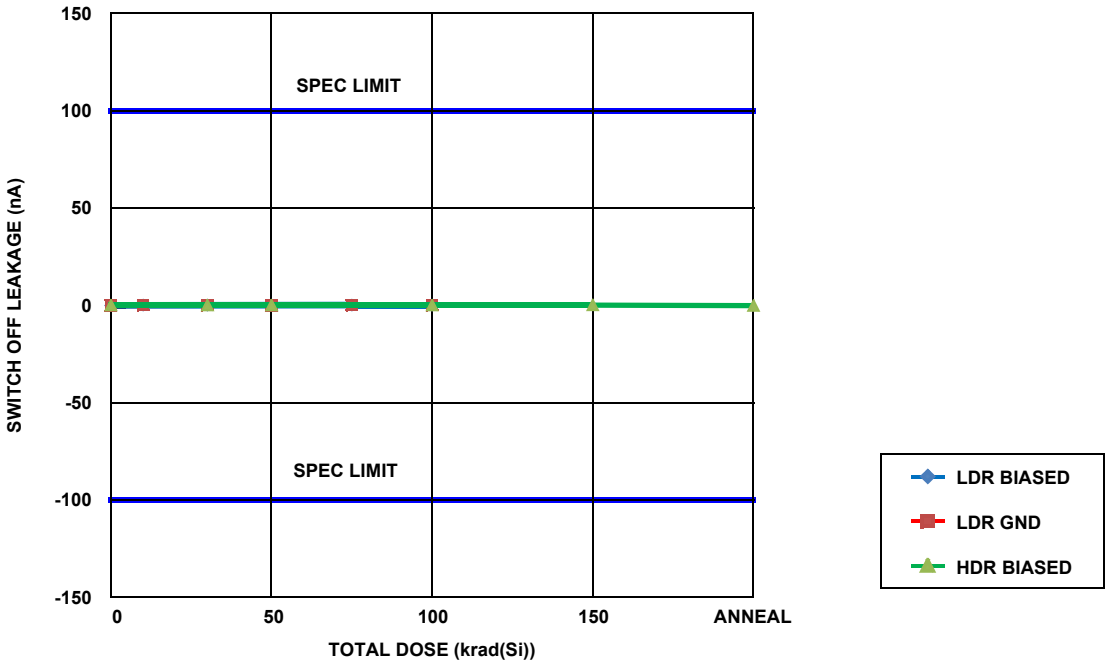


FIGURE 14. ISL7x840SEH switch OFF leakage ($I_{S(OFF)}$) into the source of an unselected channel, average of all 16 channels, supply voltage ±15V, input voltage +11.5V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -100nA to 100nA.

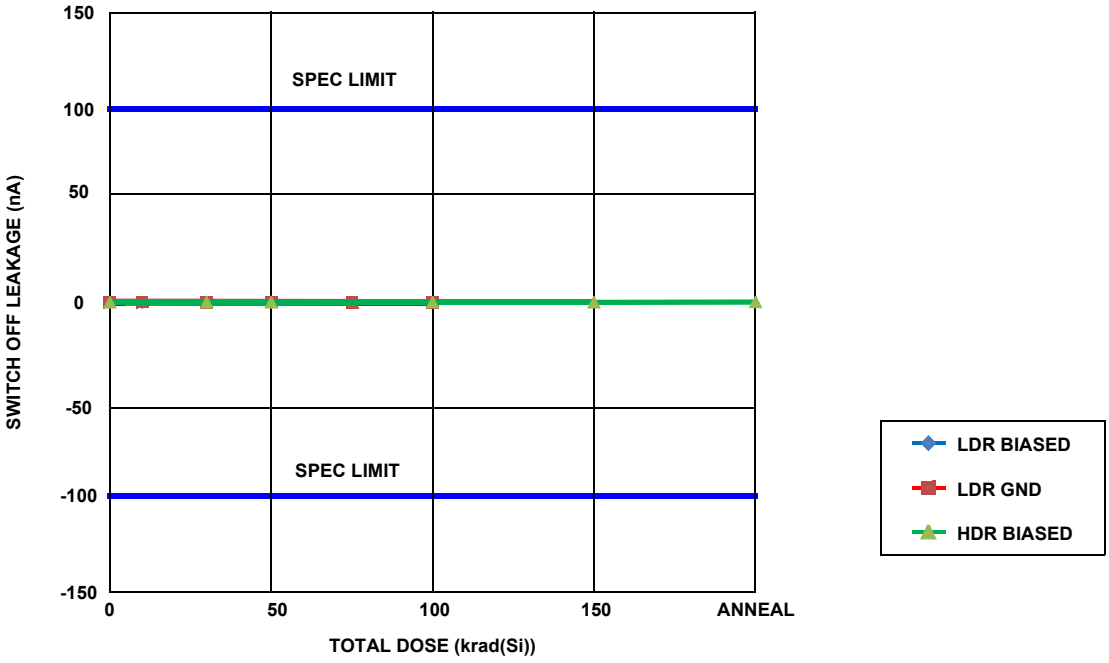


FIGURE 15. ISL7x840SEH switch OFF leakage ($I_{S(OFF)}$) into the source of an unselected channel, average of all 16 channels, supply voltage ±15V, input voltage -11.5V as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -100nA to 100nA.

Variables Data Plots (Continued)

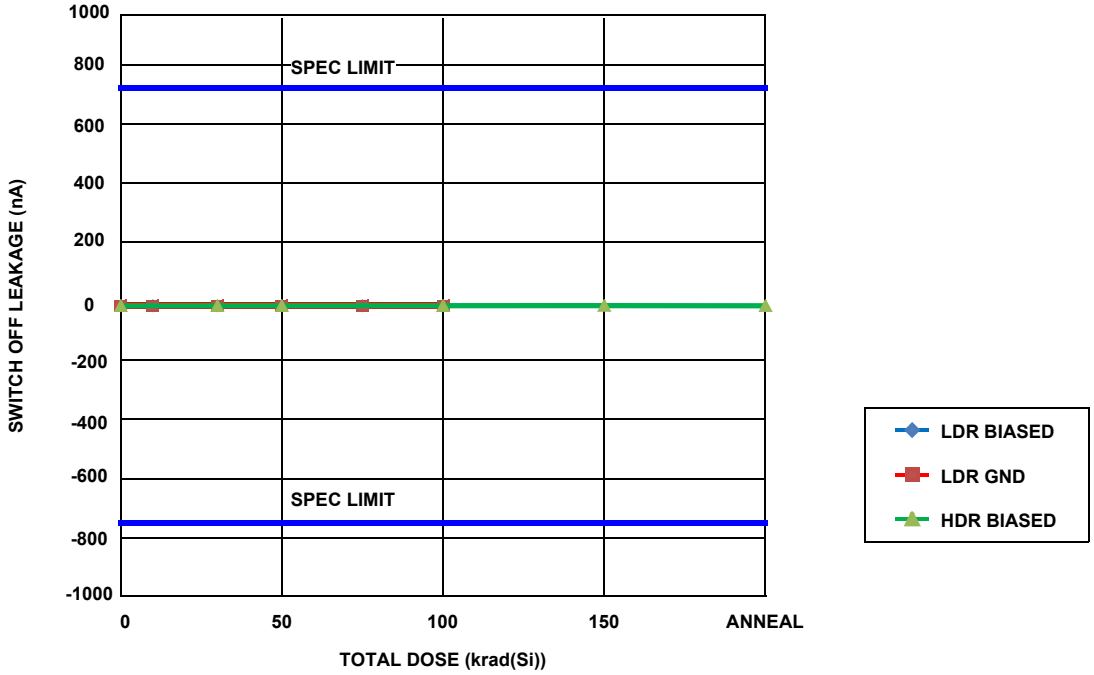


FIGURE 16. ISL7x840SEH switch OFF leakage ($I_{S(OFF)}$) into the source of an unselected channel, average of all 16 channels, supply voltage ±15V, input overvoltage +35V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -750nA to +750nA.

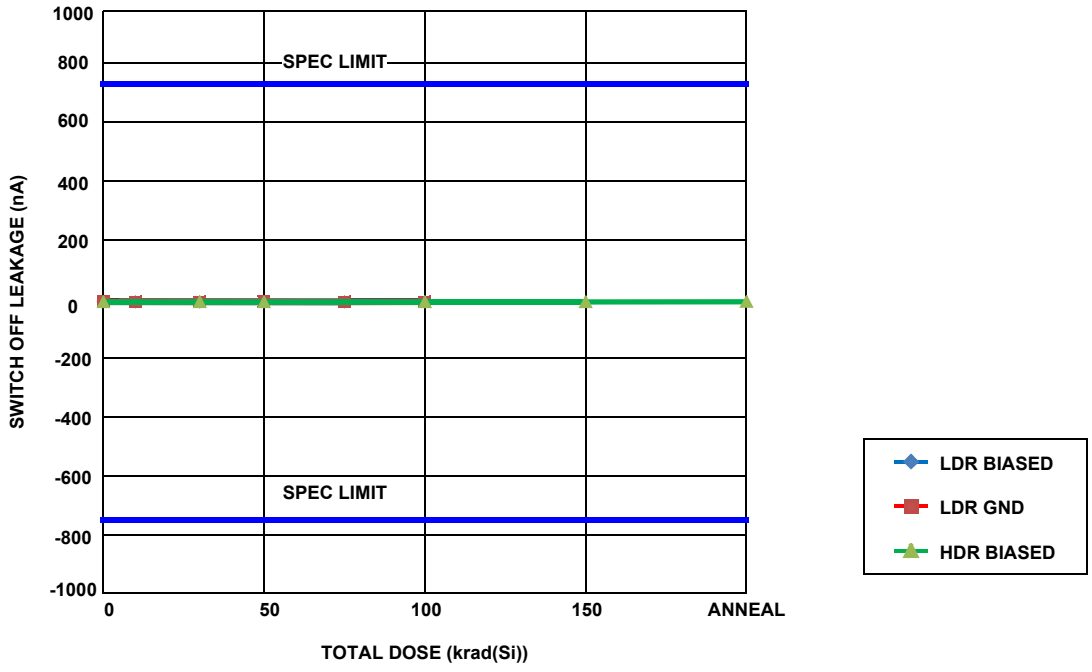


FIGURE 17. ISL7x840SEH switch OFF leakage ($I_{S(OFF)}$) into the source of an unselected channel, average of all 16 channels, supply voltage ±15V, input overvoltage -35V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -750nA to +750nA.

Variables Data Plots (Continued)

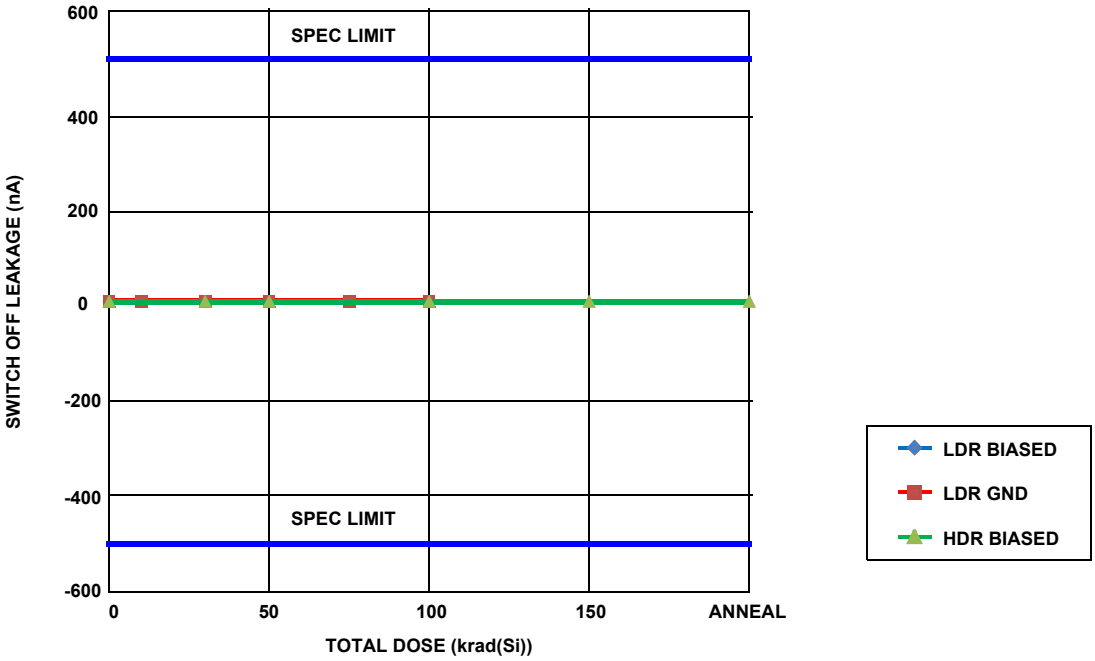


FIGURE 18. ISL7x840SEH switch OFF leakage ($I_{D(OFF)}$) into the drain of an unselected channel, supply voltage ±15V, input overvoltage +35V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -500nA to +500nA.

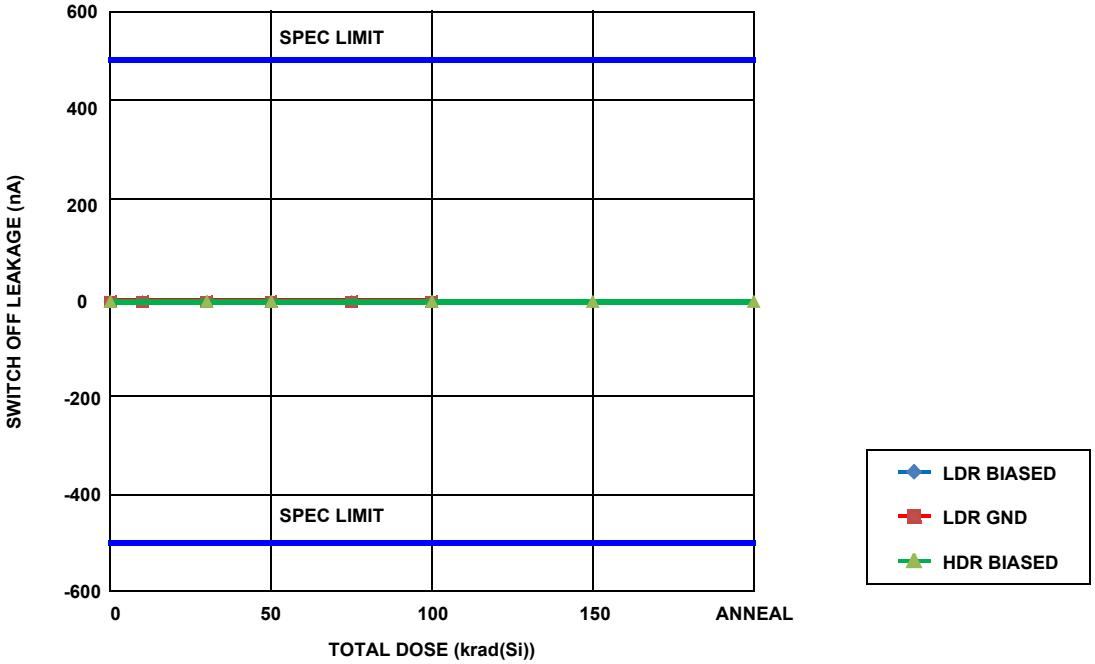


FIGURE 19. ISL7x840SEH switch OFF leakage ($I_{D(OFF)}$) into the drain of an unselected channel, supply voltage ±15V, input overvoltage -35V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -500nA to +500nA.

Variables Data Plots (Continued)

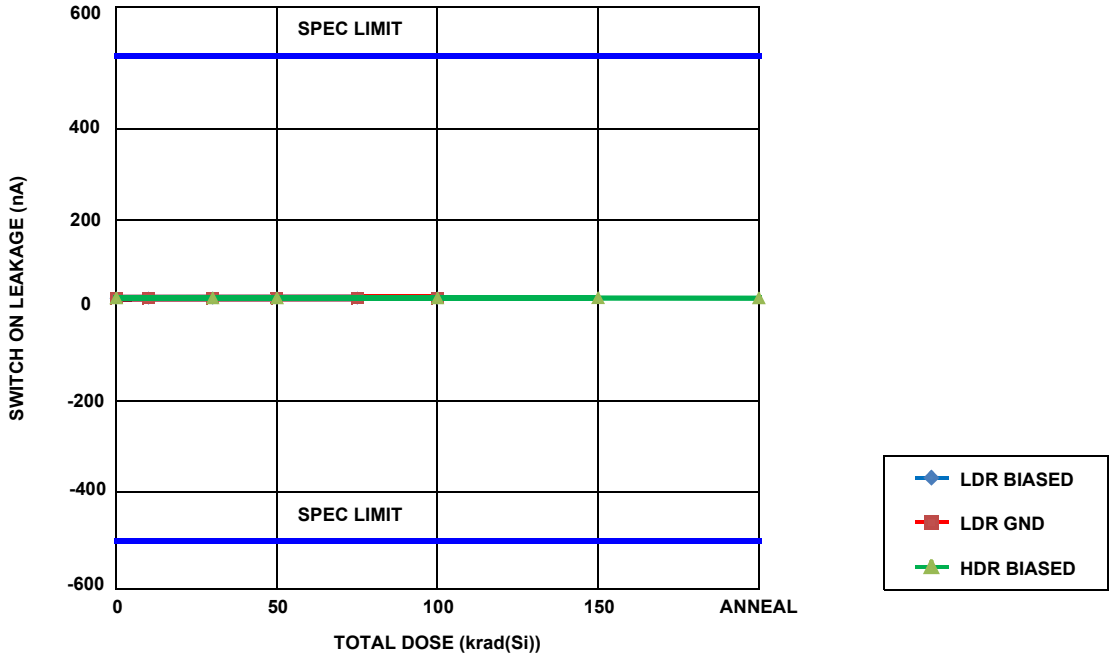


FIGURE 20. ISL7x840SEH switch ON leakage ($I_{S(ON)}$) into the source of a selected channel, average of all 16 channels, supply voltage ±15V, input overvoltage +35V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -500nA to +500nA.

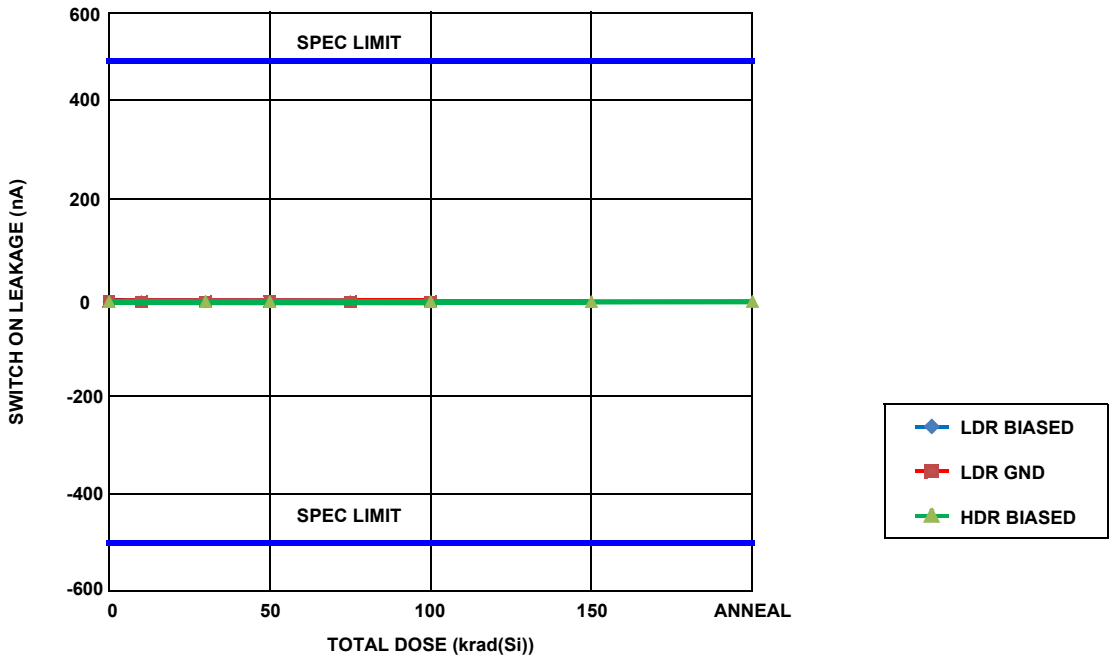


FIGURE 21. ISL7x840SEH switch ON leakage ($I_{S(ON)}$) into the source of a selected channel, average of all 16 channels, supply voltage ±15V, input overvoltage -35V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -500nA to +500nA.

Variables Data Plots (Continued)

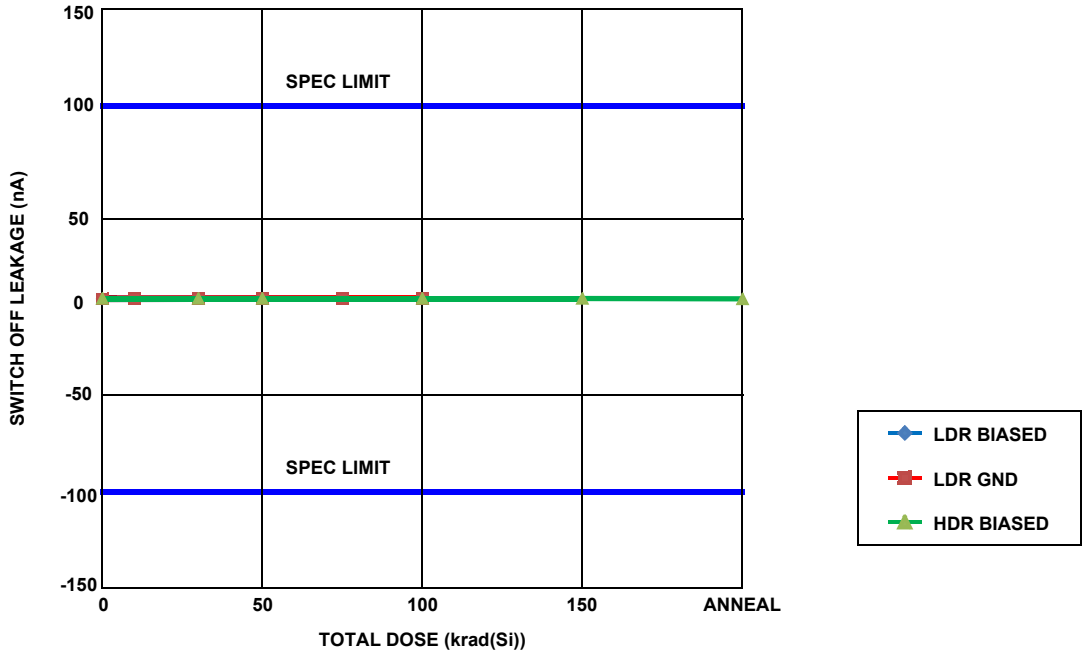


FIGURE 22. ISL7x840SEH switch OFF leakage ($I_{S(OFF)}$) into the source of an unselected channel, average of all 16 channels, with supply, address and ENABLE pins open, input voltage +25V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -100nA to +100nA.

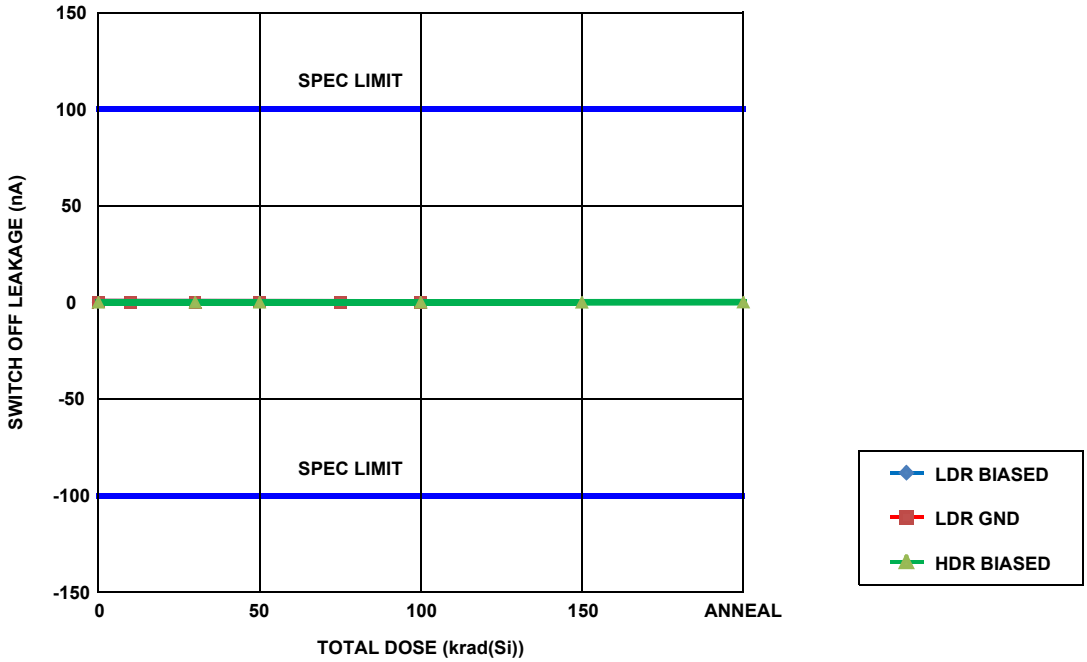


FIGURE 23. ISL7x840SEH switch OFF leakage ($I_{S(OFF)}$) into the source of an unselected channel, average of all 16 channels, with supply, address and ENABLE pins open, input voltage -25V as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -100nA to +100nA.

Variables Data Plots (Continued)

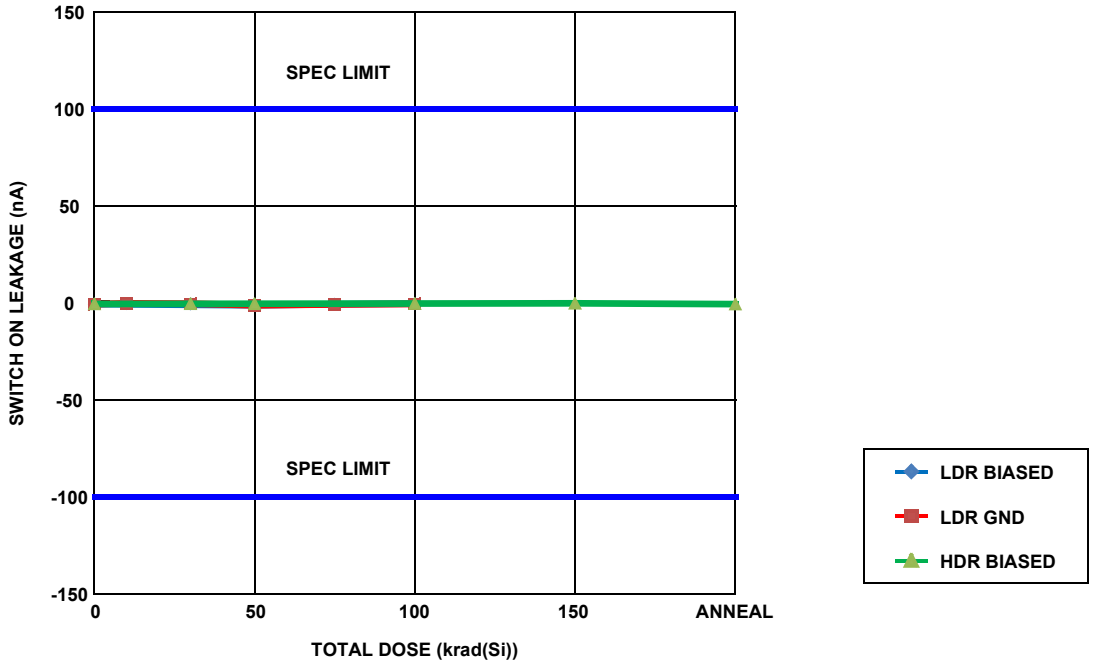


FIGURE 24. ISL7x840SEH switch ON leakage ($I_{D(ON)}$) into the source and drain of a selected channel, average of all 16 channels, supply voltage ±15V, input and output voltage 10V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -100nA to +100nA.

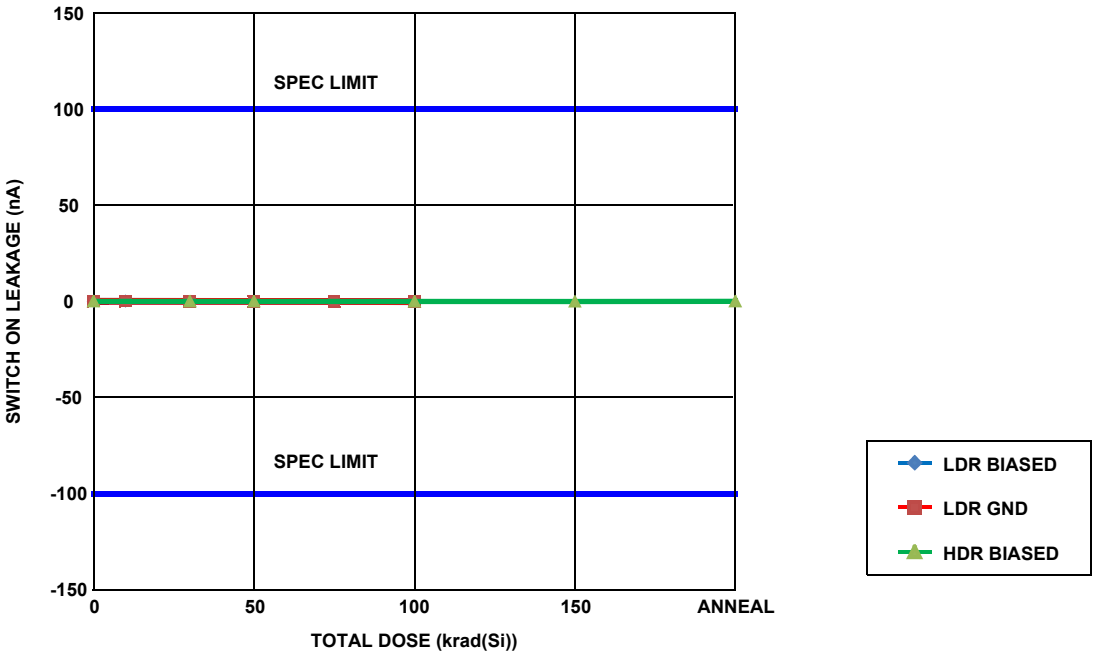


FIGURE 25. ISL7x840SEH switch ON leakage ($I_{D(ON)}$) into the source and drain of a selected channel, average of all 16 channels, supply voltage ±15V, input and output voltage -10V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -100nA to +100nA.

Variables Data Plots (Continued)

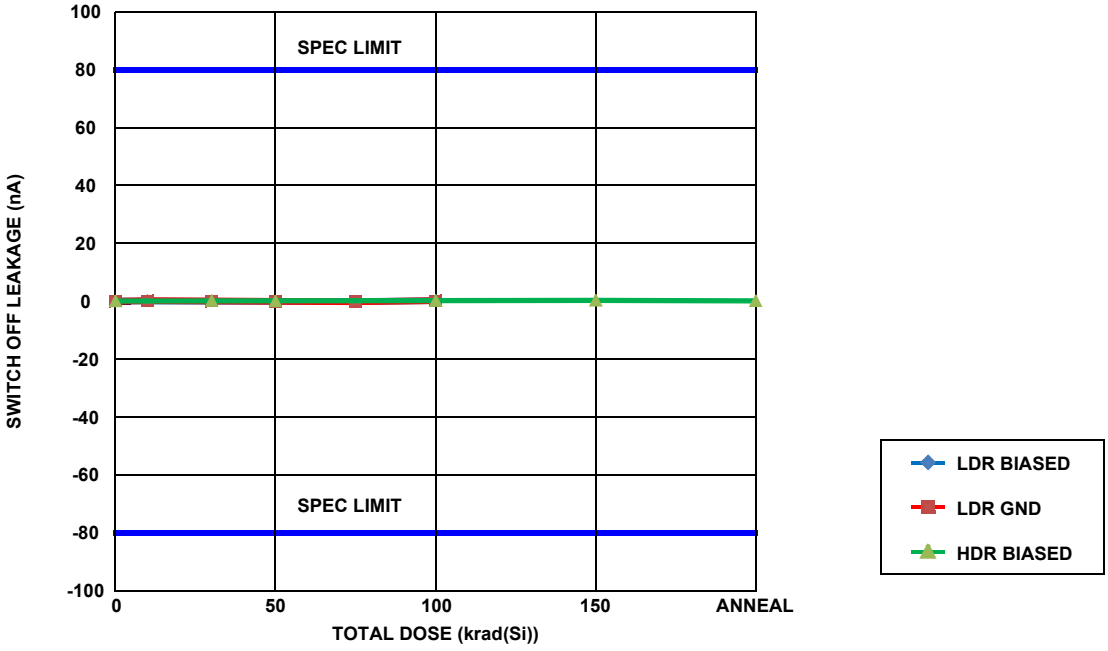


FIGURE 26. ISL7x840SEH switch OFF leakage ($I_{D(OFF)}$) into the drain with the part disabled, supply voltage ±15V, output voltage +10V, input voltage -10V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -80nA to +80nA.

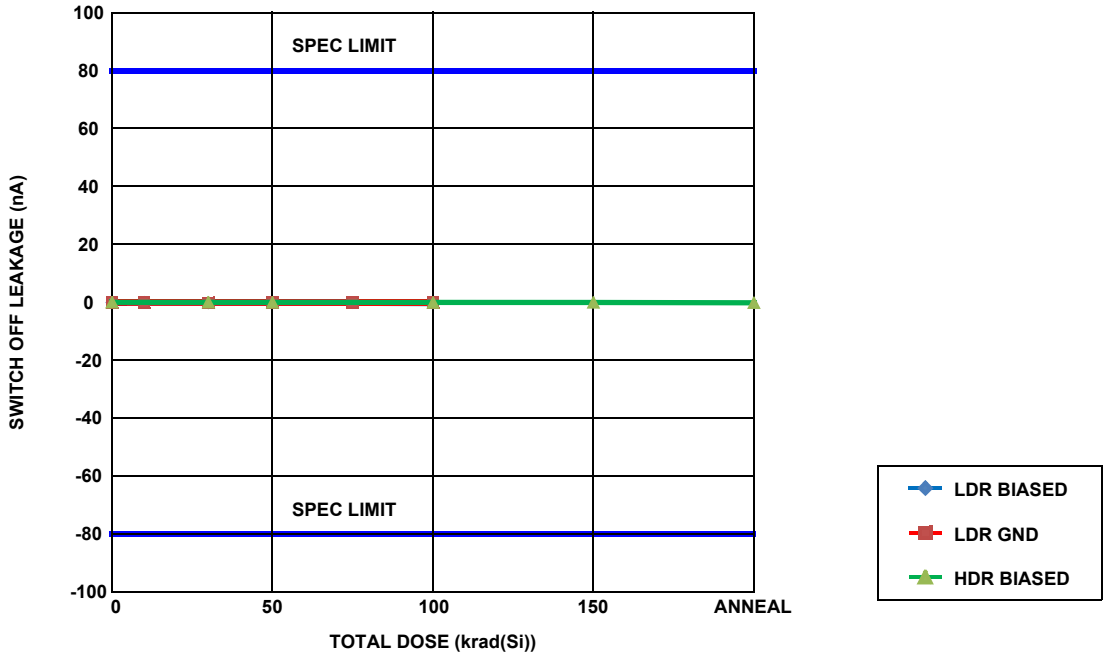


FIGURE 27. ISL7x840SEH switch OFF leakage ($I_{D(OFF)}$) into the drain with the part disabled, supply voltage ±15V, output voltage -10V, input voltage +10V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -80nA to +80nA.

Variables Data Plots (Continued)

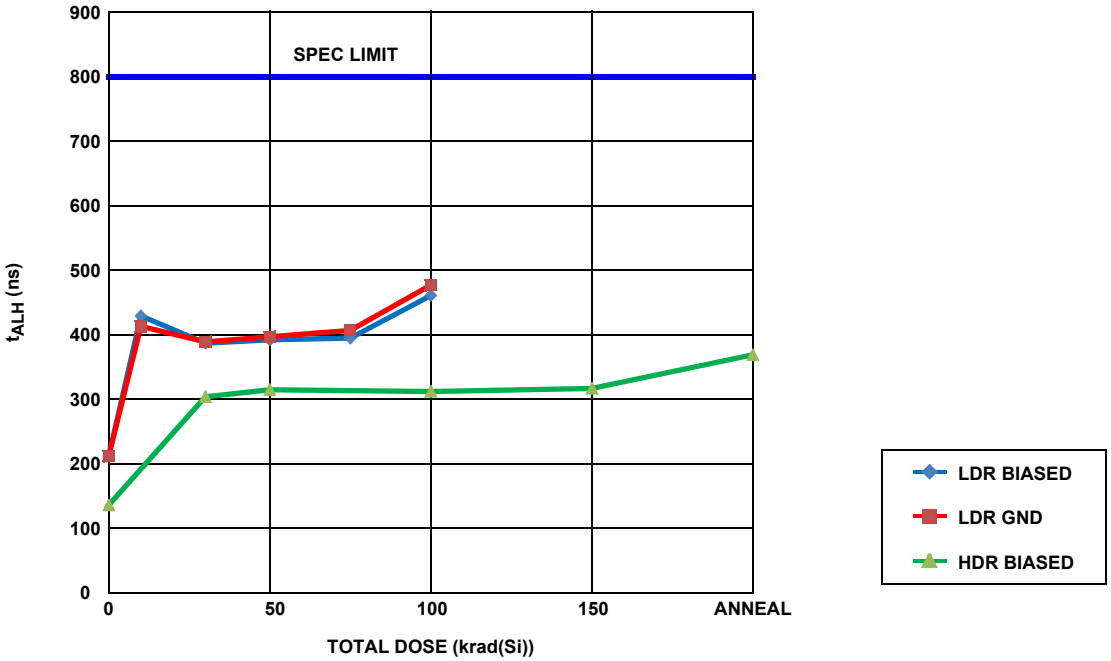


FIGURE 28. ISL7x840SEH address to output access time, LOW-to-HIGH, supply voltage ±15V, as a function of total dose irradiation at HDR for the biased case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 800ns maximum.

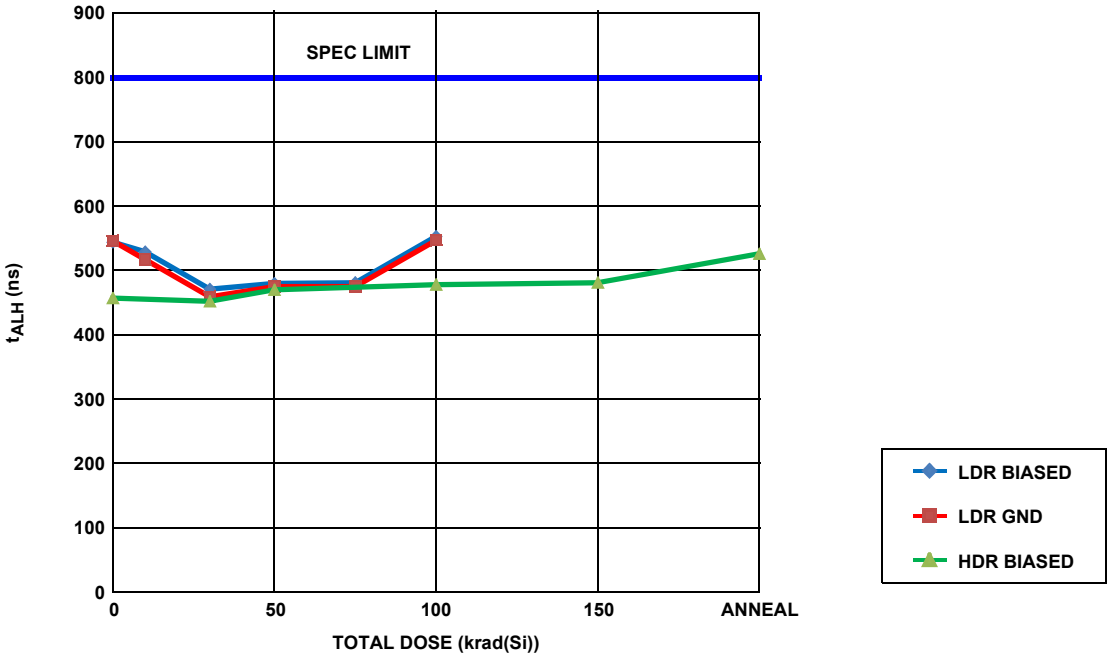


FIGURE 29. ISL7x840SEH address to output access time, HIGH-to-LOW, supply voltage ±15V, as a function of total dose irradiation at HDR for the biased case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post- irradiation SMD limit is 800ns maximum.

Variables Data Plots (Continued)

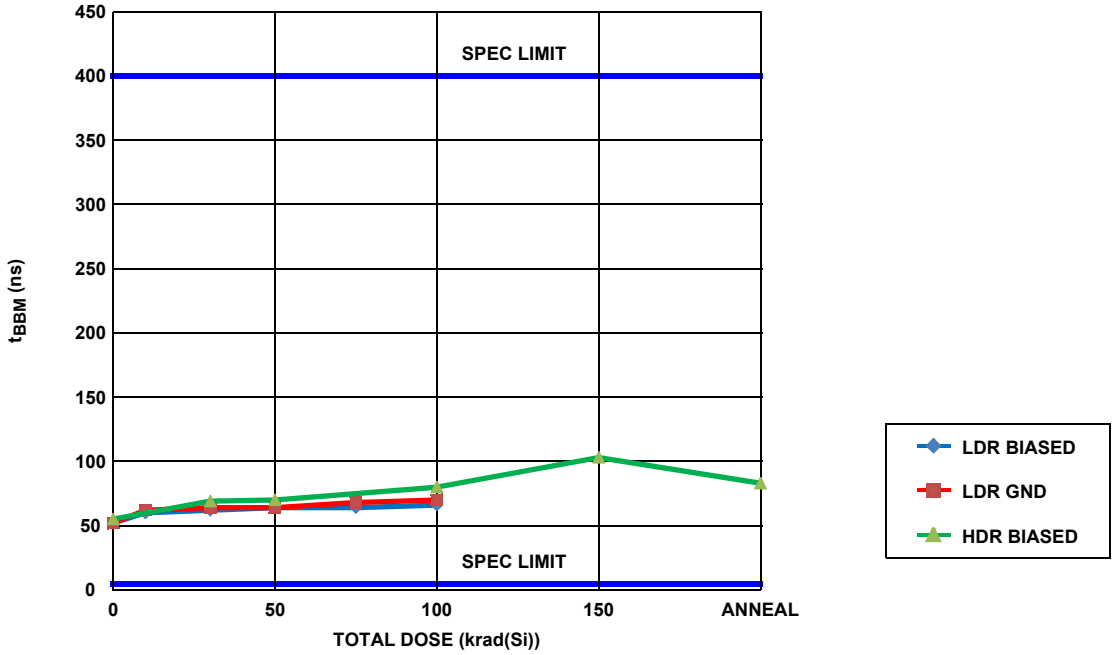


FIGURE 30. ISL7x840SEH break-before-make time delay, supply voltage ±15V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are 5ns to 400ns.

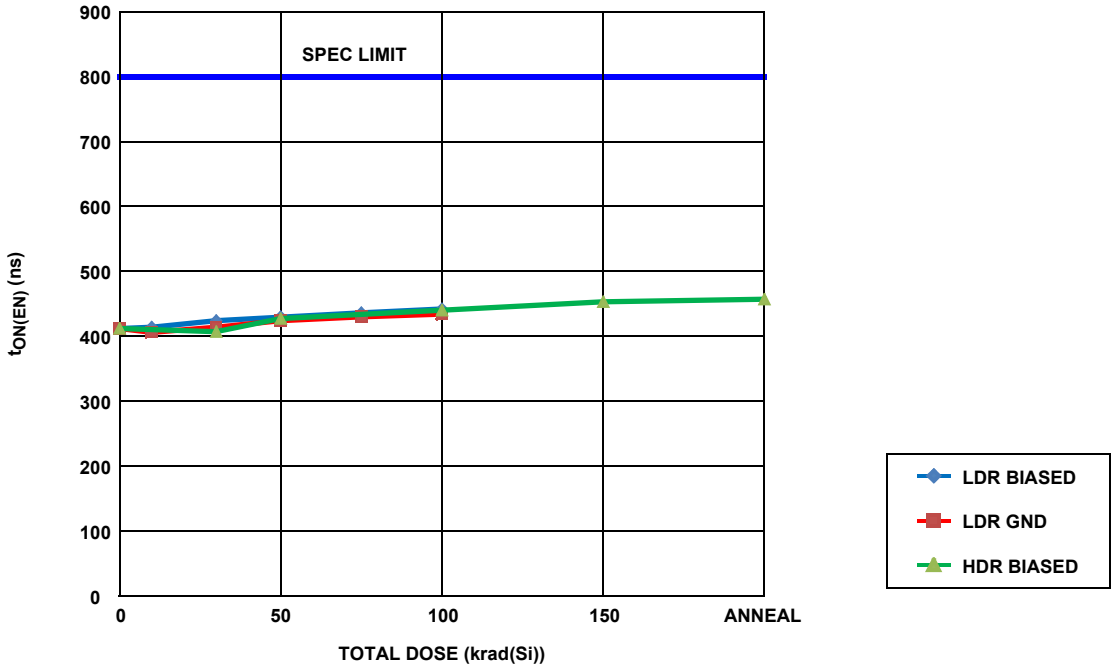


FIGURE 31. ISL7x840SEH enable to output ON delay, supply voltage ±15V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 800ns maximum

Variables Data Plots (Continued)

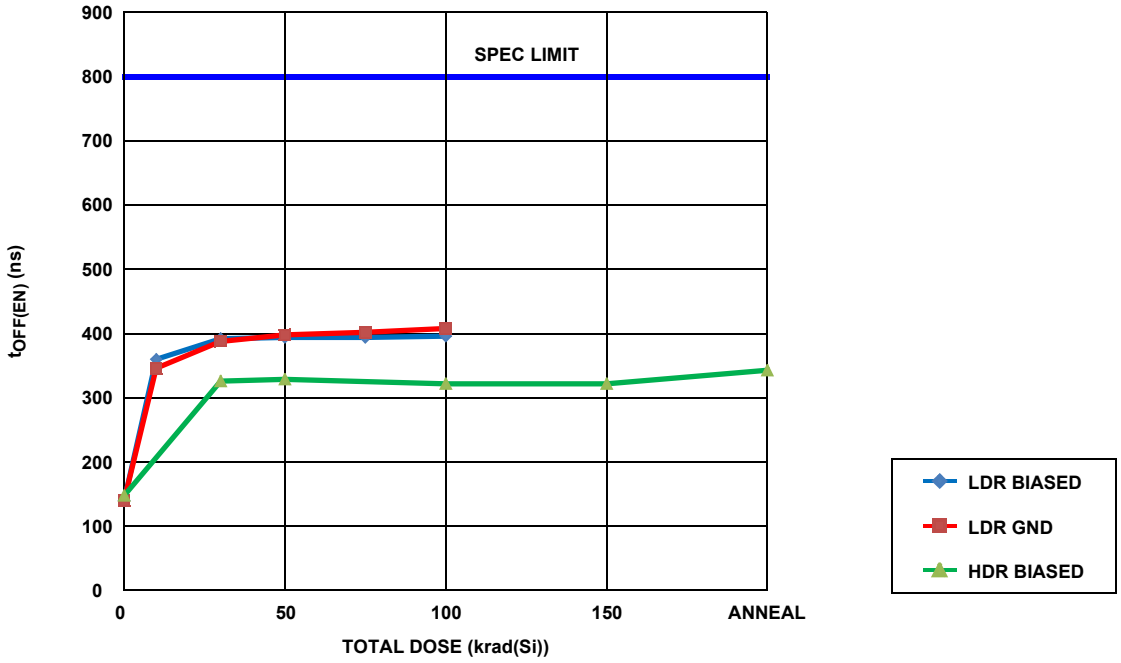


FIGURE 32. ISL7x840SEH enable to output OFF delay, supply voltage ±15V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 800ns maximum.

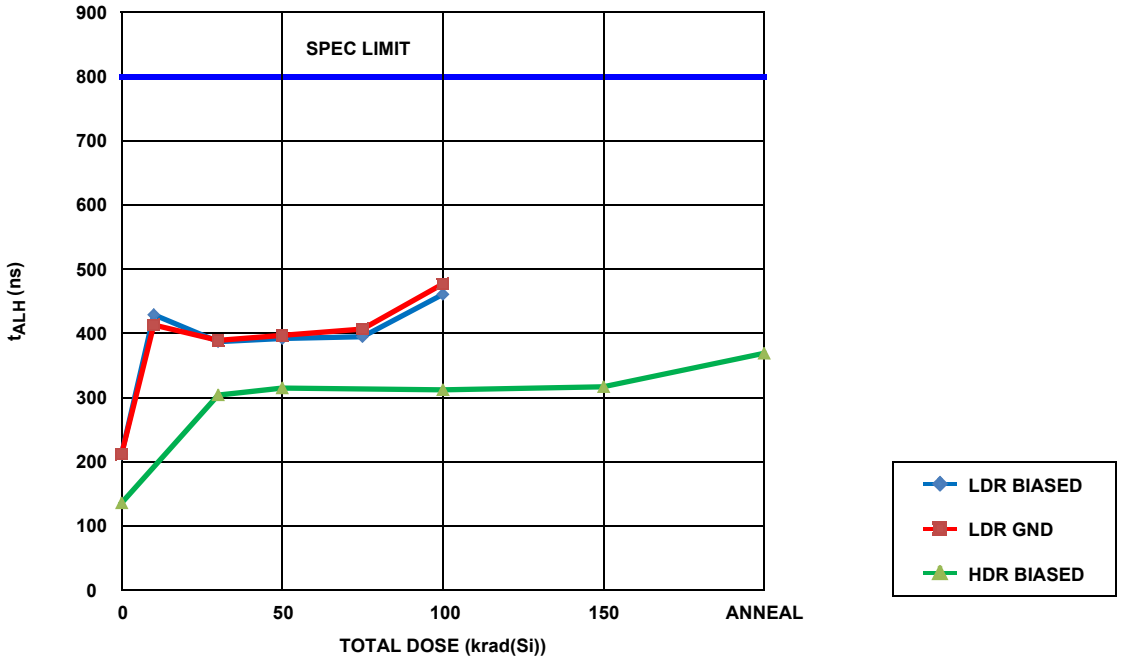


FIGURE 33. ISL7x840SEH address to output access time, LOW-to-HIGH, supply voltage ±12V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 800ns maximum.

Variables Data Plots (Continued)

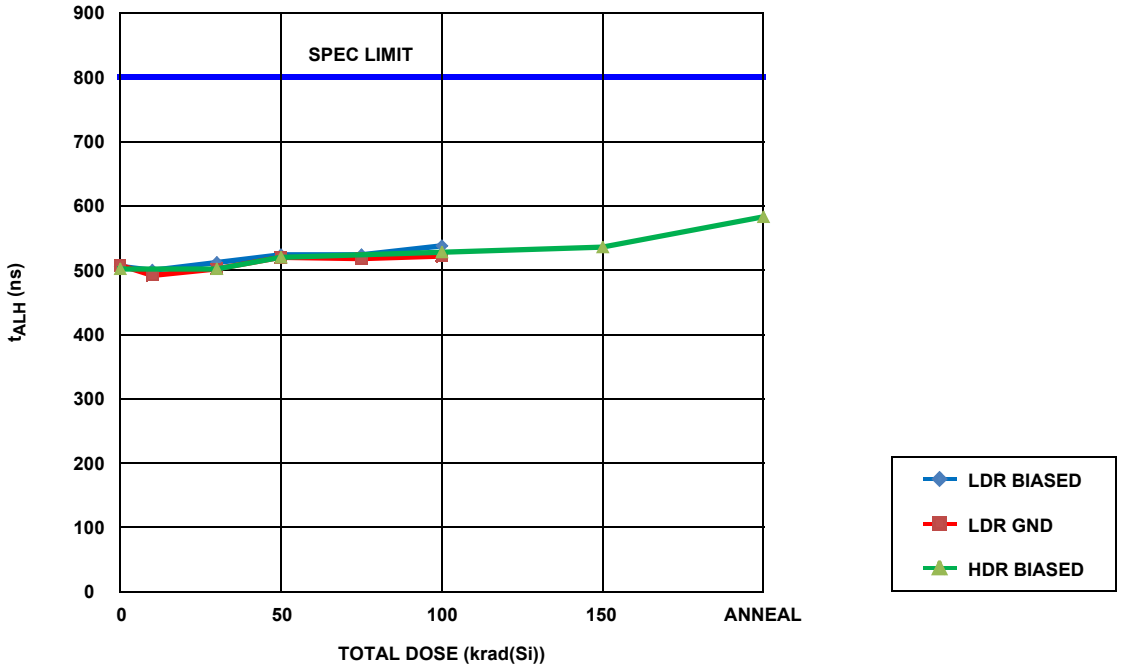


FIGURE 34. ISL7x840SEH address to output access time, HIGH-to-LOW, supply voltage ±12V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 800ns maximum.

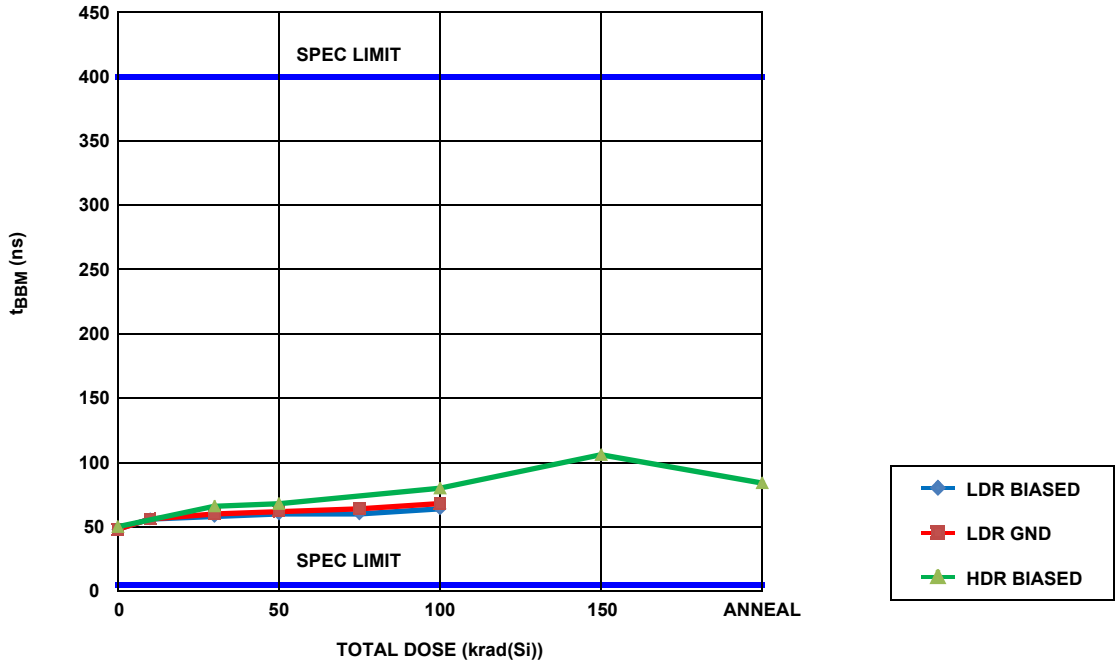


FIGURE 35. ISL7x840SEH break-before-make time delay, supply voltage ±12V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are 5ns to 400ns.

Variables Data Plots (Continued)

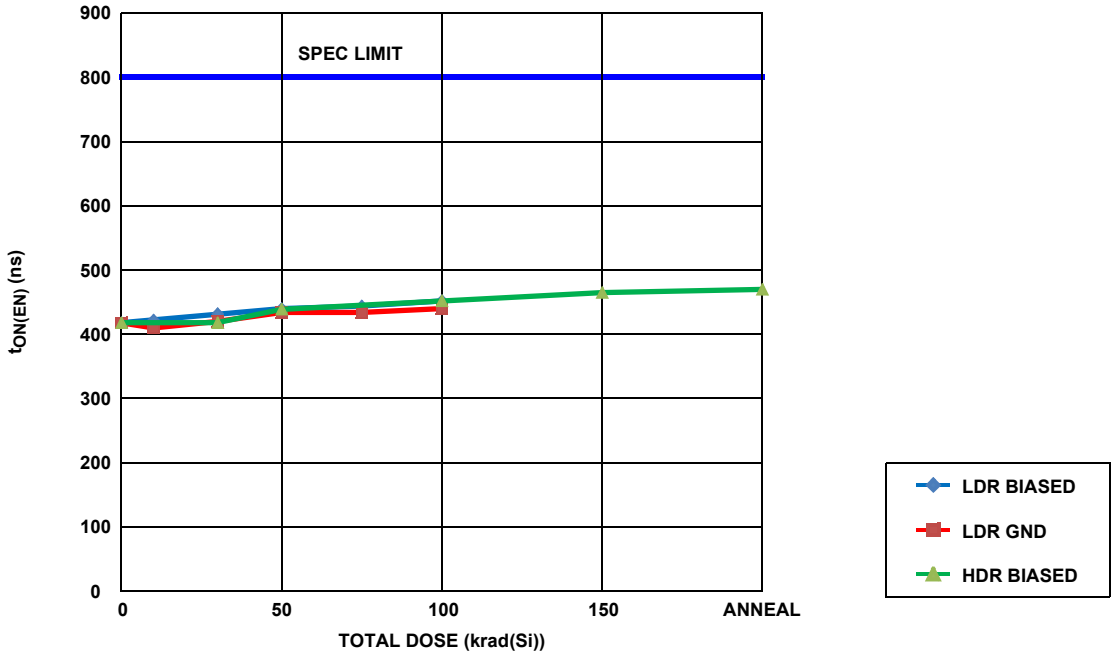


FIGURE 36. ISL7x840SEH enable to output ON delay, supply voltage ±12V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 800ns maximum.

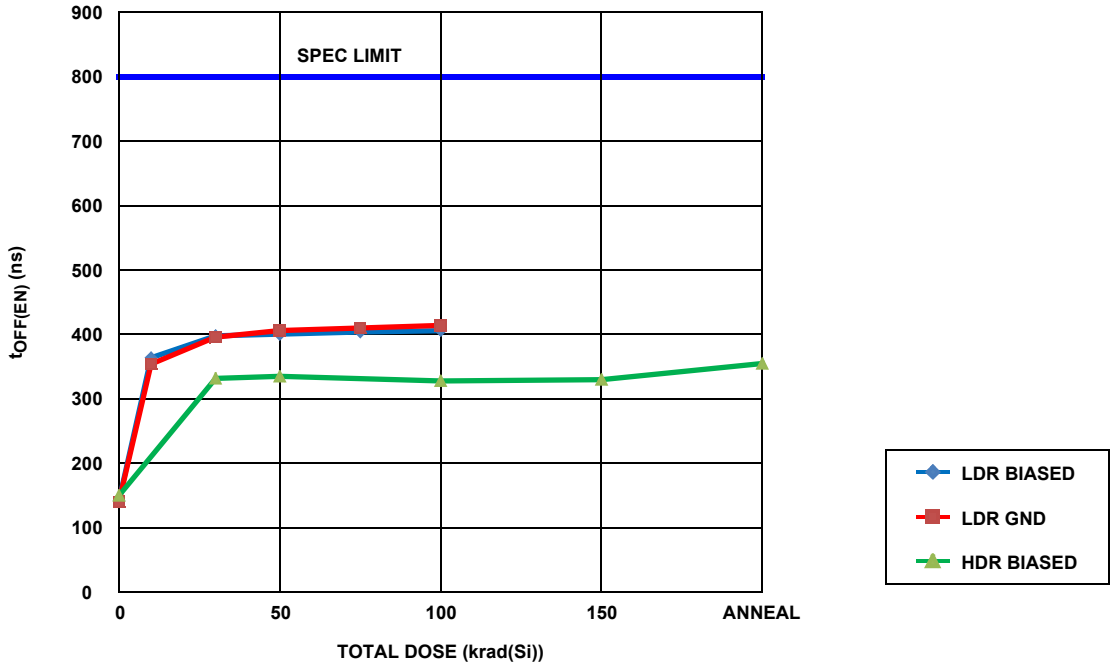


FIGURE 37. ISL7x840SEH enable to output OFF delay, supply voltage ±12V, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limit is 800ns maximum.

Variables Data Plots (Continued)

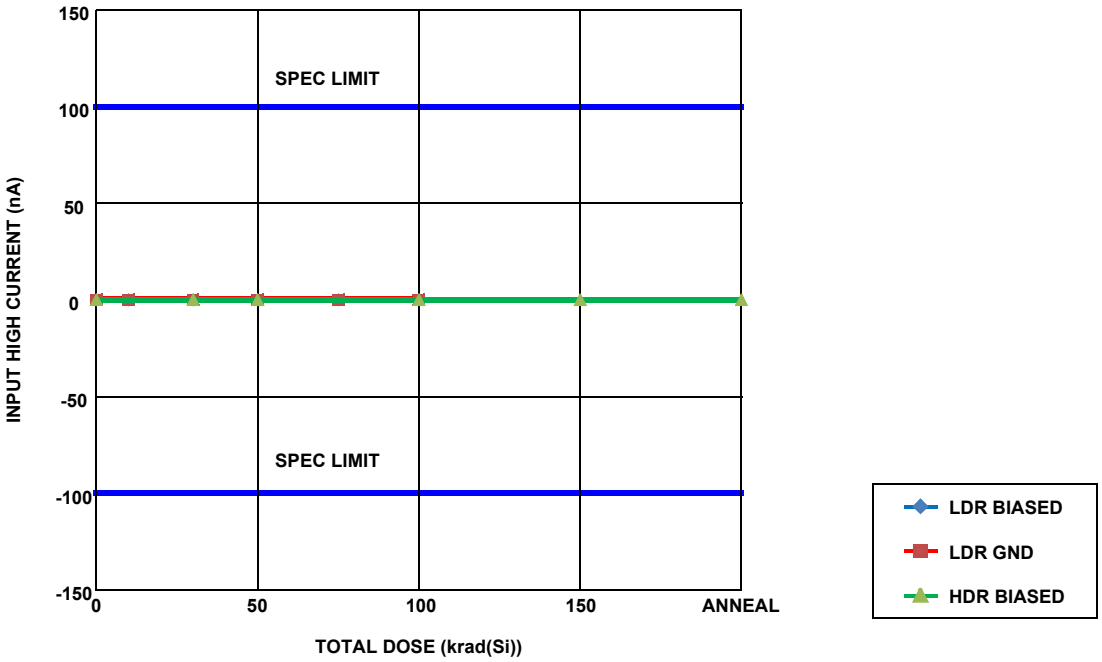


FIGURE 38. ISL7x840SEH input HIGH current, average of four addresses and ENABLE, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -100nA to 100nA.

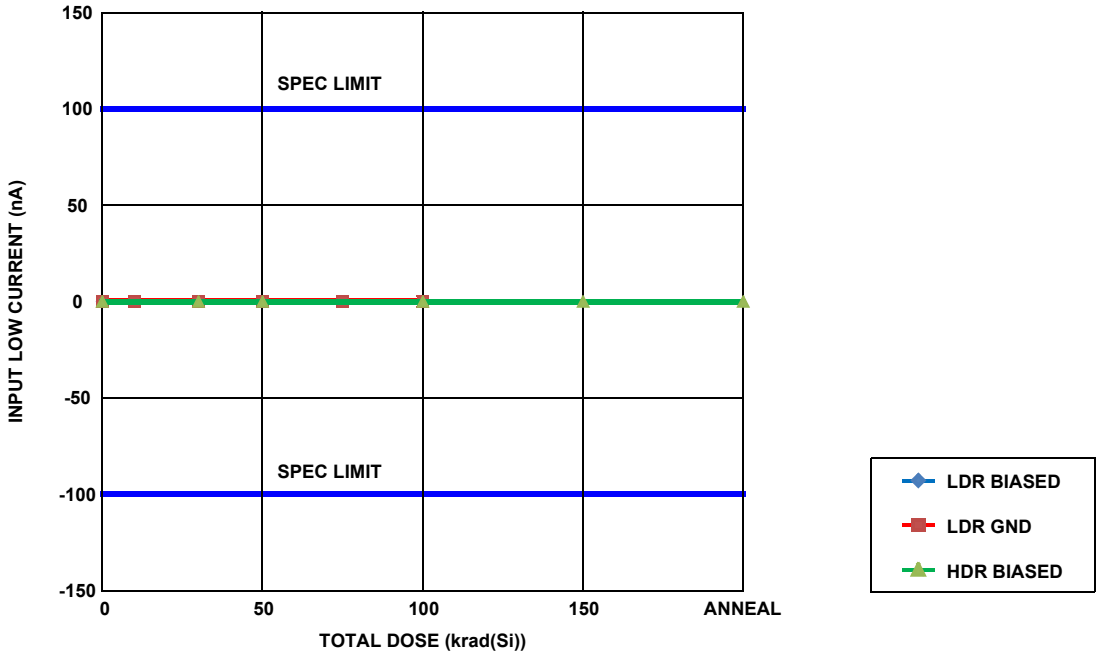


FIGURE 39. ISL7x840SEH input LOW current, average of four addresses and ENABLE, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are -100nA to 100nA.

Variables Data Plots (Continued)

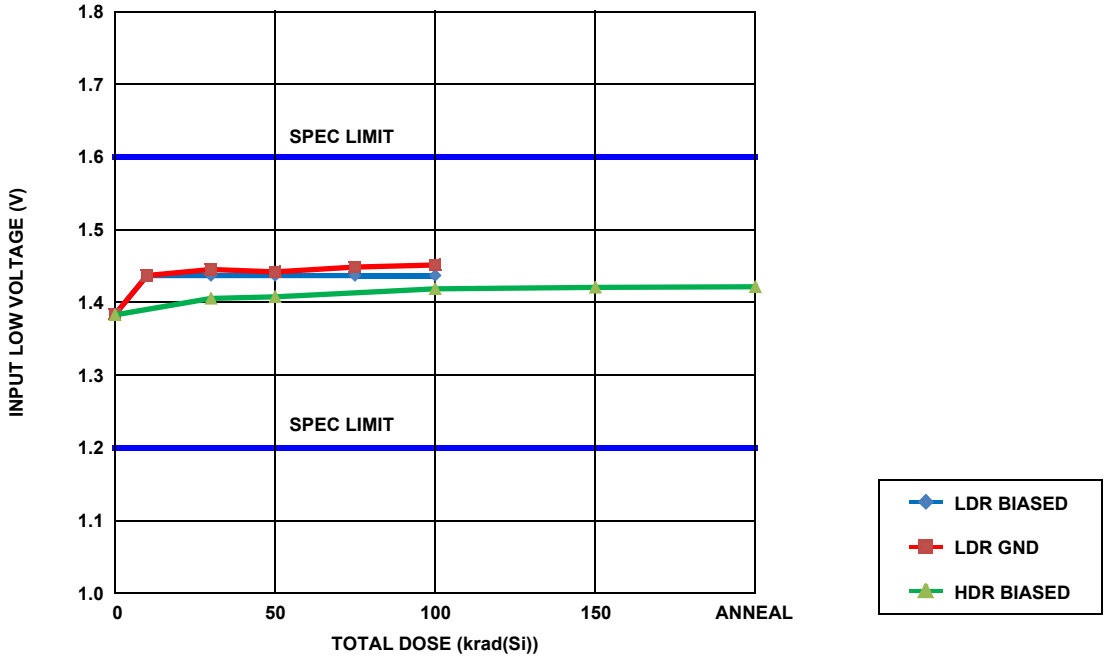


FIGURE 40. ISL7x840SEH input LOW voltage, average of four addresses and ENABLE, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are 1.2V to 1.6V.

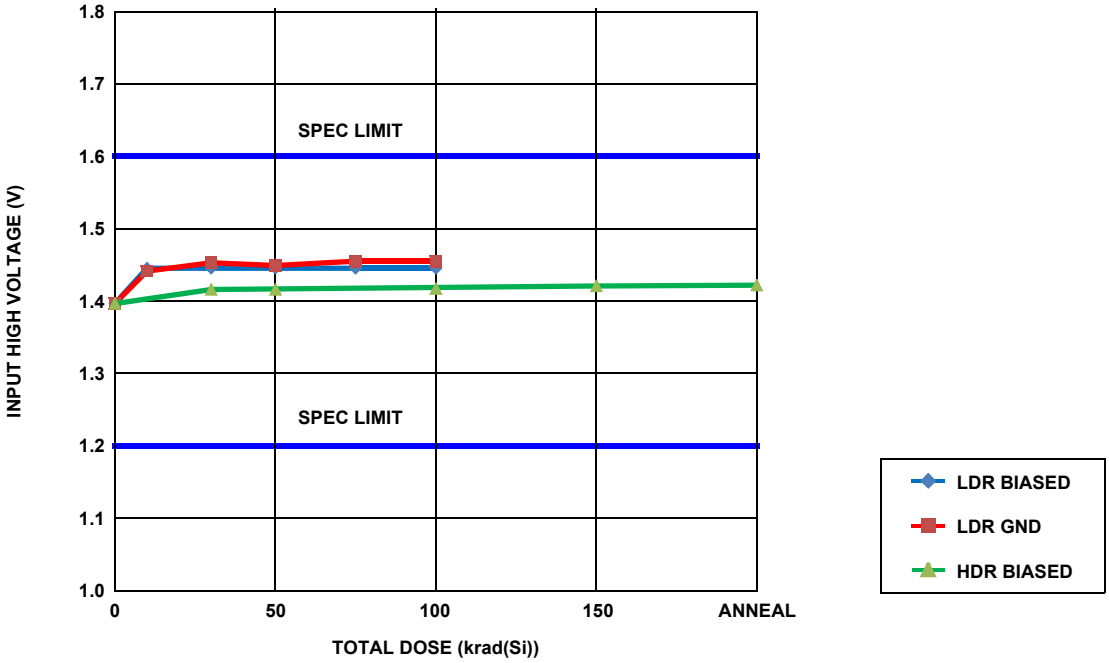


FIGURE 41. ISL7x840SEH input HIGH voltage, average of four addresses and ENABLE, as a function of total dose irradiation at HDR for the biased (per Figure 2) case and at LDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.0089rad(Si)/s and the HDR was 69.72rad(Si)/s. Sample size for each of the three cells was 4. The post-irradiation SMD limits are 1.2V to 1.6V.

Conclusion

This document reports the results of a total dose test of the ISL7x840SEH 16-channel analog multiplexer. Parts were tested at LDR under biased and unbiased conditions and at HDR under biased conditions as outlined in MIL-STD-883 Test Method 1019.7. The HDR samples were taken through 150krad(Si) and biased anneal; the LDR samples were taken through 100krad(Si).

ATE characterization testing at downpoints showed no rejects to the SMD Group A limits for biased irradiation at HDR and biased and grounded irradiation at LDR, with the HDR irradiations followed by a 100 hours biased anneal for 168 hours.

The attributes data is presented in Table 1, while the variables data for selected parameters is presented in Figures 3 through 41.

As a determinant of LDR sensitivity, MIL-STD-883 Test Method 1019.7 specifies that a delta_parameter calculation be performed for any parameters that exceed the Group A limits. These calculations were not required as there were no rejects against the Group A limits. Accordingly, the part is considered ELDRS insensitive up to 150krad(Si).

Similarly, no differences between biased and unbiased irradiation were noted, and the part is not considered bias sensitive.

TABLE 2. REPORTED PARAMETERS

FIGURE	PARAMETER	LIMIT LOW	LIMIT HIGH	UNIT	NOTES
3	Positive Supply Current	-	350	µA	
4	Negative Supply Current	-350	-	µA	
5	Positive Standby Supply Current	-	350	µA	
6	Negative Standby Supply Current	-350	-	µA	
7	Supply Current Into VREF	-	35	µA	
8	Switch ON-resistance, Average	-	500	Ω	V_{IN} = 5V
9	Switch ON-resistance, Average	-	500	Ω	V_{IN} = -5V
10	Switch ON-resistance, Average	-	700	Ω	V_{IN}= 15V
11	Switch ON-resistance, Average	-	700	Ω	V_{IN} = -15V
12	ON-resistance match, Average	-	20	Ω	V_{IN} = 5V
13	ON-resistance Match, Average	-	20	Ω	V_{IN} = -5V
14	OFF Source Leakage, Average	-100	100	nA	V_{IN} = 11.5V
15	OFF Source Leakage, Average	-100	100	nA	V_{IN} = -11.5V
16	OFF Source Leakage, Average	-750	750	nA	35V overvoltage
17	OFF Source Leakage, Average	-750	750	nA	-35V overvoltage
18	OFF Drain Leakage, Average	-500	500	nA	Power off, 35V overvoltage
19	OFF Drain Leakage, Average	-500	500	nA	Power off, -35V overvoltage
20	ON Source Leakage, Average	-500	500	nA	35V overvoltage
21	ON Source Leakage, Average	-500	500	nA	-35V overvoltage
22	OFF Source Leakage, Average	-100	100	nA	Power off
23	OFF Source Leakage, Average	-100	100	nA	Power off
24	ON Drain Leakage, Average	-100	100	nA	Source and drain at 10V
25	ON Drain Leakage, Average	-100	100	nA	Source and drain at -10V
26	ON Source Leakage	-80	80	nA	Part disabled
27	ON Source Leakage	-80	80	nA	Part disabled
28	Access Time, LOW-to-HIGH	-	800	ns	±15V supplies
29	Access Time, HIGH-to-LOW	-	800	ns	±15V supplies
30	Break-before-make Time	5	400	ns	±15V supplies

TABLE 2. REPORTED PARAMETERS (Continued)

FIGURE	PARAMETER	LIMIT LOW	LIMIT HIGH	UNIT	NOTES
31	Enable ON to Output Delay	-	800	ns	±15V supplies
32	Enable OFF to Output Delay	-	800	ns	±15V supplies
33	Access time, LOW-to-HIGH	-	800	ns	±12V supplies
34	Access time, HIGH-to-LOW	-	800	ns	±12V supplies
35	Break-before-make Time	5	400	ns	±12V supplies
36	Enable ON to Output Delay	-	800	ns	±12V supplies
37	Enable OFF to Output Delay	-	800	ns	±12V supplies
38	Input HIGH Current, Average	-100	100	nA	A0–A3 and ENABLE
39	Input LOW Current, Average	-100	100	nA	A0–A3 and ENABLE
40	Input LOW Voltage, Average	1.2	1.6	V	A0–A3 and ENABLE
41	Input HIGH Voltage, Average	1.2	1.6	V	A0–A3 and ENABLE

NOTE:

3. Limits are taken from Standard Microcircuit Drawing (SMD) 5962-15219.

Revision History

REVISION	DATE	DESCRIPTION
1.0	Jul 2, 2021	Added the ISL73840SEH information throughout the document. Changed the ISL71840SEH references to ISL7x840SEH references to cover both parts, where applicable. Added Revision History section.
0.0	Jun 30, 2015	Initial release.

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