RX23T

Immunity test - EFT

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TABLE OF CONTENTS

1 GENERAL

1.1 Scope

The LANGER immunity test procedure against Electrical Fast Transients (EFT) has been performed on RX23T in LQFP64 package.

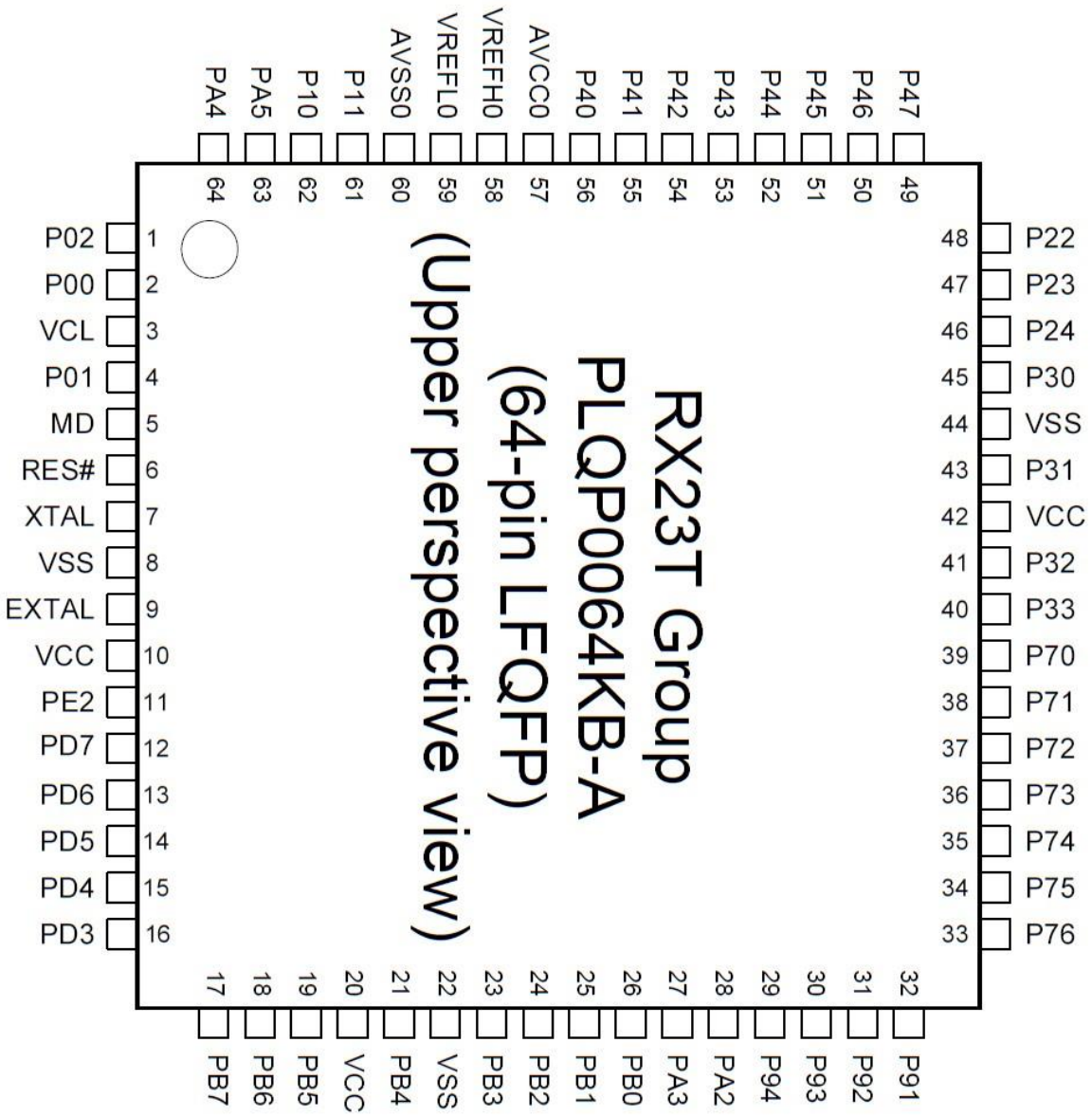
1.2 Device under test (DUT):

DUT:	RX23T R5F523T5ADFM
Manufacturer:	RENESAS Electronics Corporation
Package:	LQFP64; Body 10 x 10 x 1.7 mm
Package marking:	RX23T5 R523T5ADFM 5410ZA0
Supply voltage level:	3.3 V
Current consumption:	
- with external oscillator:	13 mA
Heartbeat LED on port:	PA3; Pin 27
Failure LED on port:	P72; Pin 37
Tristate LED on port:	P22; Pin 48
Switch on port:	PD6; Pin 13
Switch_state on port:	P71; Pin 38
Input_OSC on port:	P0_15; Pin 50
Heartbeat LED frequency:	0.56 Hz (external oscillator)
Temperature:	23 °C
Humidity:	45 %

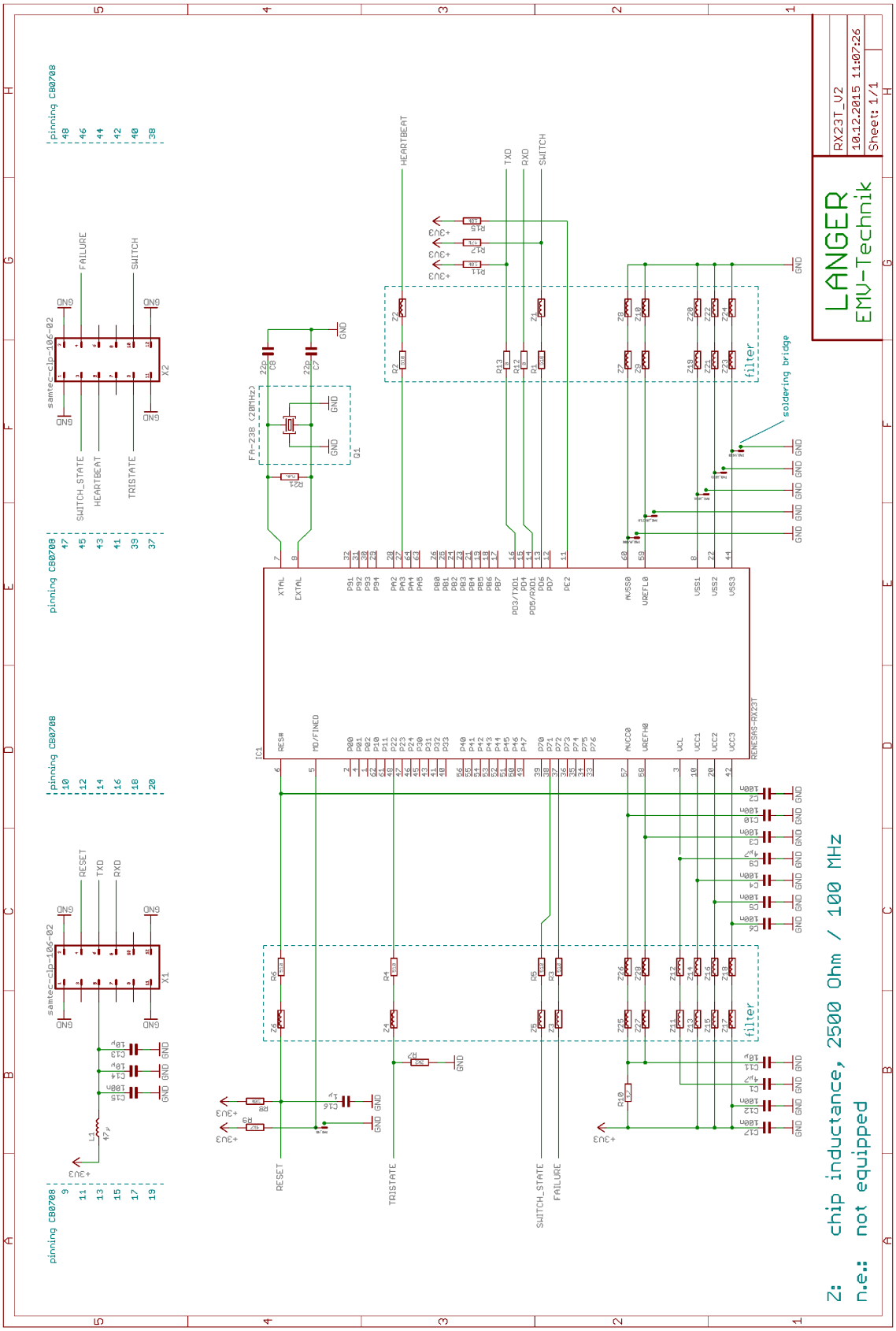
2 HARDWARE AND SOFTWARE SETTINGS

2.1 Pinout

LQFP64 package - pinout:



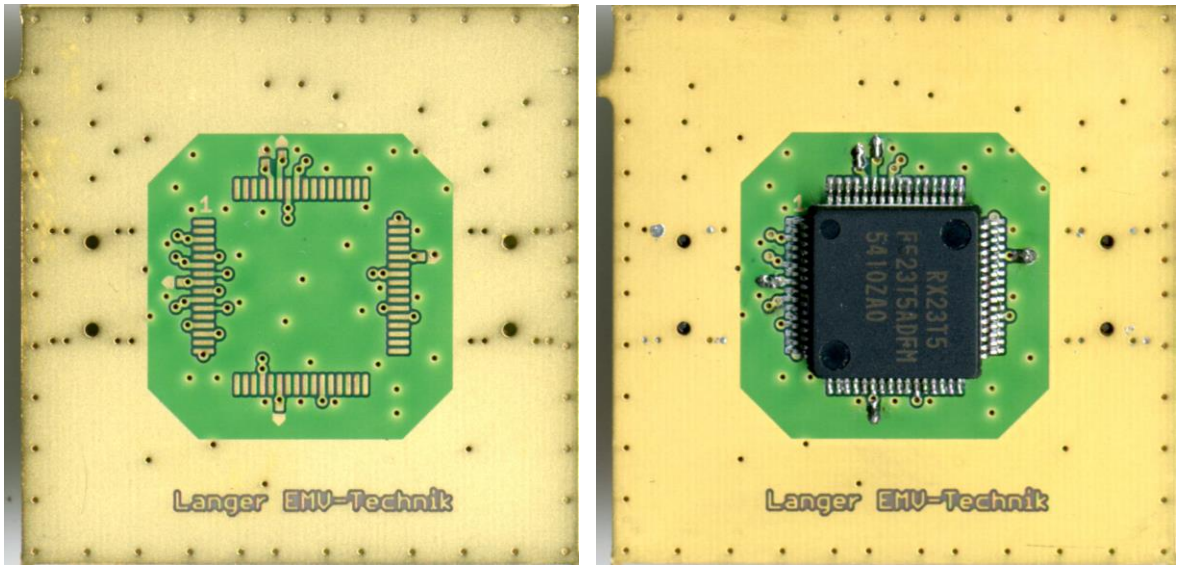
2.2 Test board schematic



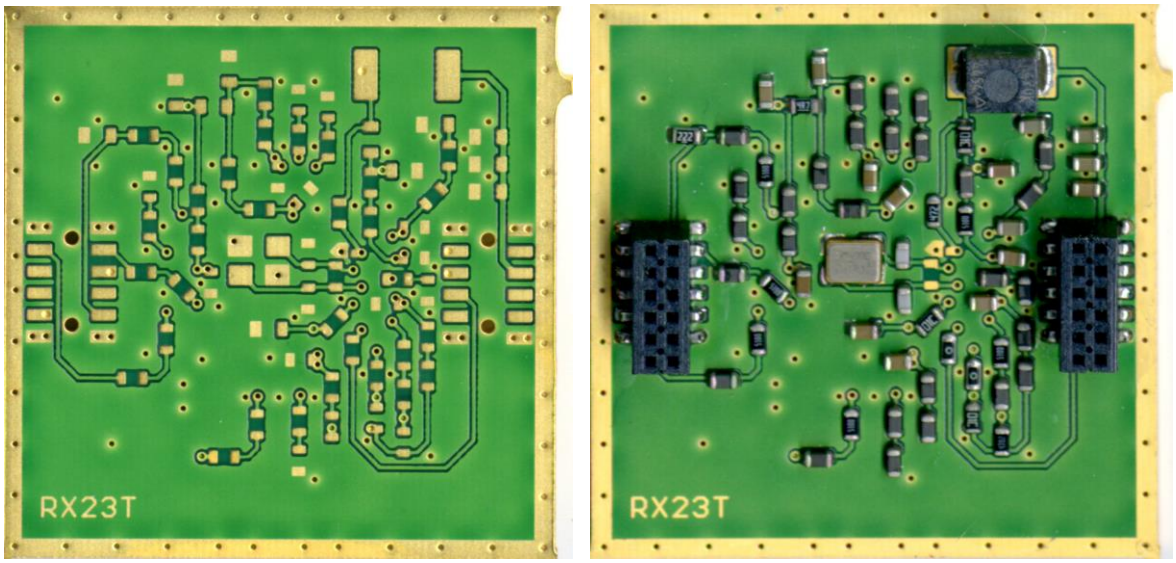
2.3 Test board

4 layers, 32 mm x 32 mm x 1.0 mm dimensions

Test board top:



Test board bottom:



3 TEST CONDITIONS

3.1 Test equipment

Table 1: Test equipment

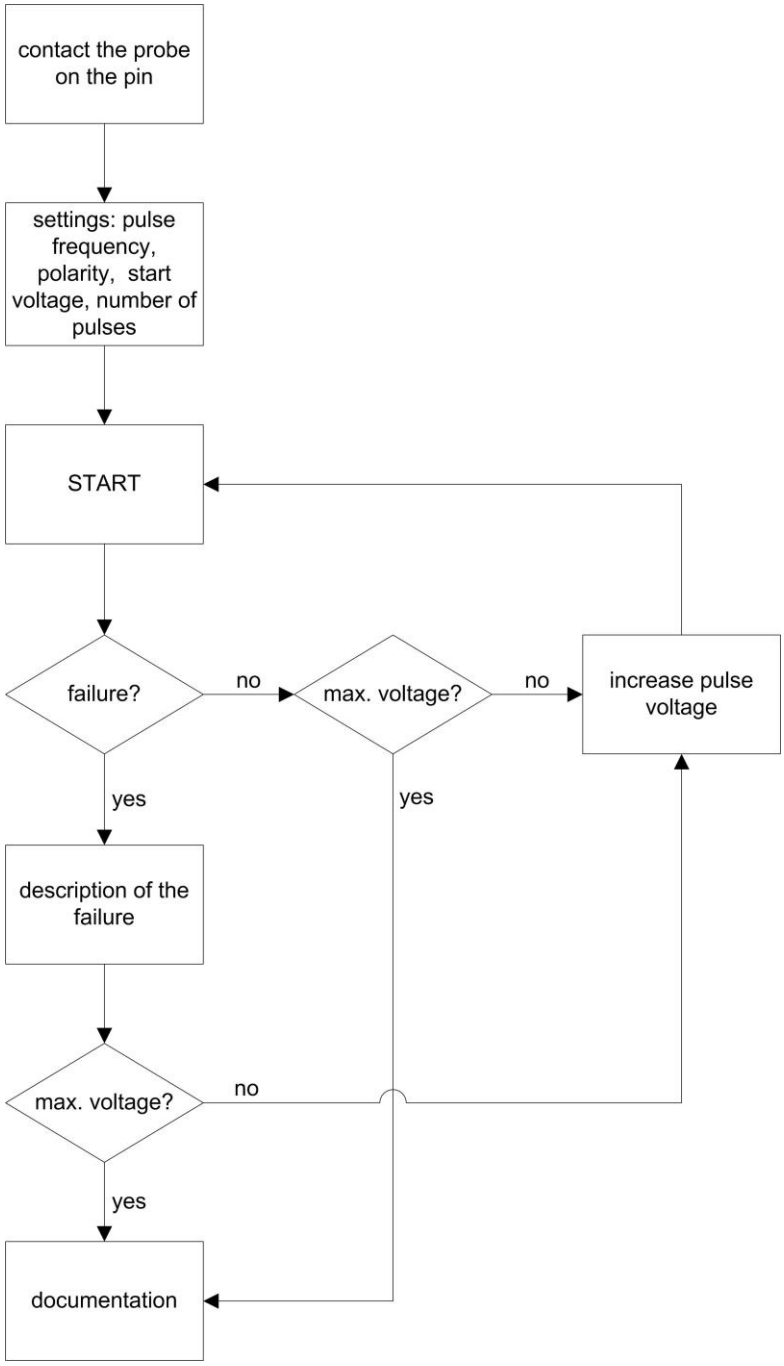
Instrument	Vendor	Model	Comment
Power supply	STATRON	Type 2229	2 x 0-40 V / 0-2.5 A
Oscilloscope	Tektronix	MSO4104	4 Channel colour digital Oscilloscope
IC-Test system	Langer	Set P200/300	EFT injection set for IC
Connection Board	Langer	CB0708	
Oscilloscope Adapter	Langer	OA4005	4 Channels
Ground Plane	Langer	GND 25 GNDA-02	

3.2 Measurement Settings

Table 2: Definitions

Test pulse:	P211/P201 → 1.5 / 5 ns P311/P301 → 1.5 / 20 ns
Increment of voltage rise:	P211/P201 → approx. 1 V P311/P301 → approx. 10 V
Max. generator voltage:	P201 → 40 V P301 → 510 V
Pulse frequency:	10 kHz
Polarity:	Positive and negative pulses
Pulse duration:	6.55 s → 65500 pulses
Current input of IC:	Manufacturer-dependent Fault if value stays below or is exceeded by 50%
Oscillator:	Internal oscillator
Fault detectors:	See section 4.2
Display of state "Failure LED":	Software-dependent

Flowchart test procedure:



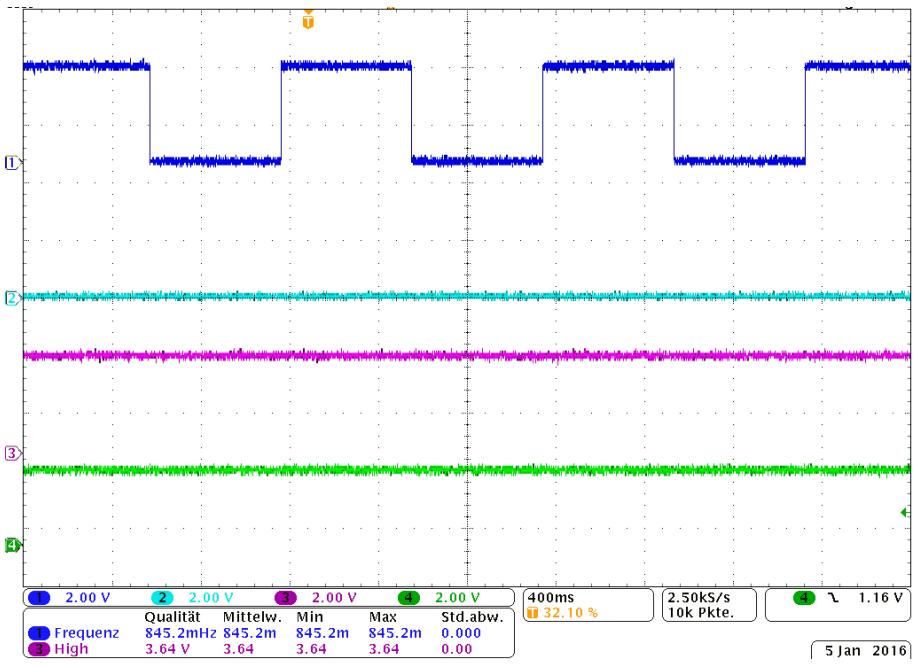
4 RESULTS

4.1 Normal operation mode

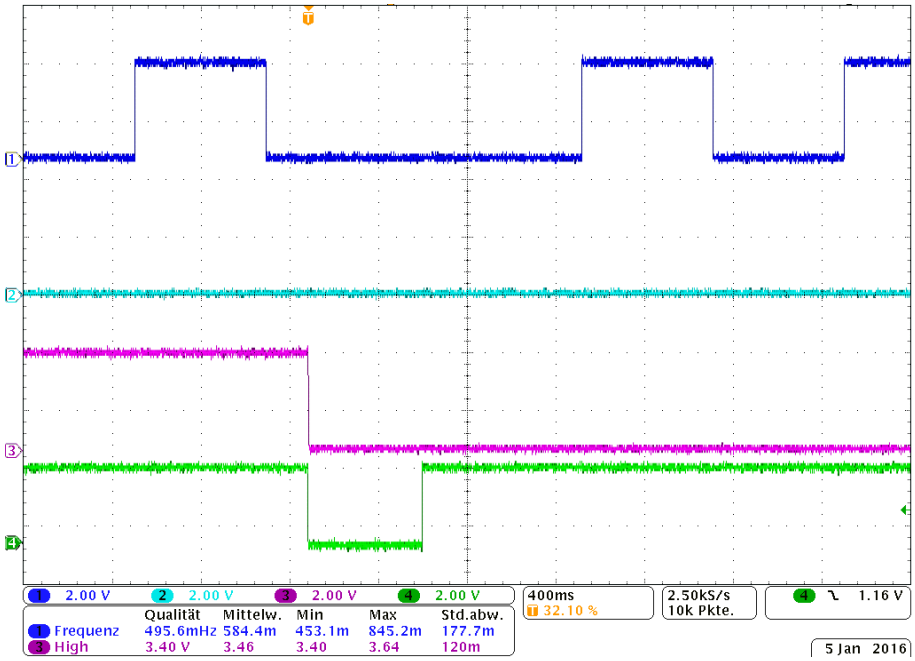
Legend:

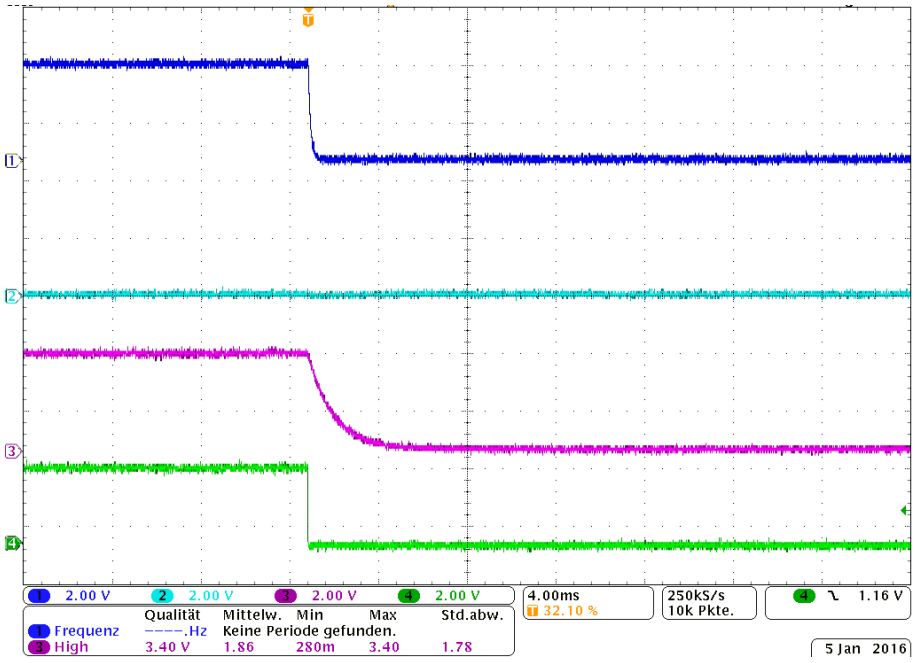
Oscilloscope Channel:	Color:	Signal name:
1	Blue	HEARTBEAT
2	Cyan	FAILURE
3	Red	SWITCH_STATE
4	Green	TRISTATE

Normal operation mode (external osc):

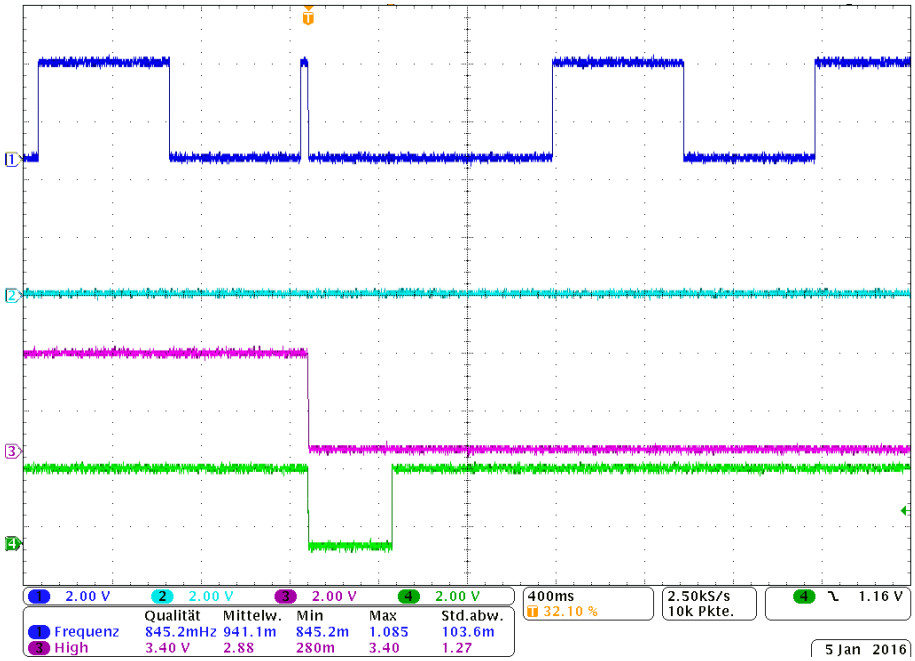


External manual Reset:





Power on Reset (POR):



4.2 Fault description

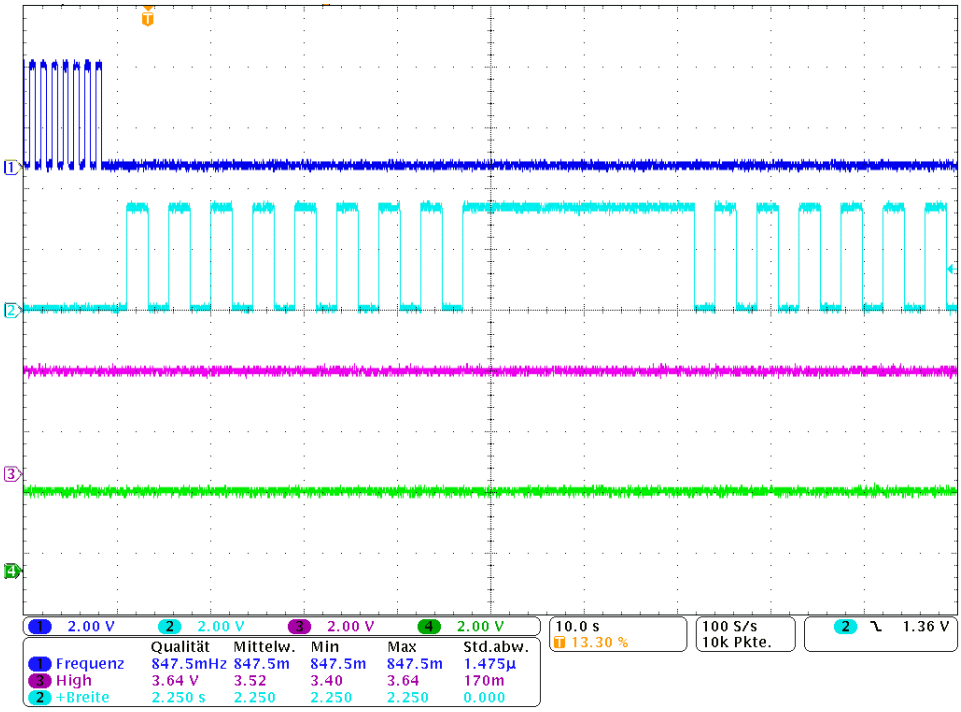
Fault classification:

F1.X function failure, self-recoverable without reset
F2.X function failure, self-recoverable with reset
F3.X function failure, requires a manual reset
F4.X function failure, requires a power off/on
F5.X permanent damage

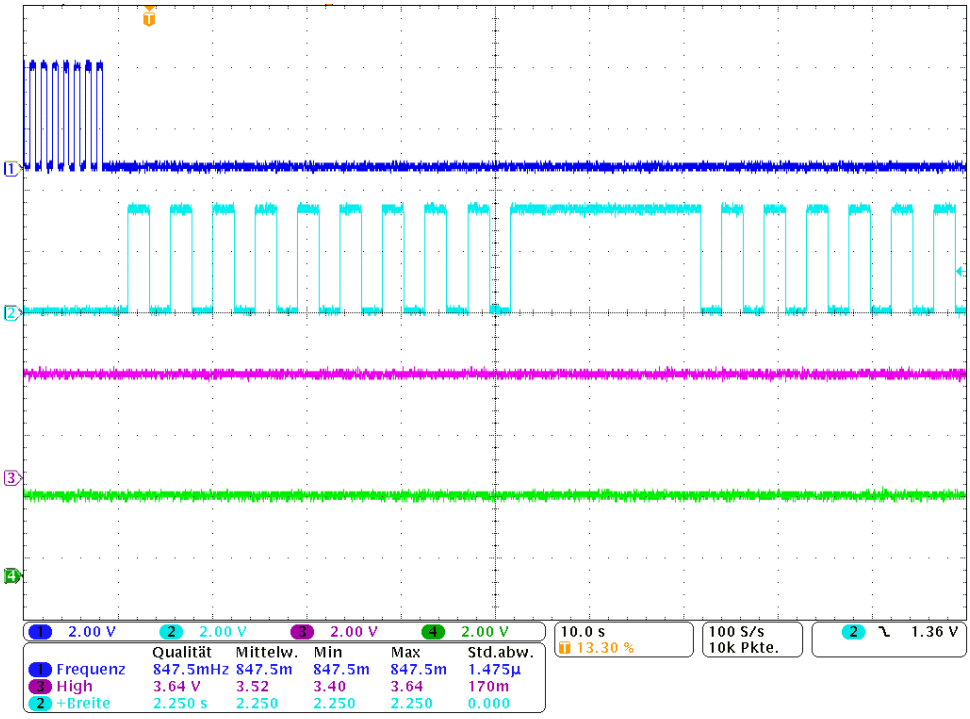
Fault reporting of special software:

Defined by RENESAS:

ERROR	**Blinking sequence of failure LED**
timer ra	1
cpu register test	2
stack test	3
flags test	4
intreg	5
unexpected HW int	6
unexpected Peri int	7
WDT	8
RAM	9
CRC	10
SWreset	11

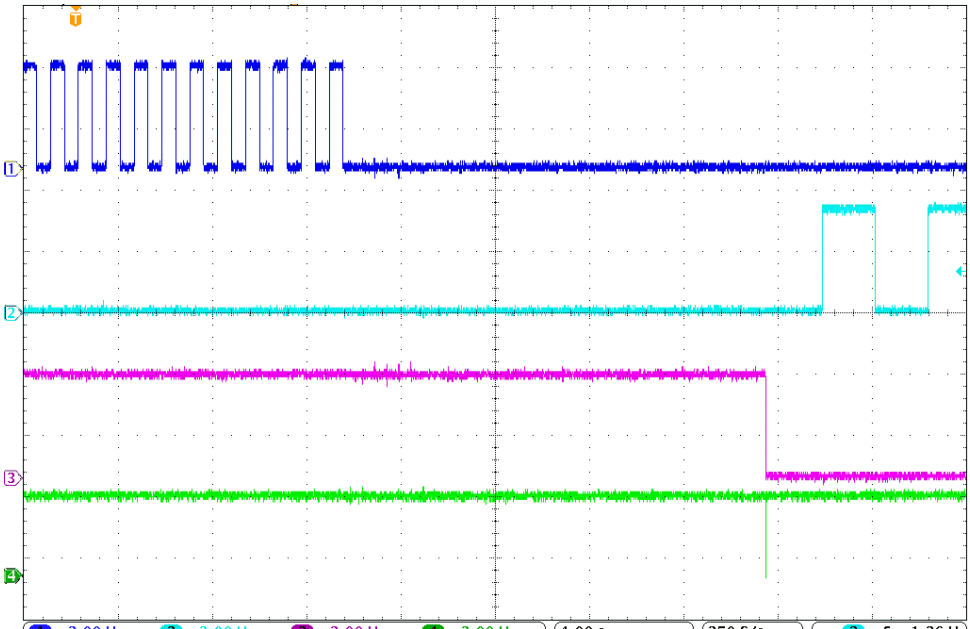
Fault list:		
	Current consumption	
F1.1	13 mA	**WDT error**  Disturbance on → Heartbeat stop; WDT error Disturbance off → Failure is flashing Manual Reset → Normal function POR → Normal function

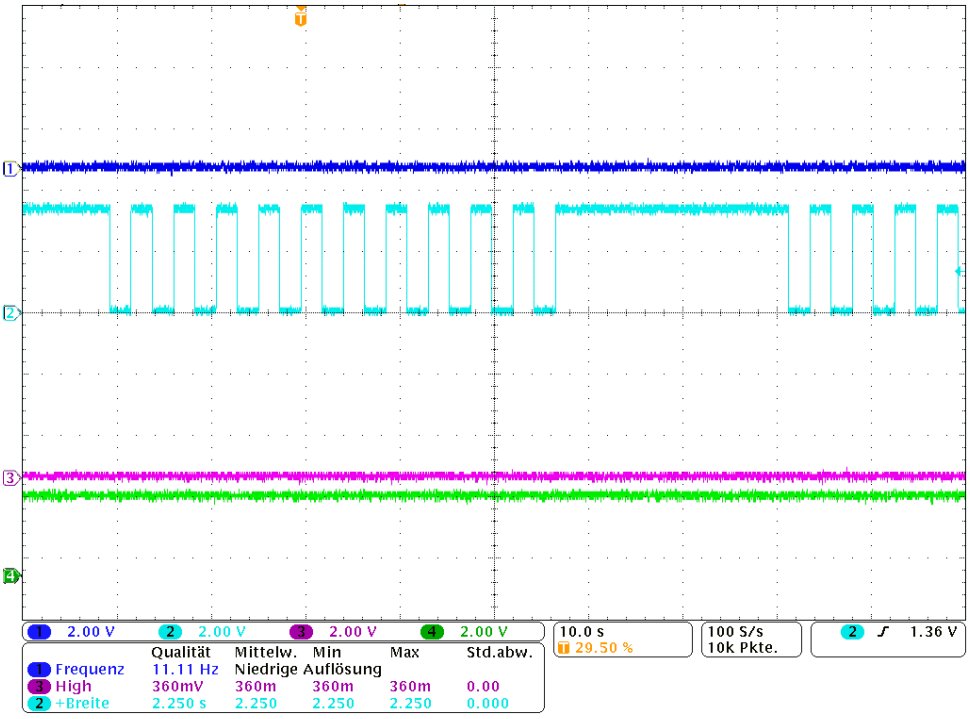
F1.2	13 mA	**RAM error**



Disturbance on → Heartbeat stop; RAM error
Disturbance off → Failure is flashing
Manual Reset → Normal function
POR → Normal function

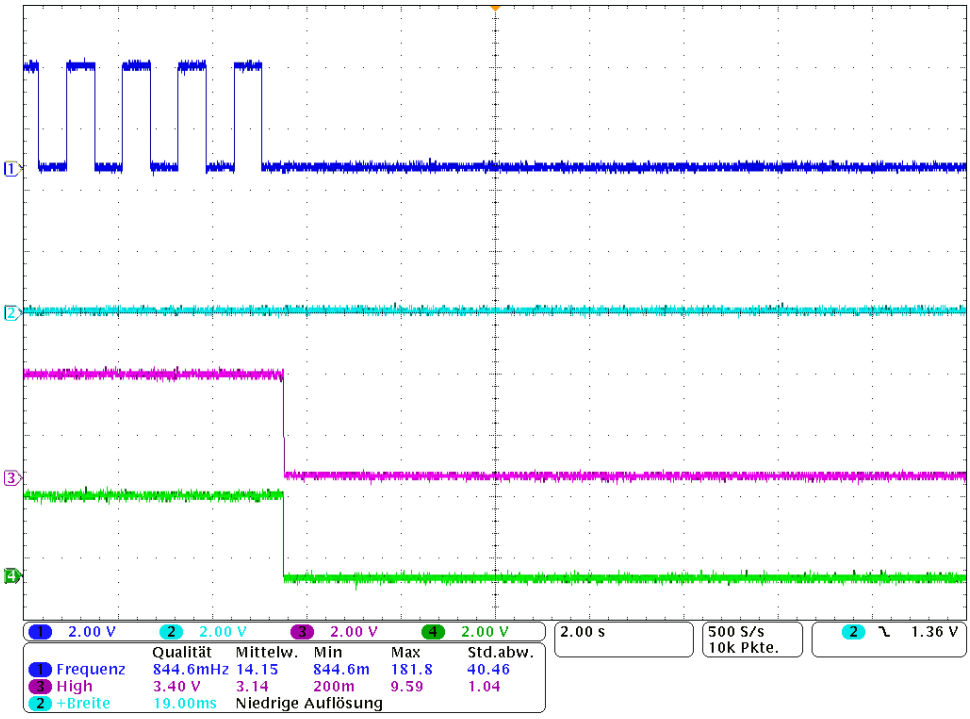
F2.1	16 mA	**CRC error**





Disturbance on	→	Heartbeat stay in last state, no function
Disturbance off	→	After several secons --> reset + CRC error
Manual Reset	→	Normal function
POR	→	Normal function

F3.1	0.5 mA	**Function stop**



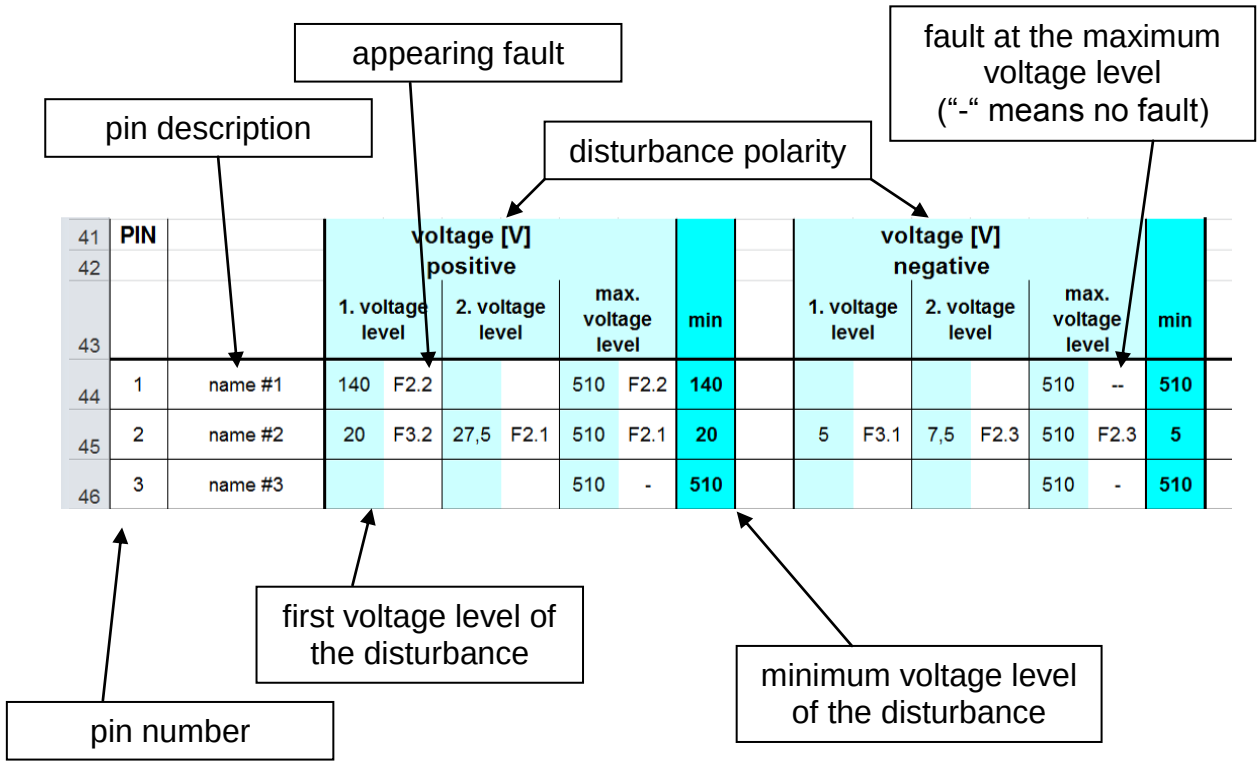
Disturbance on → No function, all Pins low
Disturbance off → No function, all Pins low
Manual Reset → Normal function
POR → Normal function

4.3 Test result diagrams

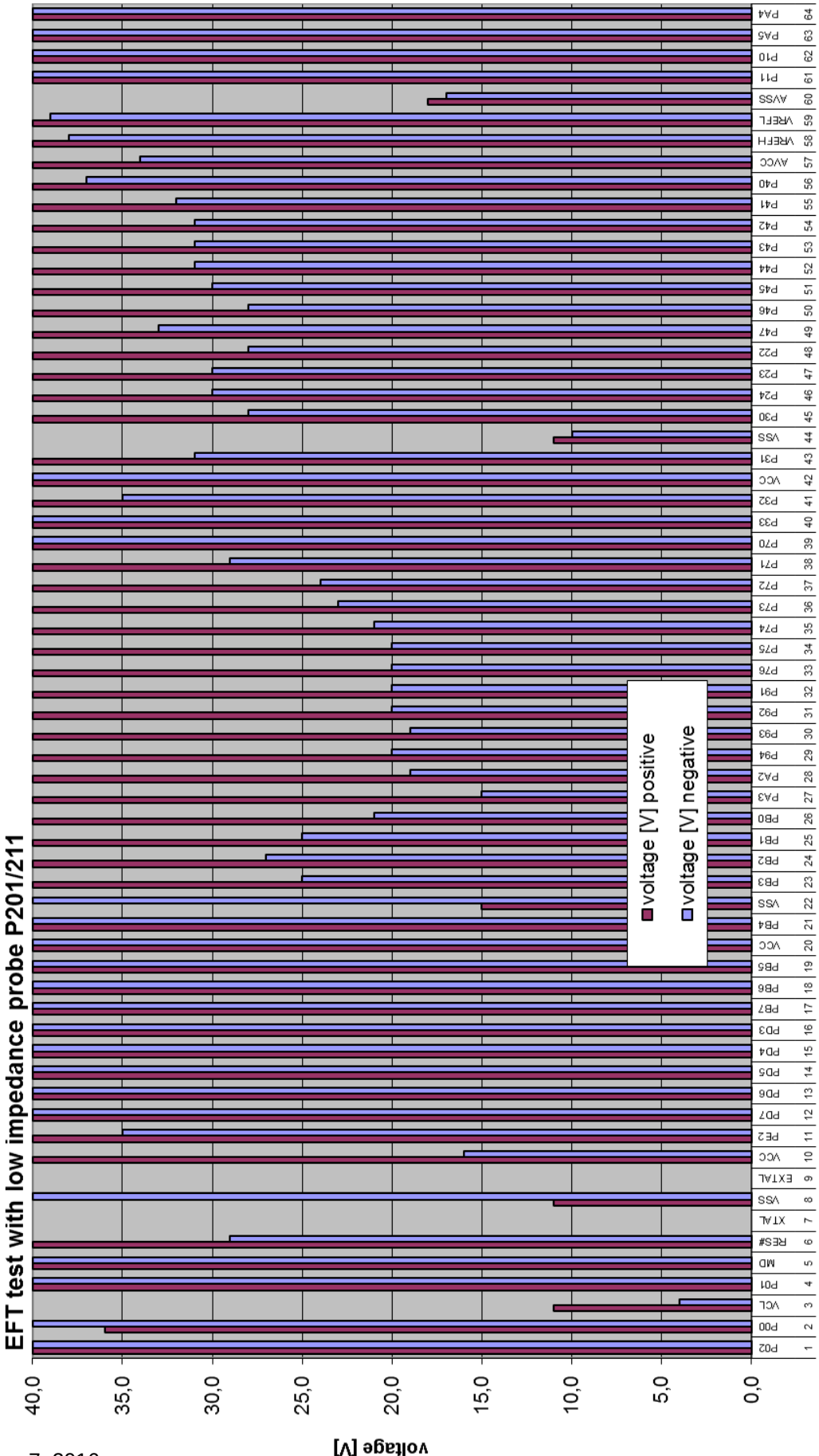
The detailed test results are located in the attached Excel file
“2015.01.07 RX23T - EFT test results.xls”.

All of the tests in the following diagrams are done with the internal oscillator.

Comment:
(The illustrated spreadsheet is an example.)



PIN		voltage [V] positive							voltage [V] negative						
		1. voltage level		2. voltage level		max. voltage level		min	1. voltage level		2. voltage level		max. voltage level		min
1	name #1	140	F2.2			510	F2.2	140					510	--	510
2	name #2	20	F3.2	27,5	F2.1	510	F2.1	20	5	F3.1	7,5	F2.3	510	F2.3	5
3	name #3					510	-	510					510	-	510



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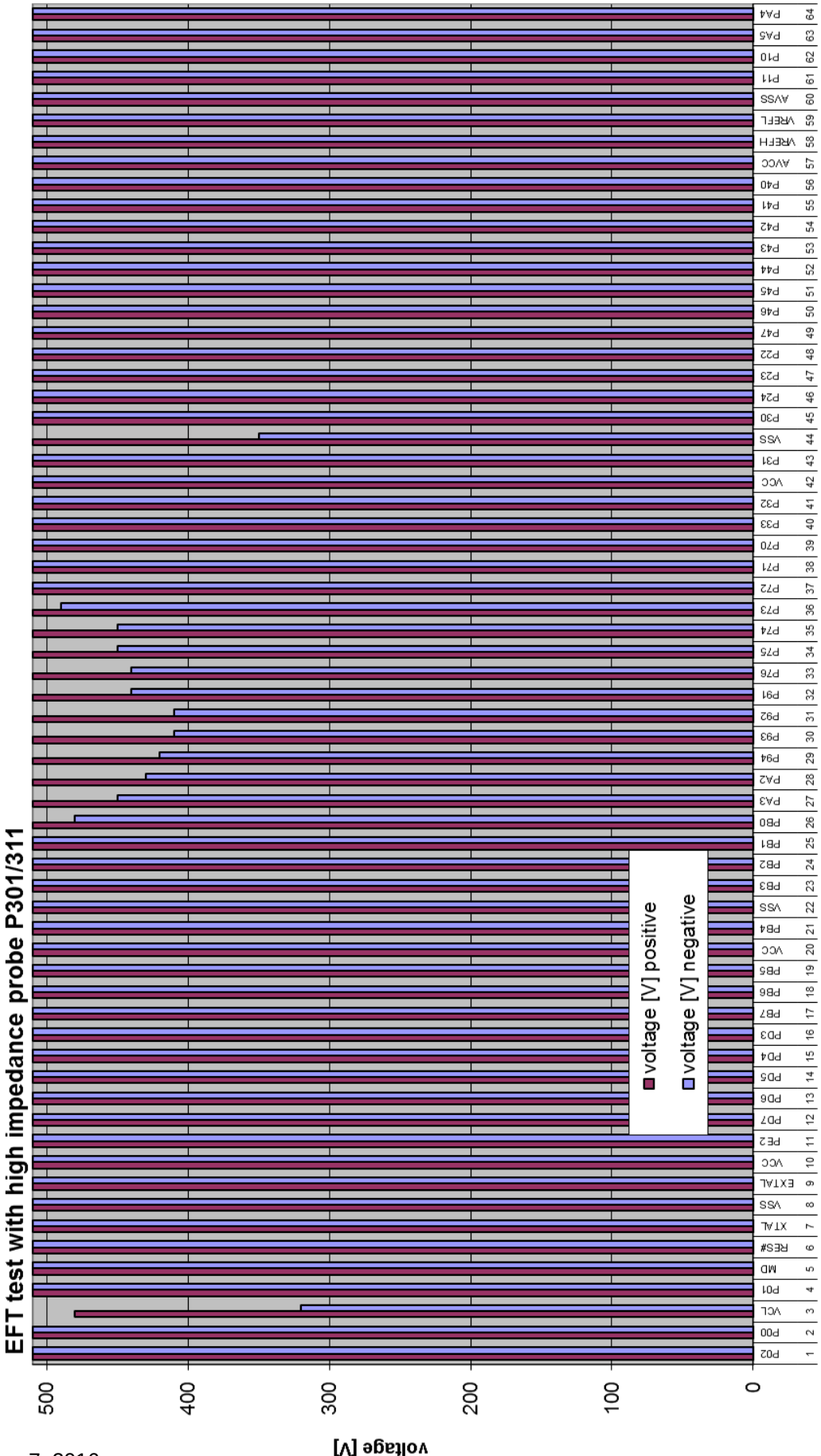

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Annex A: General description of the EFT test

1 Objective

Apart from its layout and housing design, the characteristics of the ICs which are used in a device are decisive for its EMC characteristics. The ICs susceptibility to disturbances increases significantly due to a reduction of their structural dimensions, operating voltages and operating points. The disturbance immunity is reduced to around 10 % of former ICs if the 100 nm world is approached or entered. This tendency is also reflected by the device behaviour.
Given identical functionality, a product's good EMC characteristics give manufacturers an edge over competitors. The objective is thus to determine those parameters which are decisive for disturbance immunity and allow the engineers to draw conclusions for chip design.
From the user's point of view, it stands to reason to compare different IC types under the conditions which prevail in his applications.

Current common IC test procedures

Today it is common practice with electronic components (ICs, transistors) to indicate a value of one to several kV with reference to the human body model as ESD immunity in specifications. A 100 pF capacitor which is charged to the test voltage is discharged to the DUT via 1500 Ohm. This test model is described in the MIL-STD-883G and IEC 801-2 standards. The machine model is another test model based on the same principle.
The test is exclusively used to ensure a certain stability of the IC to destruction when handling the component during manufacture, packaging, transport and assembly. The test object is, however, not connected to the power supply and thus not in operation.
The ESD immunities specified according to the human body model are not related to the ESD behaviour in operation. The protective mechanisms which are designed for the human body model may even cause problems in disturbance operating tests (without taking into account any disturbances in operation).

This approach means that a clear line has to be drawn between the objective of the present directive and that pursued by the test system from Langer EMV-Technik.

IC test system from Langer EMV-Technik

This test system refers to the ESD and burst immunity of PCBs and electronic devices. These are subjected to an ESD and burst test (IEC standard 61000-4-2/61000-4-4). The test voltages are in the kV range. The ICs themselves have considerably lower disturbance levels.
The pulsed voltages which are applied to the device from outside are attenuated on their way to the IC. Voltages of several kV outside of the device are thus reduced to around 1 ... 100 V on the IC pin.

The I**C test system** has been developed to test the IC immunity to pulsed disturbances.

The IC test system permits the

- user of ICs:
    - to keep track of changes in disturbance immunity
    - to take control over component selection and layout
    - to make decisions on where to use the IC

- manufacturer of ICs:
    - to check the immunity of existing ICs to disturbances
    - to identify the causes of disturbances and improve the IC

2 Set-up of the IC test system

An RF-proof IC (DUT) connection is the basic requirement for correct measurements. A solid GND plane is thus used as a reference plane in which the DUT is inserted using an IC adapter testboard (Figure 1) which has a continuous GND plane too.
The respective measuring task determines which of the different probes is used for the actual measurement. The probe is positioned so that a large part of its surface rests on the GND plane and thus provides an electric connection. The measuring connection is established to the DUT pin under test via the probe's pin contact. This confined set-up and the continuous GND plane ensure that correct measurements can be performed up to and even in the GHz range.

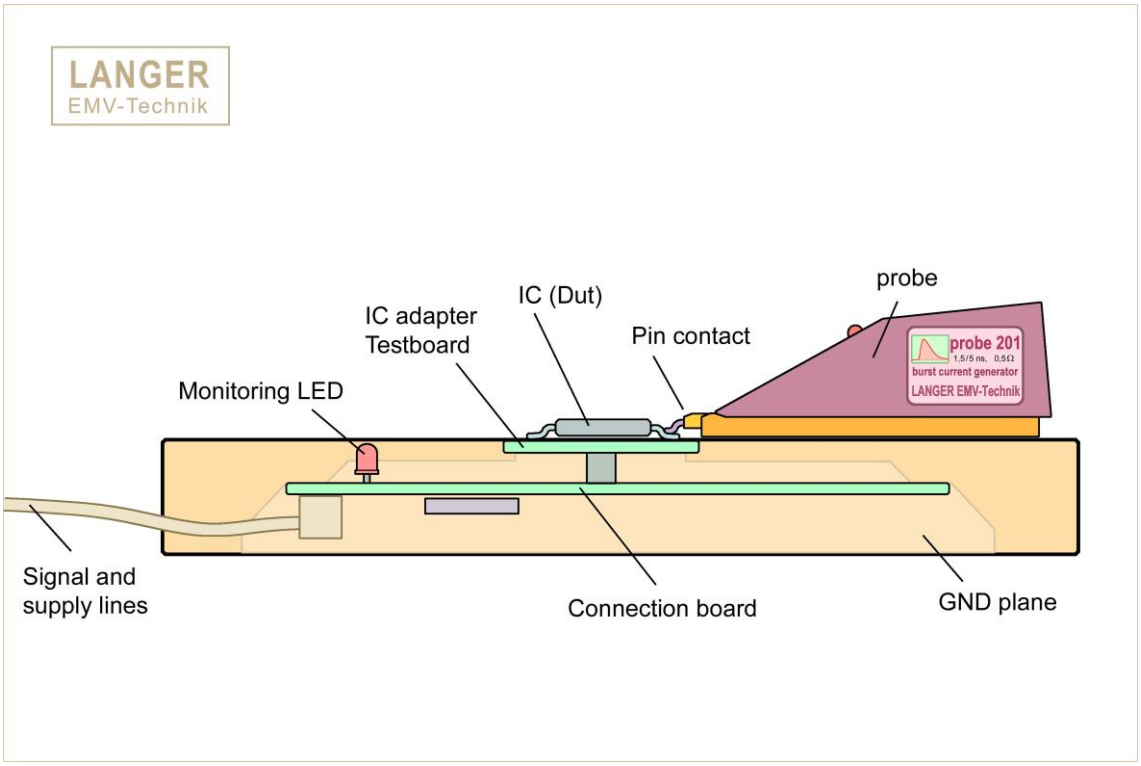

Figure 1 - test set-up

The measurement system comprises the following components:

1. GND plane including a connection board
2. IC adapter testboard (must be manufactured for the respective IC types)
3. BPS 201 (burst power station) for control
4. P200 / P300 probes for conducted disturbances
5. Operating software for the PC

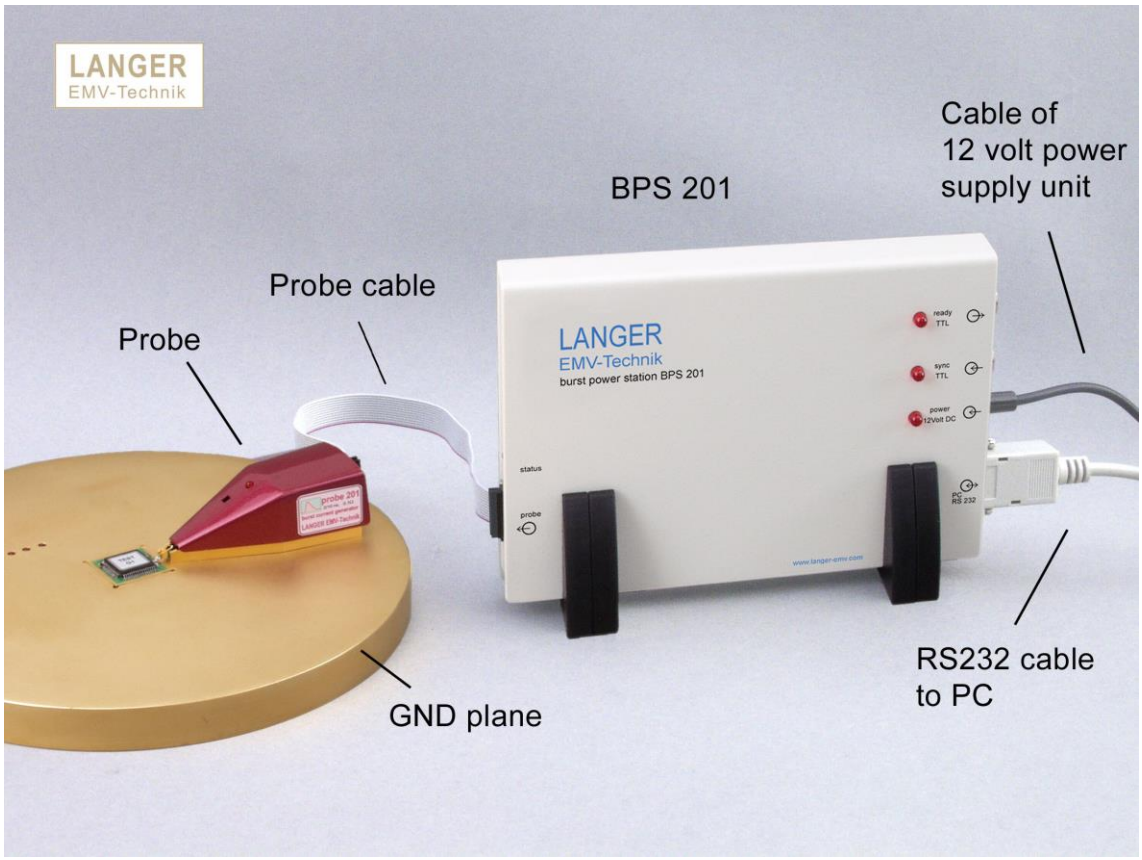

Figure 2 - components of the IC test system

The IC adapter testboard must be manufactured before measurements can be performed on an IC. This testboard has several tasks:

1. A continuous contact with the GND plane must be ensured to guarantee correct measurements.
2. The supply voltage must be connected depending on the measuring task and blocked in a defined way by filter elements.
3. The relevant signals must be provided or read out to ensure the chip's function. The lines required for this purpose must be equipped with appropriate filters.

The IC adapter testboard is plugged onto the connection board. The various ports of the IC under test are supplied with power and monitored / controlled via this connection board and connecting cable.

3 Definition of test pulses

The IC test pulses are defined on the basis of the device test procedures. The respective test set-ups generate electric and magnetic fields in the device. These quantities also have a local effect at the interface to the IC housing. IC test generators must provide a universally applicable simulation of these electric and magnetic quantities. Figure 3 shows the set-up principle of a burst or ESD test-bench. The test pulse $u_G(t)$ which is applied to the DUT generates a current pulse i(t) which flows through the device. A voltage drop $\Delta u(t)$ occurs in the device. The voltage $\Delta u(t)$ results in an electric field strength E(t) in the device. The pulsed magnetic field H(t) which is generated in the device results from the current i(t). These fields have an indirect effect on the IC via the conductor runs connected from outside or a direct effect on the IC housings.

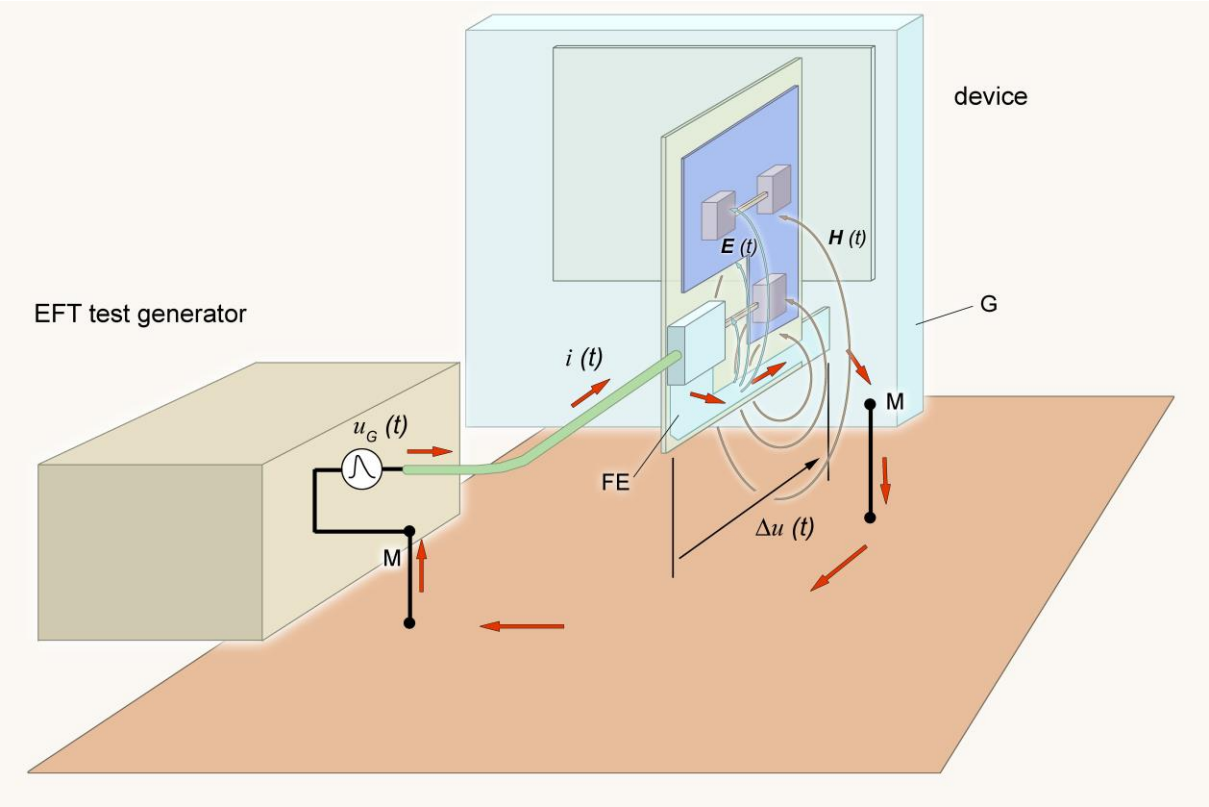

Figure 3 - set-up EFT test-bench

3.1 Magnetic coupling

A pulsed disturbance current which flows through a PCB generates pulsed magnetic fields. These magnetic fields B_{St} can couple into conductor loops and induce disturbance voltages u_{St}. There are two ways on which such a pulsed magnetic field can interfere with the IC function (Figure 4):

a) The induced voltage influences the IC pin which has been selected as the input. The disturbance voltage u_{St} is converted into a disturbance signal in the IC by the input circuit and further processed like a logical signal.

b) The induced voltage drives a disturbance current i_{St} into the IC pins. This disturbance current is driven directly to the IC's internal Vdd / Vss system if these are Vdd / Vss pins. However, it can also penetrate via signal pins and be guided to the IC's internal Vdd / Vss-System via internal drivers or damping diodes or capacitances. The Vdd / Vss system conducts the disturbance current to other functional components of the IC so that disturbances can occur in areas which have no functional connection to the affected pins.

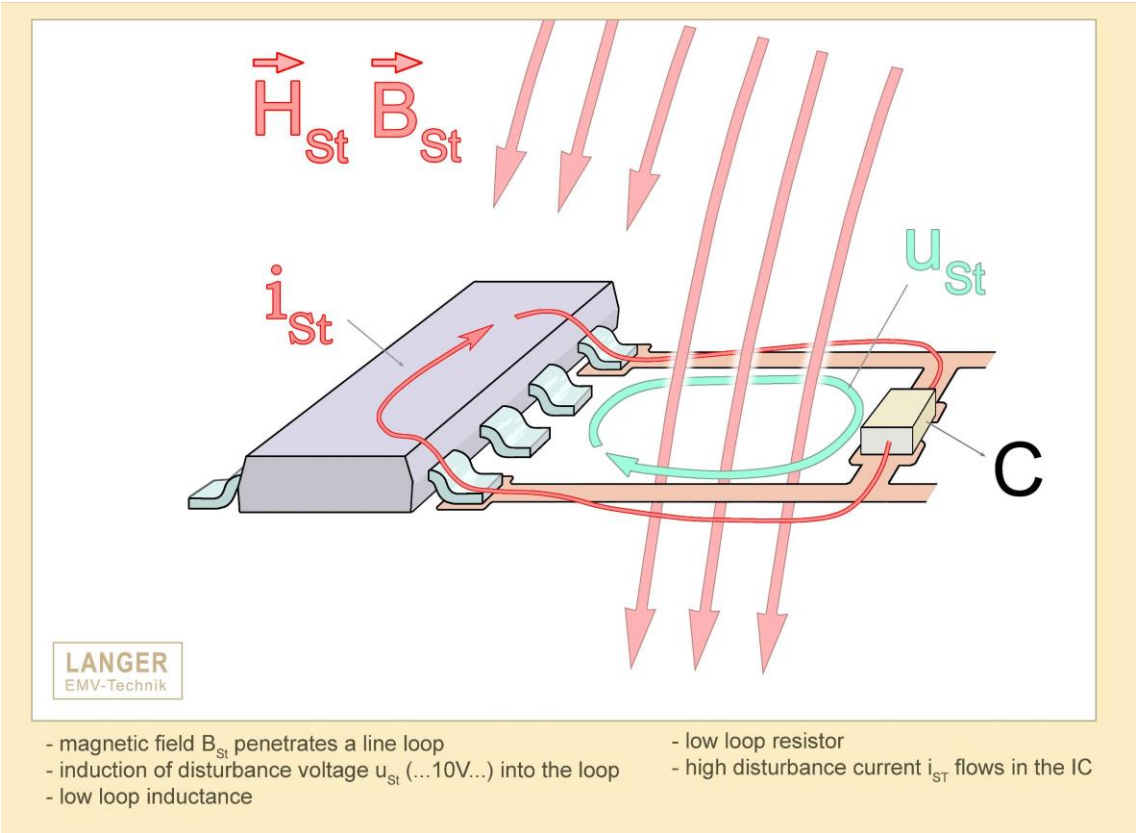

Figure 4 - influences with pulsed magnetic fields

3.2 Electric coupling

Assemblies can be subjected to pulsed electric fields of several 10,000 V/m (measurement set-up acc. to IEC 61000-4-4). The PCB's conductor systems receive this field (Figure 5).
A displacement current D flows to the environment via the conductor's parasitic capacitance. The IC which is connected to the lines can be interfered with in two ways:

a) Essentially, the conductor system has R and L switch elements as well as diodes against Vdd and Vss on the PCB and in the IC. The displacement current generates a disturbance pulse u_{St} on these elements. This disturbance pulse is converted into a disturbance signal by the IC's input circuit and further processed like a logical signal.

b) The displacement current is divided into two shares. A first share drains via the PCB's equivalent elements and any anti-interference capacitors that may be present. The second share of the disturbance current i_{St} flows through the IC to the Vdd / Vss system via the drivers or damping diodes. It generates an effect that is similar to that of magnetic field coupling.

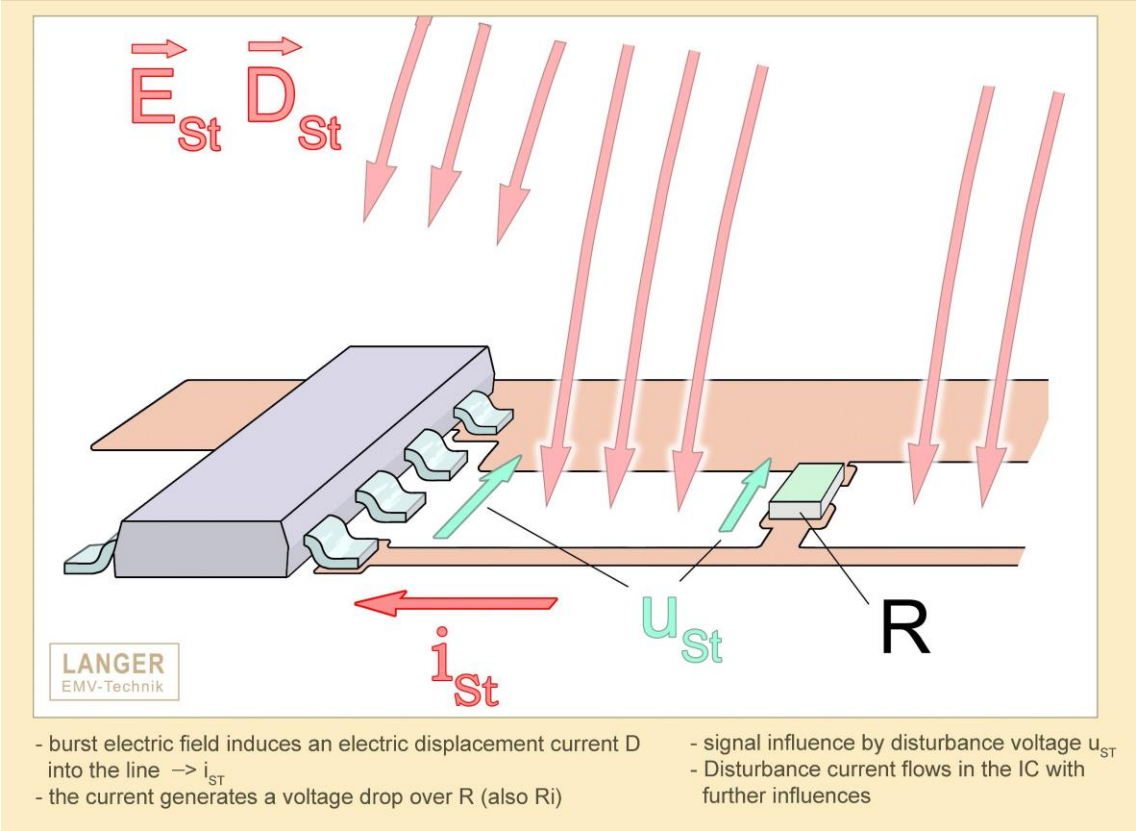

Figure 5 - influences with pulsed electric fields

4 Test pulses and test generators

The probes from the P200 and P300 series are provided for disturbance pulse coupling. Their dimensional design is adapted to the mechanisms used for coupling pulses into the electronic assemblies. Probes from the P200 series are provided for generating disturbances by pulsed magnetic fields. These probes have a higher coupling capacitance then those from the P300 series and a very low resistance.
The probes are supplied and controlled by the BPS 201 burst power station.

4.1 Test generator with low impedance

The probes from the P200 series are provided for generating this type of pulse (Figure 6). These probes must simulate the induction loop of the PCB. In extreme cases, this induction loop may comprise the IC's internal current path and a blocking capacitor which is connected to the pins.
The equivalent circuit of the entire current loop can have several hundred mΩ and some nH. The probe is thus designed to have a low resistance and low inductance (1 Ω, 2 nH).

The generator voltage value which is set on the PC corresponds to the disturbance effect of the probe in no-load operation.
Figure 6 shows a voltage pulse which has been coupled into different loads via a P200 probe.

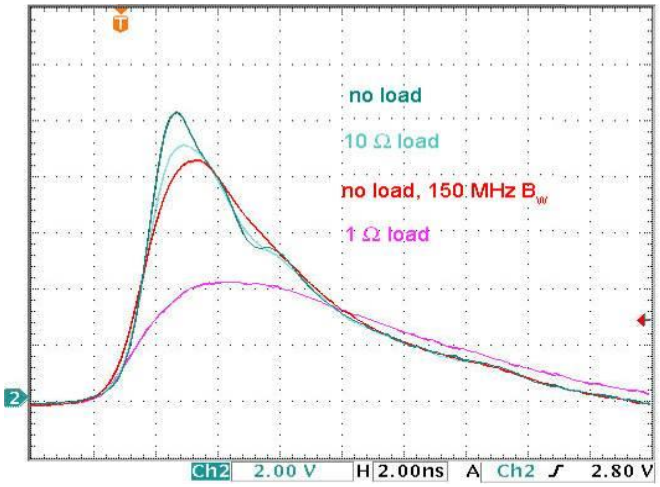

Figure 6 - voltage pulse of P200 on different loads

Technical parameters:

Probes:	**Probe 201**	**Probe 211**
Pulse shape:	1.5 / 5 ns	1.5 / 5 ns
Coupling capacitance:	1.2 µF	1.2 µF
Internal resistance:	1 Ω	1 Ω
Internal inductance:	approx. 2 nH	approx. 2 nH
Pulse voltage:	± 5 - 35 Volt	± 0.5 - 5 Volt

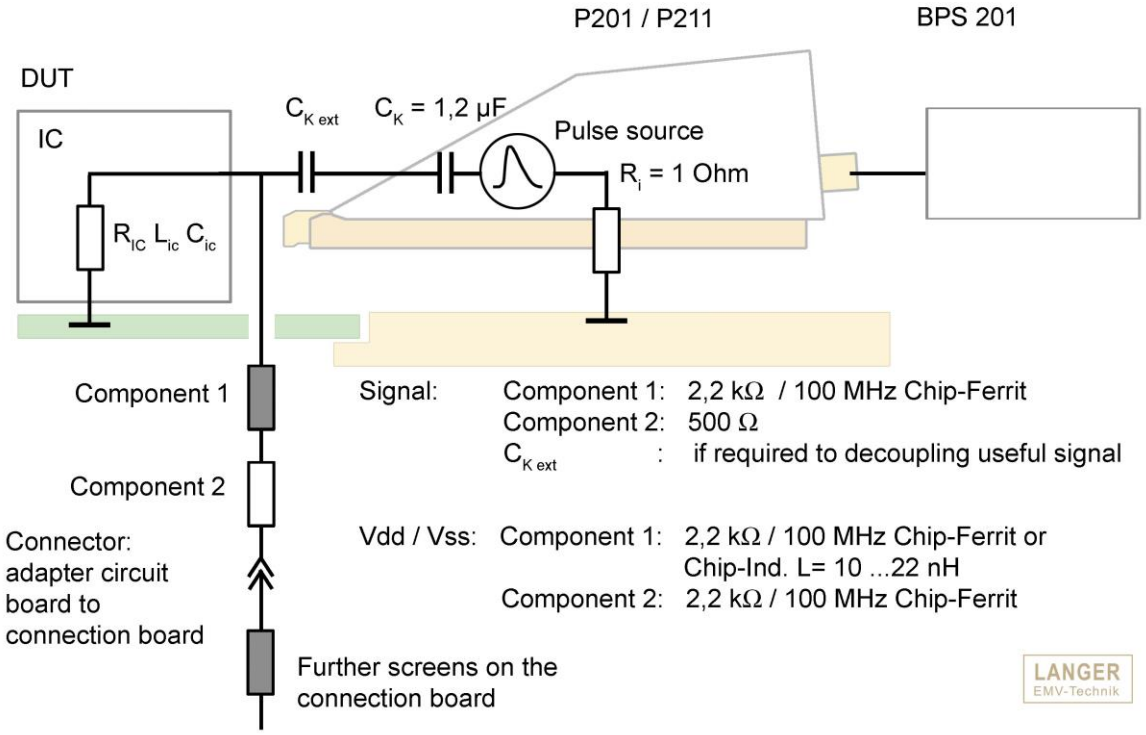

Figure 7 - generator parameters P201 / P211

4.2 Test generator with high impedance

The probes from the P300 series simulate the displacement current coupling of the electric field. The probes couple voltage pulses (Figure 8) with a rise time of 1.5 ns that originate from a coupling capacitance of 18 pF into the IC. In general, the voltage pulses are short-circuited in the IC against Vdd / Vss via clamping diodes or conductor systems. The generator functions as a pulsed current source. The current pulse (Figure 9) depends on the generator parameters.

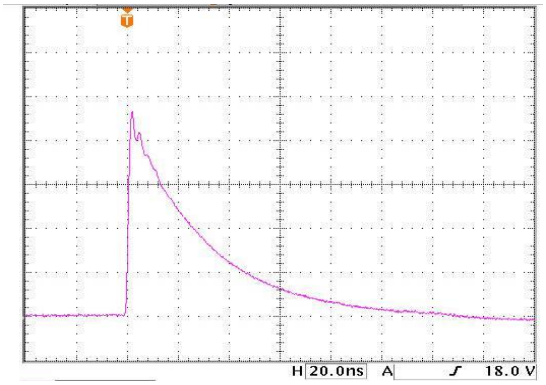

Figure 8 - P300 no-load voltage

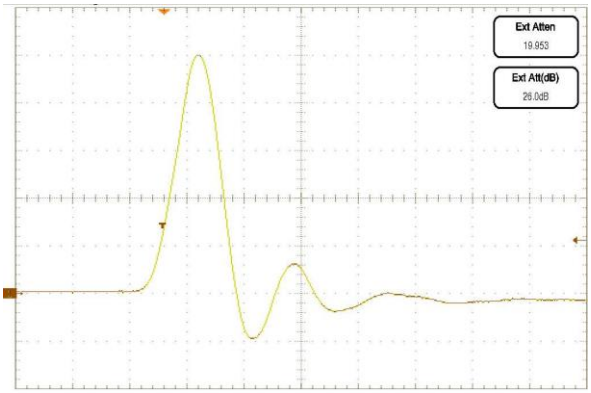

Figure 9 - P300 current pulse on a load of 2.5 Ω

Technical parameters:

Probes:	**Probe 301**	**Probe 311**
Pulse shape:	1.5 / 20 ns	1.5 / 20 ns
Coupling capacitance:	18 pF	18 pF
Internal resistance:	100 Ω	100 Ω
Internal inductance:	approx. 50 nH	approx. 50 nH
Pulse voltage:	± 120-500 Volt	± 5-140 Volt

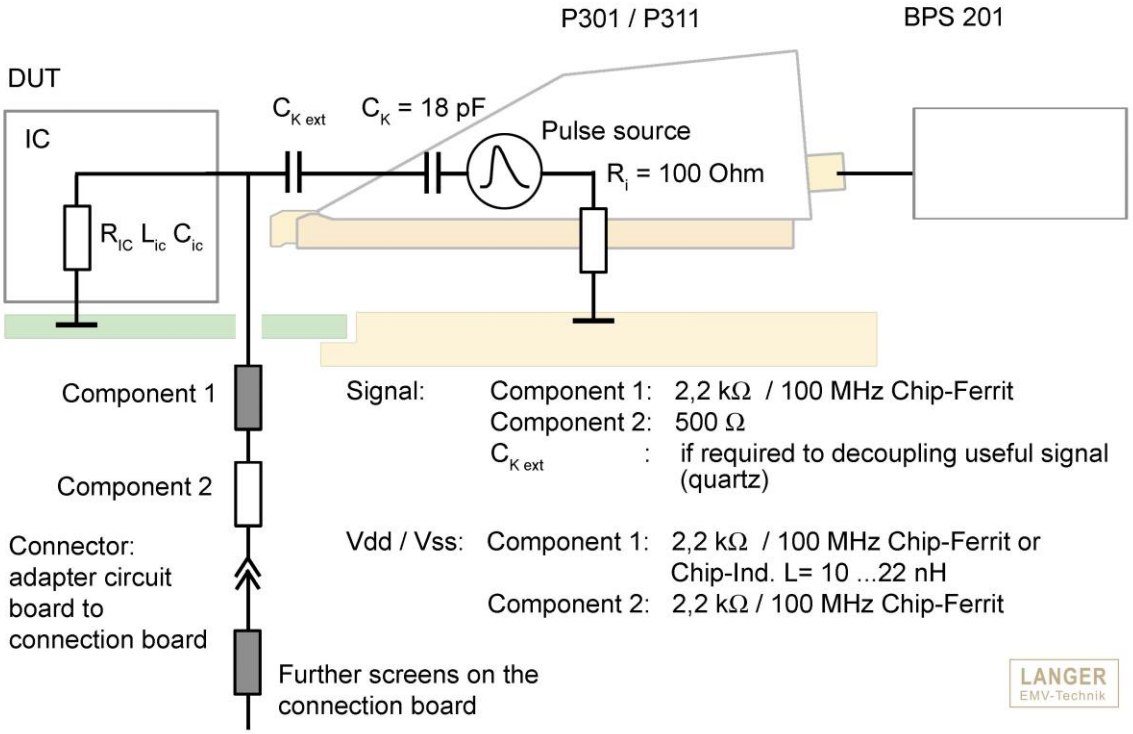

Figure 10 - generator parameters P301 / P311

Annex B: Evaluation of immunity

Recommended evaluation of the immunity test results on ICs:

Probe family 200 - Pulse current injection

Immunity of supply pins:

Voltage at probe (off-load voltage)	Evaluation of the immunity
< 3 Volt	very low
3 ... 10 Volt	low
10 ... 20 Volt	medium
> 20 Volt	high

Immunity of signal pins:

Voltage at probe (off-load voltage)	Evaluation of the immunity
< 10 Volt	very low
10 ... 20 Volt	low
20 ... 25 Volt	medium
> 25 Volt	high

Probe family 300 - Pulse voltage test

Immunity of signal pins:

Voltage at probe (off-load voltage)	Evaluation of the immunity
< 50 Volt	very low
50 ... 150 Volt	low
150 ... 300 Volt	medium
> 300 Volt	high