ClockMatrix Firmware Version v4.9.8

Contents

1. Overview

This document describes changes in the functionality and register map between firmware version 4.9.8 and version 4.9.6.

Table 1. Related Documents

Document Title	Document Description
Device Datasheet	Contains a functional overview of a specific device and hardware design related details including pinouts, AC and DC specifications, and applications information related to power filtering and terminations.
8A3xxx Family Programming Guide v4.9 dated May 1, 2024	Contains detailed register descriptions and address maps for all members of the family of devices. All devices use some subset of this register map.

2. Firmware Version Number

The firmware version can be read from the GENERAL_STATUS registers as shown in the following table.

Register Module Base Address: C014h			Firmware Version v4.9.6	Firmware Version v4.9.8
Offset Address (Hex)	**Individual Register Name**	**Register Description**	**Default Value**	**Default Value**
010h	GENERAL_STATUS.MAJ_REL	Major release number	09h	09h
011h	GENERAL_STATUS.MIN_REL	Minor release number	09h	09h
012h	GENERAL_STATUS.HOTFIX_REL	Hotfix release number	06h	08h

3. Improvements in Version 4.9.8 Added Since Version 4.9.6

Issue Number: BRMBXR-3679	
Firmware	**Functional Difference**
v4.9.6	When a DPLL is configured to follow the feedback clock of another DPLL, if the index of the master channel is higher than the index of the follower (e.g., DPLL0 follows DPLL1) then the follower can remain in the Freerun state for up to 10 seconds (approximately) before it begins locking to the master.
v4.9.8	A DPLL can be configured to follow the feedback clock of any other DPLL, and it will lock as expected.

Issue Number: BRMBXR-3689	
Firmware	**Functional Difference**
v4.9.6	The following applies when the DPLL_COMBO_SW_VALUE_CNFG field is set to a non-zero value. If the total FFO sent to an FOD is zero or near zero, then phase transients of up to 50 ns (approximately) can occur randomly on the FOD output clock. The total FFO means the total from all sources, including DPLL_COMBO_SW_VALUE_CNFG, the DPLL filter associated with the FOD and any source over the Combo Bus.
v4.9.8	The DPLL_COMBO_SW_VALUE_CNFG field operates as expected.

Issue Number: BRMBXR-3696	
Firmware	**Functional Difference**
v4.9.6	The FODs use divide ratios consisting of an integer part and a fractional part. In cases when the integer part is toggling, phase transients of up to 50 ns (approximately) can occur randomly on the FOD output clock.
v4.9.8	The FODs operate as expected.

4. Renesas Documentation

Issue Number	Description
BRMBXR-3678 BRMBXR-3680 BRMBXR-3694 BRMBXR-3697	These issues are related to Renesas documentation and interim firmware versions.

5. Register Differences Between Version 4.9.8 and Version 4.9.6

Register Module Base Address: C014h		
Offset Address (Hex)	**Individual Register Name**	**Change**
012h	GENERAL_STATUS. HOTFIX_REL	Default value is 8.

6. Revision History

Revision	Date	Description
1.01	Dec 8, 2025	Final release.
1.00	May 1, 2024	Initial release.

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