CS+ Instruction Simulator for RH850 V5.05.00

Release Note

Thank you for using the CS+ integrated development environment.

This document describes restrictions on and points for caution regarding the simulator.

Read this document before using the product.

Contents

Chapter 1. Target Devices

The simulator allows the simulation of instructions for the following RH850 CPU cores: RH850G4MH, RH850G3M, RH850G3MH, RH850G3K, and RH850G3KH.
The target devices the CS+ IDE supports are listed on the Web site.
Please see the URL below.

CS+ Product Page

https://www.renesas.com/cs+

Chapter 2. User's Manuals

Please read the following user's manuals together with this document.

Manual Name	Document Number
CS+ V8.07.00 RH850 Debug Tool	R20UT5061EJ0100
CS+ V8.07.00 Message	R20UT5057EJ0100

Chapter 3. Uninstallation

There are two ways to uninstall this product.

- Use the integrated uninstaller from Renesas (uninstalls all CS+ components)
- Use the Windows uninstaller (only uninstalls this product)

To use the Windows uninstaller, select [CS+ for CC] from [Apps & features] from [Settings] of Windows or [Programs and Features] of the control panel.

Chapter 4. Changes

This chapter describes changes from V5.04.00 to V5.05.00 of the instruction simulator for RH850 devices.

4.1 Improvements

4.1.1 Operation in writing to the read-only I/O registers

In the RH850 instruction simulator, the access attribute of the I/O register is R/W (readable and writable), and writing to the read-only I/O registers is now possible except for some registers. This enables writing pseudo-values to the read-only I/O registers and proceeding with simulation on the [IOR] panel or via the Python console.

For points for caution on writing to the read-only I/O registers, refer to section 5.6, Operation in writing to the read-only I/O registers.

4.1.2 Improvements to the operation when the name of a path to the project folder includes single-byte space characters

In the RH850 instruction simulator, operation in cases where the name of a path to the project folder includes single-byte space characters has been improved in the following ways.

(1) When a device has the virtualization facility, even if [Enable] was specified for [Initial state of the hardware-assisted virtualization] in the [Hardware-assisted Virtualization] category on the [Connect Settings] tabbed page of the [Property] panel of the simulator, the simulator would operate with the virtualization facility disabled. However, this problem has been corrected so that the simulator operates according to the settings.

(2) Even if [Yes] was specified for [Permit writing to the writing prohibited area] in the [Memory] category on the [Debug Tool Settings] tabbed page of the [Property] panel of the simulator, a break would occur in the case of writing to a writing-prohibited area. However, this problem has been corrected so that the simulator operates according to the settings.

(3) For a device that supports the map mode for memory, even if a setting other than [Single map mode] was selected for [Map mode] in the [Memory] category on the [Connect Settings] tabbed page of the [Property] panel of the simulator, the simulator would operate in single-map mode. However, this problem has been corrected so that the simulator operates in the selected map mode.

4.2 Eliminated restriction

4.2.1 Simulation of an MPU facility

The following restriction in V5.04.00 has been eliminated. If all MPU entries are disabled (MPATn.E=0), an MIP exception does not occur when MPM.MPE=1 (the MPU facility is enabled), MPM.SVP=0, and an instruction is executed in SV mode.

Restriction in the release notes for V5.04.00:

✓ Simulation of an MPU facility

[Affected device] RH850G4MH

[Details] Even if all MPU entries* are disabled (MPATn.E=0), an erroneous MIP exception occurs when MPM.MPE=1 (the MPU facility is enabled), MPM.SVP=0, and an instruction is executed in SV mode.

Note: MPU entries must be replaced by the following words in host and guest modes of G4MH2.0.

G4MH2.0 host mode: Host management MPU entries

G4MH2.0 guest mode: Guest management MPU entries

Chapter 5. Points for Caution

This chapter describes points you will need to note when you are using the simulator.
For details, refer to section 2.3.3, [Simulator], in the CS+ V8.07.00 Integrated Development Environment User's Manual: RH850 Debug Tool.

5.1 CPU Operating Clock

The CPU clock operates at the frequency set up with the property "Main clock frequency [MHz]" of the simulator.

5.2 Access Latency

Since the latency of access to the various types of memory and peripheral modules is not considered, the execution times (numbers of cycles) will be different from those for the actual device.
Thus, the results of measuring the following items differ according to whether the instruction simulator or an actual device is in use.

- The results of measurement by the Run-Break timer
- The results of measurement of Timer Result events
- The [Pipeline] area of the Trace panel
- The [Time] area of the Trace panel
- Result of tracing when the trace target is selected as [All core] (timing between processor elements)
- Timestamps of the software trace data

5.3 Peripheral Functions

The simulator does not support simulation of the peripheral functions.

5.4 Controlling Booting up of Individual CPUs

Some RH850 MCUs have specific option bytes for selecting the boot mode for the CPUs and IO registers for selecting which CPUs should be booted up when the MCU is reset. The simulator, on the other hand, does not support such facilities and all CPUs are booted up when the MCU is reset.

5.5 Simulation for RH850G3KH2.0 core

The instruction simulator for RH850 devices works according to the specification for RH850G3KH core equipped on RH850/F1K etc. when the target device has RH850G3KH core (which includes

RH850G3KH2.0 core). Therefore, when simulating a product with RH850G3KH2.0 core, LDL.W and STC.W behave differently from the target device.

5.6 Operation in writing to the read-only I/O registers

In the RH850 instruction simulator, the access attribute of the I/O register is R/W (readable and writable), and writing to the read-only I/O registers is possible except for some registers.
For the read-only I/O registers in INTC1, INTC2, IPG, and IPIR, note that no values can be written even if the access attribute is displayed as R/W in the [IOR] panel.

Chapter 6. Restriction

This chapter describes restriction on the use of the simulator.

6.1 Simulation of the HALT Instruction

[Affected device] RH850G4MH

[Details] Execution of the HALT instruction is not reflected in the results of tracing. However, the results of tracing in the processor elements for which the HALT instruction was not executed are not affected.

[Workaround] There is no workaround.

[Schedule for fixing the problem] We will fix this problem in the next and subsequent versions.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec.03.21	-	First Edition

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