

RZ/T2, RZ/N2

EtherNet/IP OpENer Sample Program Package

Introduction

This document is a release note for the EtherNet/IP protocol stack sample program package for RZ/T2 and RZ/N2 series microprocessor.

This release note describes the structure of this package.

Target Device

RZ/T series: RZ/T2M, RZ/T2ME, RZ/T2H Group

RZ/N series: RZ/N2L, RZ/N2H Group

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1. Overview

This release note applies to the EtherNet/IP protocol stack sample program package for RZ/T2 and RZ/N2 series microprocessor.

1.1 Requirements

This sample program package runs under the operating requirements below.

Table 1.1 Requirements

Category	Name	Version	Description
Board	Renesas Starter Kit+ for RZ/T2M	-	Renesas RZ/T2M-RSK - Renesas Starter Kit Plus for RZ/T2M Renesas
	Renesas Starter Kit+ for RZ/T2ME	-	Renesas RZ/T2ME-RSK - Renesas Starter Kit+ for RZ/T2ME Renesas
	RZ/T2H Evaluation Board	-	Renesas RZ/T2H-EVKIT - Evaluation Board Kit for RZ/T2H Renesas
	Renesas Starter Kit+ for RZ/N2L	-	Renesas RZ/N2L-RSK - Renesas Starter Kit+ for RZ/N2L Renesas
	RZ/N2H Evaluation Board	-	Renesas RZ/N2H-EVKIT - Evaluation Board Kit for RZ/N2H Renesas
IDE	EWARM	9.60.3	IAR Systems IAR Embedded Workbench for Arm IAR
	e ² studio	2025-12	Renesas Release v4.0.0 · renesas/rz-fsp · GitHub
Configurator	FSP Smart Configurator	2025-12	
Flexible Software Package	FSP for Renesas RZ	4.0.0	
GCC Compiler	GNU ARM Embedded Toolchain	13.3.Rel1	
	GNU ARM A-Profile (AArch64 bare-metal)	13.2.Rel1	
Emulator	J-Link™	8.60	SEGGER SEGGER - The Embedded Experts - Downloads - J-Link / J-Trace
	I-jet	-	IAR Systems IAR debug probes IAR
Software	CODESYS	v3.5.21.10 64-bit	CODESYS GmbH CODESYS Group

2. Package folder structure

The folder structure of this sample program package is below.

Table 2.1 Folder structure

Item	Description
r01an8286xx0400-rzt2-rzn2-ethernetip-opener-package.zip	RZ/T2, RZ/N2 EtherNet/IP Sample Package
├── RZT2M_EtherNetIP_OpENer_RSK_rev0400.zip	Archive for RZ/T2M (RSK board)
├── RZT2H_EtherNetIP_OpENer_EVB_rev0400.zip	Archive for RZ/T2H (EVB board)
├── RZN2L_EtherNetIP_OpENer_RSK_rev0400.zip	Archive for RZ/N2L (RSK board)
├── RZN2H_EtherNetIP_OpENer_EVB_rev0400.zip	Archive for RZ/N2H (EVB board)
├── r01an6601ej0400_rzt2_rzn2_ethernetip_rsk.pdf	Application note
└── r01an8286ej0400-rzt2_rzn2_ethernetip_package.pdf	Release note

3. Feature added

This section describes package updates and function additions.

Rev.	Date	Description	
		Page	Summary
4.00	Apr. 13, 2026	-	Consolidate the EtherNet/IP Sample Program Packages for RZ/T2M, RZ/T2H, RZ/N2L and RZ/N2H into this single package. - And issue a new document number r01an8286
		-	Support FSP v4.0.0 for all devices
		-	Update for RZ/T2H, RZ.N2H Implement following - ACD Improve functionality equivalent to that required by CT21. - LLDP function - Connection state transition Remove Flash boot projects.
		-	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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