

RZ/T2L Group

RZ/T2L FuSa Reference Kit (CIP Safety)

Introduction

This document is the release note of CIP safety[™] for operating on the RZ/T2L Functional Safety Reference Board (hereinafter referred to as RZ/T2L FuSa Kit), which is equipped with two RZ/T2L MPUs manufactured by Renesas Electronics.

Target Device

RZ/T2L Group

R01AN7876JJ0100 Rev.1.00 Jun.30.2025



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1. Overview

CIP Safety is equipped on the RZ/T2L FuSa Reference Board manufactured by Renesas Electronics to perform CIP Safety communication.

2. Hardware Configuration

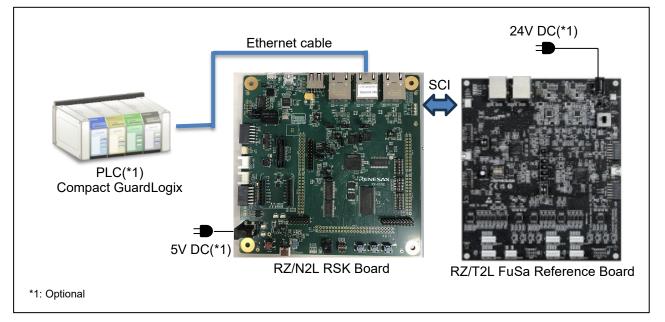


Figure 2-1 RZ/T2L FuSa Reference Kit Configuration

These boards can be purchased from the following URL.

RZ/N2L RSK Board: https://www.renesas.com/rzn2l-rsk RZ/T2L FuSa Reference Board: https://www.renesas.com/rzt2l-safety-network



2.1.1 Operation Environment

■RZ/T2L FuSa Reference Kit

ltem	Description		
Board	RZ/T2L FuSa Reference Kit		
MPU	RZ/T2L Group		
	R9A07G074M04GBG x2 : 196pinFBGA		
Operating frequency	CPU Core : 800MHz (Arm [®] Cortex [®] -R52)		
Operating voltage	3.3V/1.8V/1.1V		
Operating mode	xSPI0 boot mode(x1 boot serial flash)		
Device	Serial Flash ROM (64Mbyte)		
	Renesas Electronics AT25SF128A		
ntegrated development IAR Systems			
environment Embedded Workbench® for Arm Version 9.20.3(Functional Safet			
Emulator	IAR Systems		
	I-jet		
Software(*1)	RZ/T2L CIP Safety Reference Software Ver.1.00 or later		
	(P/N: RTK0EF0200F01001SJ_CI)		

*1: Download from QR code of CD-ROM included with the board.

■RZ/N2L RSK Board

ltem	Description
Board	RZ/N2L RSK Bard
MPU	RZ/N2L Group
	R9A07G084M04GBG: 225pinFBGA
Operating frequency	CPU Core : 400MHz (Arm [®] Cortex [®] -R52)
Operating voltage	3.3V/1.8V/1.1V
Operating mode	xSPI0 boot mode(x1 boot serial flash)
Device	Serial Flash ROM (64Mbyte)
	Macronix MX25UR51245GMI00
Integrated development IAR Systems	
environment	Embedded Workbench [®] for Arm Version 9.60.2 (FSPv2.1.0)
	Renesas Electronics
	e ² studio 2024-10 (FSPv2.1.0)
Emulator	IAR Systems
	I-jet
	Segger
	J-link OB
Software(*2)	RZ/N2L EtherNet/IP OpENer Sample Program Ver.2.10 or later

*2: <u>https://www.renesas.com/en/document/scd/rzn2l-group-ethernetip-opener-sample-program-package?language=en&r=1622401</u>



■Connecting Devices

Item	Description
PLC programming environment	Studio 5000 Logix Designer (9324M-RLDT11M Studio 5000 Lite Edition)
	(Rockwell Automation)
PLC	Compact GuardLogix SIL3 0.6.0,3M Motion : 5069-L306ERMS3(Rockwell
	Automation)
	Compact 5000 Spring RTB : 5069-RTB64-SPRING(Rockwell Automation)

*: For how to get them, please contact each manufacturer.



2.2 RZ/T2L FuSa Reference Board Settings

Table 2-1 shows RZ/T2L FuSa Reference Board Switch Settings, and Table 2-2 shows RZ/T2L FuSa Reference Board Jumper Settings.

Table 2-1 RZ/T2 L FuSa Reference Board Switch Setting

SW1

1	2	3	4	5	6	7	8
OFF							

SW2

1	2	3	4	5	6
OFF	OFF	OFF	OFF	OFF	OFF

SW3

1	2
OFF	OFF

SW4

1	2	3	4	5	6	7	8
OFF							

SW6

1	2
OFF	OFF

SW9-12

Switch	Left	Center	Right
Switch	Silkscreen: "LP-B"	Silkscreen: "F"	Silkscreen: "-"
	Loop-back connection	Pseudo stuck-at fault	Normal connection
SW9	RZ/T2L-B TXD4 RXD4 RXD4	RZ/T2L-B Stuck at "H" → RXD4	RZ/T2L-A RZ/T2L-B TXD4 RXD4
SW10	RZ/T2L-A TXD4 RXD4	RZ/T2L-A RXD4 Stuck at "H"	RZ/T2L-A RZ/T2L-B RXD4 - TXD4
SW11	RZ/T2L-B GTIOC10A GTETRGB	RZ/T2L-B Stuck at "L" → GTETRGB	RZ/T2L-A RZ/T2L-B GTIOC10A D→ GTETRGB
SW12	RZ/T2L-A GTIOC10A GTETRGB	RZ/T2L-A GTETRGB Stuck at	RZ/T2L-A RZ/T2L-B



SW13			
Switch	Left Silkscreen: SCI-CON	Center	Right Silkscreen: T2L-B
	Connected to: CON14	Connected to: None	Connected to: RZ/T2L-B
SW13	RZ/T2L-A CON14 TXD3 RXD3 RXD3 C TXD3 C TXD3 C TXD3 CON14 CON14 TXD3 CON14 TXD3 CON14	Setting not allowed	RZT2L-A RZT2L-B TXD3 RXD3 RXD3 TXD3
			1

Table 2-2 RZ/T2L FuSa Reference Board Jumper Settings

No.	Jumper	Setting
1	JP1	1-4 Short



2.3 RZ/N2L RSK Board Settings

Table 2-3 shows RZ/N2L RSK Board Switch Settings and Table 2-4 shows RZN2L RSK Board Jumper Settings.

Table 2-3 RZ/N2L RSK Board Switch Settings

SW3

1	2	3	4	
OFF	OFF	OFF	OFF	

SW4

1	2	3	4	5	6	7	8
ON	ON	ON	ON	OFF	OFF	OFF	OFF

SW8

1	2	3	4	5	6	7	8	9	10
OFF	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF

SW11

1	2	3	4	5	6	7	8	9	10
ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF

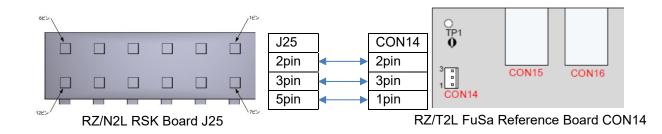
Table 2-4 RZ/N2L RSK Board Jumper Settings

No.	Jumper	Setting	
1	JP9	Open	
2	CN8	2-3 short	
3	CN17	1-2 short	
4	CN20	2-3 short	
5	CN21	2-3 short	
6	CN22	2-3 short	
7	CN24	2-3 short	
8	CN25	1-2 short	
9	CN27	1-2 short	
10	CN29	1-2 short	
11	CN31	1-2 short	
12	CN32	1-2 short	



2.4 RZ/T2L FuSa Reference Board and RZ/N2L RSK Board Settings

Connecting with RZ/T2L FuSa Reference Board and RZ/N2L RSK Board is shown the below.





3. Operating Procedure

3.1 How to write Program

■RZ/N2L RSK Board

Refer to "Quick Start Guide: EtherNet/IP OpENer Sample Program(r01an6601)" in RZ/N2L EtherNet/IP OpENer Sample Program Package.

■RZ/T2L FuSa Reference Board

Refer to "RZ CIP Safety Reference Software Development Handbook (R30UZ0217)" in RZ/T2L CIP Safety Reference Software Package.

3.2 Operation

Refer to "RZ CIP Safety Reference Software Development Handbook (R30UZ0217)" in RZ/T2L CIP Safety Reference Software Package.



Revision History

		Description	
Rev.	Date	Page	Summary
1.00	Jun.30. 2025	-	First edition issued



General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power is supplied until the power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

- 6. Voltage application waveform at input pin Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
- 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a systemevaluation test for the given product.

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