RZ/T2N Group

Encoder I/F HIPERFACE DSL Sample Program

Summary

This document describes the package contents of the RZ/T2N Encoder I/F HIPERFACE DSL® sample program.

Functionality Checked Device

RZ/T2N Evaluation Board (RTK9RZT2Nxxxxxxxxx)

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1. Package Contents

This package contains the following items.

The RZ/T2N encoder interface supports up to 8 axes, but the sample program uses only 1 of those axes. If you use 2 or more axes simultaneously, modify the sample program to support the required number of axes.

1.1 Software

- Source Code

No.	Name	Version number
1	RZ/T2N HIPERFACE DSL sample program (CR52 ver. *)	4.0
2	RZ/T2N HIPERFACE DSL sample program (CA55 ver. *)	4.0

Note: This sample program has a CR52 version that runs on the CPU core Cortex-R52 and a CA55 version that runs on the CPU core Cortex-A55. CR52 ver. and CA55 ver. are descriptions of the respective versions.

1.2 Documents

No.	Document name	Version	File name
1	RZ/T2N Group Encoder I/F HIPERFACE DSL Sample Program Release Notes	4.00	(j) r11an1036jj0400-rzt2n.pdf (e) r11an1036ej0400-rzt2n.pdf (this document)
2	RZ/T2N Group HIPERFACE DSL Sample Program	4.00	(j) r11an1035jj0400-rzt2n-hfdsl.pdf (e) r11an1035ej0400-rzt2n-hfdsl.pdf

2. File Structure

The file structure and contents of this package are shown below.

```
Top
 ├── r11an1036jj0400-rzt2n.pdf
 ├── r11an1036ej0400-rzt2n.pdf
 ├── SBOM
 │    ├── RZT2N_hfdsl_evb_rev4.00.json        : Sample program SBOM information
 │    └── RZT2N_hfdsl_evb_rev4.00.spdx        : Sample program SBOM information
 └── workspace
      ├── Software
      │    ├── iccarm
      │    │    ├── RZ_T2N_CR52_hfdsl.zip     : RZ/T2N HIPERFACE DSL sample program set
      │    │    │                               CR52 ver. (EWARM)
      │    │    └── RZ_T2N_CA55_hfdsl.zip     : RZ/T2N HIPERFACE DSL sample program set
      │    │                                    CA55 ver. (EWARM)
      │    └── gcc
      │         ├── RZ_T2N_CR52_hfdsl.zip     : RZ/T2N HIPERFACE DSL sample program set
      │         │                               CR52 ver. (e2 studio)
      │         └── RZ_T2N_CA55_hfdsl.zip     : RZ/T2N HIPERFACE DSL sample program set
      │                                         CA55 ver. (e2 studio)
      └── Documents
           ├── r11an1035jj0400-rzt2n-hfdsl.pdf
           └── r11an1035ej0400-rzt2n-hfdsl.pdf
```

The file structure of the RZ_T2N_CR52_hfdsl.zip and RZ_T2N_CA55_hfdsl.zip is shown below.

```
Top folder
 ├── configuration.xml                : FSP Configuration data
 ├── ( Environment File Depending on Build Tool )
 └── src
      ├── hal_entry.c                 : HIPERFACE DSL sample program
      ├── hfdsl_main.c                : HIPERFACE DSL sample program
      ├── siochar.c                   : SCI_UART sample program
      ├── syscalls.c                  : SCI_UART sample program
      ├── sio_char.h                  : SCI_UART sample program
      └── drv
           └── hfdsl
                ├── iodefine_hfdsl.h      : HFDSL register definition file
                ├── r_hfdsl_rzt2.c        : HFDSL driver file
                ├── r_hfdsl_rzt2_config.h : HFDSL driver file
                ├── r_hfdsl_rzt2_dat.h    : HFDSL driver file
                └── r_hfdsl_rzt2_if.h     : HFDSL driver file
```

3. About HIPERFACE DSL Sample Program

This section contains information necessary to use the complete set of HIPERFACE DSL sample program.

3.1 Software Information

3.1.1 Base OS

This sample program is OS-independent.

3.1.2 Memory Size

Memory sizes used by this sample program and the HFDSL driver are shown in the following table. This table excludes memory used by the Flexible Software Package and the compiler C language libraries.

(1) CR52 version

Items		Memory Size	
		EWARM [kBytes]	e² studio [kBytes]
HFDSL driver	Code	3.4	2.5
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.2	0.2
	Constant Data	0.3	1.1
Sample program	Code	1.8	2.1
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.3	0.3
	Constant Data	0.8	0.1

(2) CA55 version

Items		Memory Size	
		EWARM [kBytes]	e² studio [kBytes]
HFDSL driver	Code	4.7	3.8
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.3	0.3
	Constant Data	0.5	1.8
Sample program	Code	3.1	3.8
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.3	0.3
	Constant Data	0.9	0.1

3.2 Hardware Information

3.2.1 Device

RZ/T2N

3.2.2 Target Board

(1) Board Name

RZ/T2N Evaluation Board (RTK9RZT2Nxxxxxxxxx)

(2) Setting of the Target Board

The target board configuration is as follows.

SW7-3: OFF, SW7-4: OFF, SW7-5: OFF, SW7-6: OFF, SW7-7: OFF, SW7-8: OFF

SW9-3: OFF, SW9-5: OFF, SW9-6: OFF, SW9-7: OFF, SW9-8: OFF

SW12-5: ON, SW13-1: ON, SW13-2: OFF, SW13-6: ON, SW13-7: OFF

SW8-1: ON, SW8-2: OFF, SW8-3: ON (Set xSPI1 boot mode)

SW10-3: OFF, J18: Short between 2-3 pins (Set VCC1833_2 to 3.3 V)

SW10-6: OFF, J39: Short between 2-3 pins (Set VCC1833_5 to 3.3 V)

(3) Used pins of the Target Board

The correspondence between the pin used as the encoder I/F and the pin header of the target board is as follows.

Channel	Port Name	Pin Header	Input/Output	Voltage Domain	Description
HFDSL0	ENCIFDI0 (dsl_in)	J49 #44	Input	VCC1833_2	Data input
	ENCIFDO0 (dsl_out)	J49 #43	Output	VCC1833_2	Data output
	ENCIFOE0 (dsl_en)	J49 #42	Output	VCC1833_2	Drive/receive control
HFDSL1	ENCIFDI1 (dsl_in)	J50 #44	Input	VCC1833_2	Data input
	ENCIFDO1 (dsl_out)	J50 #43	Output	VCC1833_2	Data output
	ENCIFOE1 (dsl_en)	J50 #42	Output	VCC1833_2	Drive/receive control
HFDSL2	ENCIFDI2 (dsl_in)	J51 #44	Input	VCC33	Data input
	ENCIFDO2 (dsl_out)	J51 #43	Output	VCC33	Data output
	ENCIFOE2 (dsl_en)	J51 #42	Output	VCC33	Drive/receive control
HFDSL3	ENCIFDI3 (dsl_in)	J52 #44	Input	VCC1833_4	Data input
	ENCIFDO3 (dsl_out)	J52 #43	Output	VCC1833_4	Data output
	ENCIFOE3 (dsl_en)	J52 #42	Output	VCC1833_4	Drive/receive control
HFDSL4	ENCIFDI4 (dsl_in)	J49 #49	Input	VCC33	Data input
	ENCIFDO4 (dsl_out)	J49 #48	Output	VCC33	Data output
	ENCIFOE4 (dsl_en)	J49 #47	Output	VCC1833_3	Drive/receive control
HFDSL5	ENCIFDI5 (dsl_in)	J51 #49	Input	VCC1833_5	Data input
	ENCIFDO5 (dsl_out)	J51 #48	Output	VCC1833_5	Data output
	ENCIFOE5 (dsl_en)	J51 #47	Output	VCC1833_5	Drive/receive control
HFDSL6	ENCIFDI6 (dsl_in)	J50 #49	Input	VCC1833_4	Data input
	ENCIFDO6 (dsl_out)	J50 #48	Output	VCC33	Data output
	ENCIFOE6 (dsl_en)	J50 #47	Output	VCC33	Drive/receive control
HFDSL7	ENCIFDI7 (dsl_in)	J52 #49	Input	VCC1833_3	Data input
	ENCIFDO7 (dsl_out)	J52 #48	Output	VCC33	Data output
	ENCIFOE7 (dsl_en)	J52 #47	Output	VCC33	Drive/receive control

3.3 Procedures on Development Environments: CR52 version

3.3.1 Preparation before Executing the Sample Program

This sample program communicates with a PC. The USB connection terminal on the target board is J33.
Select the higher-numbered COM port that appears when the board is connected to the host PC.
The terminal software of the host PC is set as shown in the following table.

Function	Setting
Communication method	Asynchronous serial transmission/reception
Transmission/reception order	LSB first
Transfer rate	19200 bps
Character length	8 bits
Stop bit length	1 bit
Parity function	None
Hardware flow control	None

3.3.2 EWARM from IAR Systems

(1) Build Environment

IAR Embedded Workbench for Arm (EWARM)

Version 9.60.3 + patch (EWARM_Patch_for_RZT2N_rev1.0)

RENESAS FSP Smart Configurator (FSP SC) 2026-07

RENESAS Flexible Software Package (FSP) for RZ v4.2.0

(2) Debug Probe

IAR I-jet

Connect the JTAG debug probe to J31 and short between the J29 jumper pins.

(3) Build Procedure of the Sample Program

The build procedure for the sample program is as follows.

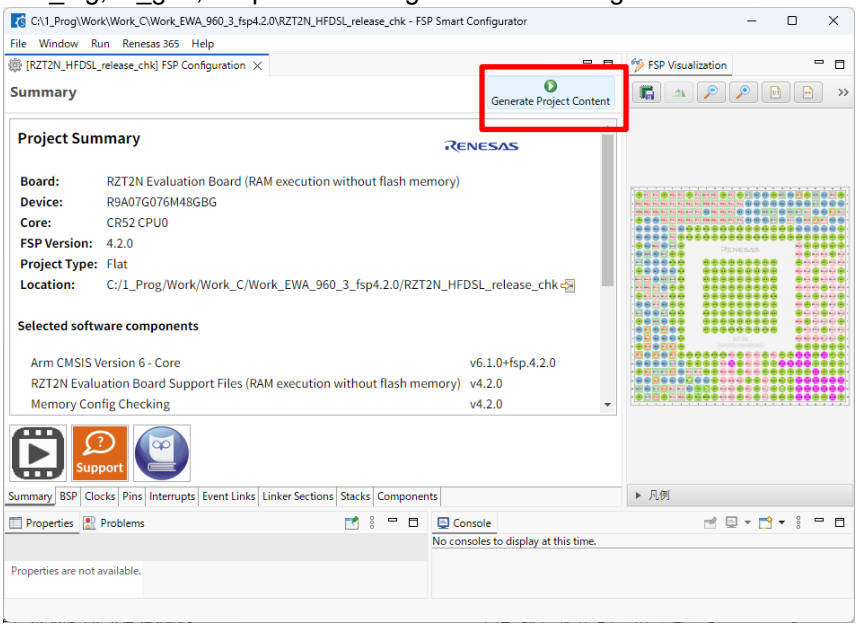
1. Extract RZ_T2N_CR52_hfdsl.zip and copy the extracted source files to the desired location.
2. Start EWARM.
3. Select [File] menu -> [Open Workspace].
4. Open the extracted source file RZ_T2N_hfdsl.eww.
5. Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE. *

Note: The following procedure adds an FSP Smart Configurator command to the EWARM IDE [Tools] menu. Select [Tools] menu -> [Tool Configuration] in the EWARM IDE. Select the [New] button, specify the strings shown in the following table for each field, and press [OK].

Field	String
Menu text	FSP Smart Configurator
Command	$RASC_EXE_PATH$
Argument	--compiler IAR configuration.xml
Initial directory	$PROJ_DIR$

The string in the command field is a variable that holds the path of the FSP Smart Configurator executable file, rasc.exe.
If the path written as RASC_EXE_PATH in the buildinfo.ipcf file does not match your rasc.exe installation path, edit buildinfo.ipcf accordingly.
You can also start the FSP Smart Configurator directly from the command prompt by specifying the folder where it is installed.

6 In the FSP Configuration pane of the FSP Smart Configurator, click Generate Project Content. The rz, rz_cfg, rz_gen, script and .settings folders will be generated.



7 When project generation is complete, close the FSP Smart Configurator.

8 Select [Rebuild All] from the [Project] menu of EWARM.
The file Debug\Exe\RZ_T2N_hfdsl.out will be generated.

(4) Sample Program Execution Procedure

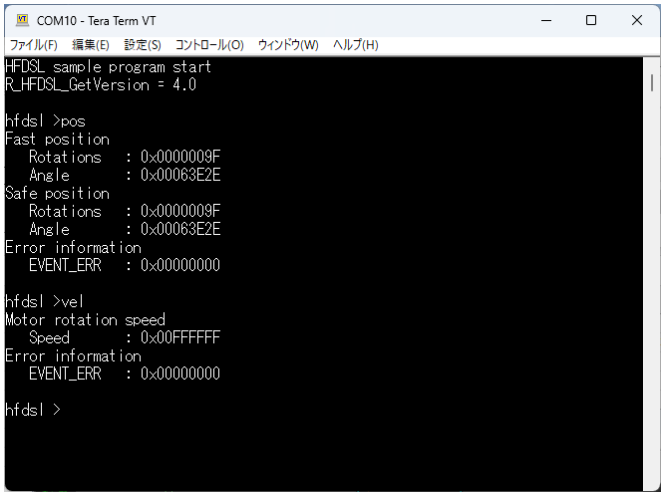
After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

1 Select [Project] menu -> [Download and Debug].

2 Select [Debug] menu -> [Execute].

(5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see “4.11.6 Console Commands” in the “RZ/T2N Group HIPERFACE DSL Sample Program” application note.



3.3.3 e² studio from Renesas Electronics

(1) Build Environment

RENESAS e² studio 2026-07

Toolchain version: GNU Arm Embedded 13.3.1.arm-13-24

RENESAS Flexible Software Package (FSP) for RZ v4.2.0

(2) Debug Probe

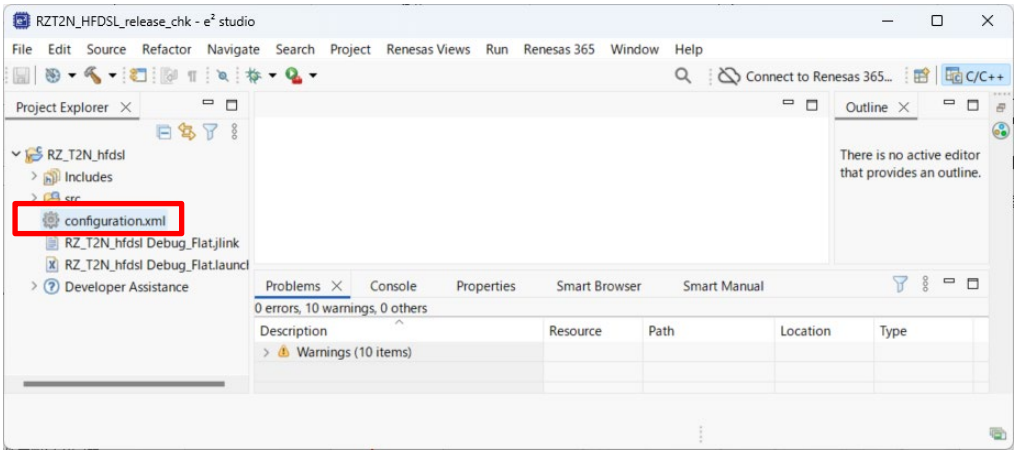
SEGGER J-Link™ v9.44

Connect the JTAG debug probe to J31 and short between the J29 jumper pins. If you use on-board debug probe (J-Link OB) on the target board, open between the J29 jumper pins and connect PC to J32.

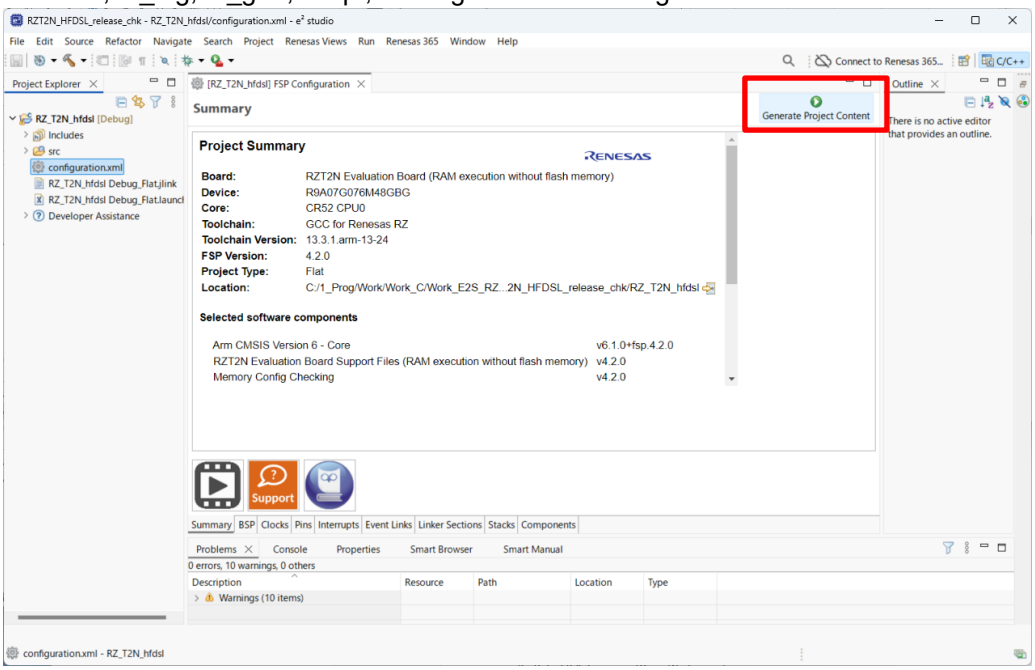
(3) Build Procedure of the Sample Program

The procedure for building the sample program is as follows.

1. Extract RZ_T2N_CR52_hfdsl.zip and copy the extracted source files to the desired location.
2. After launching e² studio and moving to the workspace, click the [File] menu-> [Import] and select General > Existing Projects into Workspace, and click [Next].
3. On the project import screen, select the folder where the sample program was extracted as the root directory.
4. Select a project, check Copy Project to Workspace, and click [Finish].
5. Double-click the configuration.xml in the Project Explorer pane of e² studio to open it.



6 Click Generate Project Content in the FSP Configuration pane of e² studio.
The rz, rz_cfg, rz_gen, script, .settings folders will be generated.



7 Select [Project] menu -> [Build All].
The file Debug\RZ_T2N_hfdsl.elf will be generated.

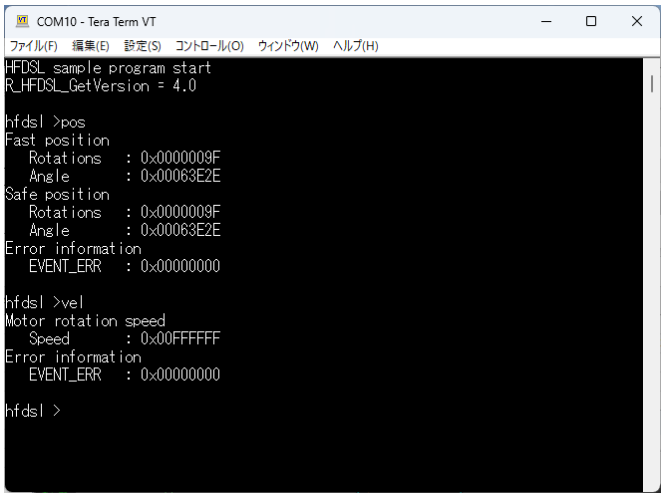
(4) Execution Procedure of the Sample Program

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

1 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging].
2 Click [Debug] to start downloading to internal RAM.
3 Click [Run] menu -> [Resume] to run the sample program.

(5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see “4.11.6 Console Commands” in the “RZ/T2N Group HIPERFACE DSL Sample Program” application note.



3.4 Procedures on Development Environments: CA55 version

3.4.1 Preparation before Executing the Sample Program

This sample program communicates with a PC. The USB connection terminal on the target board is J33.
Select the lower-numbered COM port that appears when the board is connected to the host PC.
The terminal software of the host PC is set as shown in the following table.

Function	Setting
Communication method	Asynchronous serial transmission/reception
Transmission/reception order	LSB first
Transfer rate	19200 bps
Character length	8 bits
Stop bit length	1 bit
Parity function	None
Hardware flow control	None

3.4.2 EWARM from IAR Systems

(1) Build Environment

IAR Embedded Workbench for Arm (EWARM)

Version 9.60.3 + patch (EWARM_Patch_for_RZT2N_rev1.0)

RENESAS FSP Smart Configurator (FSP SC) 2026-07

RENESAS Flexible Software Package (FSP) for RZ v4.2.0

(2) Debug Probe

IAR I-jet

Connect the JTAG debug probe to J31 and short between the J29 jumper pins.

(3) Build Procedure of the Sample Program

The build procedure of the sample program is as follows.

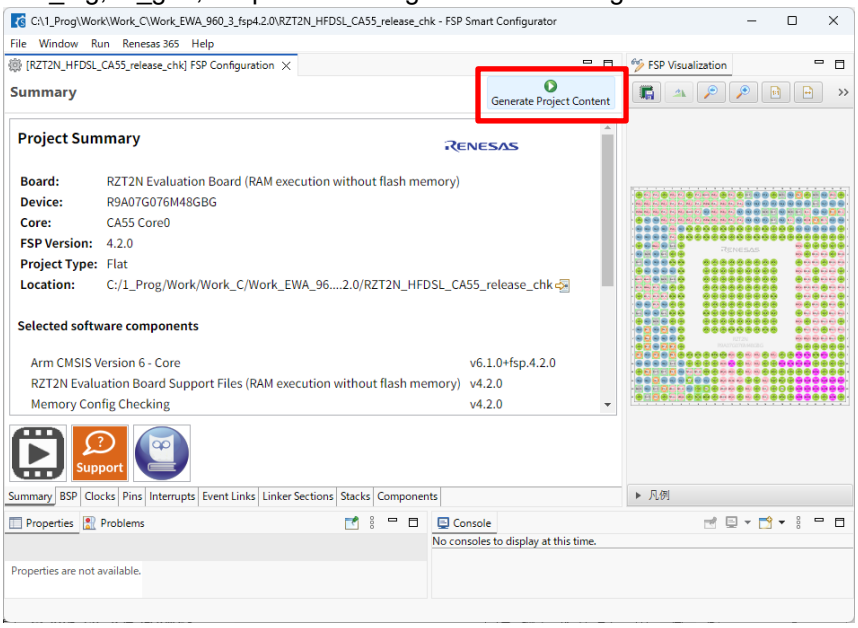
1. Extract RZ_T2N_CA55_hfdsl.zip and copy the extracted source files to the desired location.
2. Start EWARM.
3. Select [File] menu -> [Open Workspace].
4. Open the extracted source file RZ_T2N_CA55_0_hfdsl.eww.
5. Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE. *

Note: The following procedure adds an FSP Smart Configurator command to the EWARM IDE [Tools] menu. Select [Tools] menu -> [Tool Configuration] in the EWARM IDE. Select the [New] button, specify the strings shown in the following table for each field, and press [OK].

Field	String
Menu text	FSP Smart Configurator
Command	$RASC_EXE_PATH$
Argument	--compiler IAR configuration.xml
Initial directory	$PROJ_DIR$

The string in the command field is a variable that holds the path of the FSP Smart Configurator executable file, rasc.exe.
If the path written as RASC_EXE_PATH in the buildinfo.ipcf file does not match your rasc.exe installation path, edit buildinfo.ipcf accordingly.
You can also start the FSP Smart Configurator directly from the command prompt by specifying the folder where it is installed.

6 In the FSP Configuration pane of the FSP Smart Configurator, click Generate Project Content. The rz, rz_cfg, rz_gen, script and .settings folders will be generated.



7 When project generation is complete, close the FSP Smart Configurator.

8 Select [Rebuild All] from the [Project] menu of EWARM.
The file Debug\Exe\RZ_T2N_CA55_0_hfdsl.out will be generated.

(4) Sample Program Execution Procedure

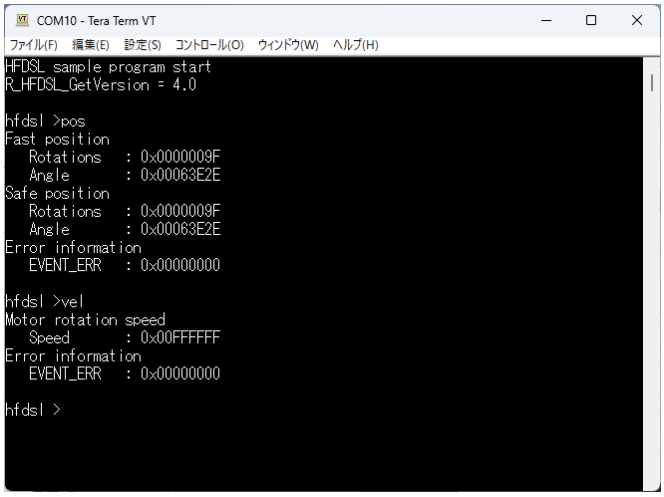
After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

1 Select [Project] menu -> [Download and Debug].

2 Select [Debug] menu -> [Execute].

(5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see “4.11.6 Console Commands” in the “RZ/T2N Group HIPERFACE DSL Sample Program” application note.



3.4.3 e² studio from Renesas Electronics

(1) Build Environment

RENESAS e² studio 2026-07

Toolchain version: GCC Arm A-Profile (AArch64 bare-metal) 13.2.1.20231009

RENESAS Flexible Software Package (FSP) for RZ v4.2.0

(2) Debug Probe

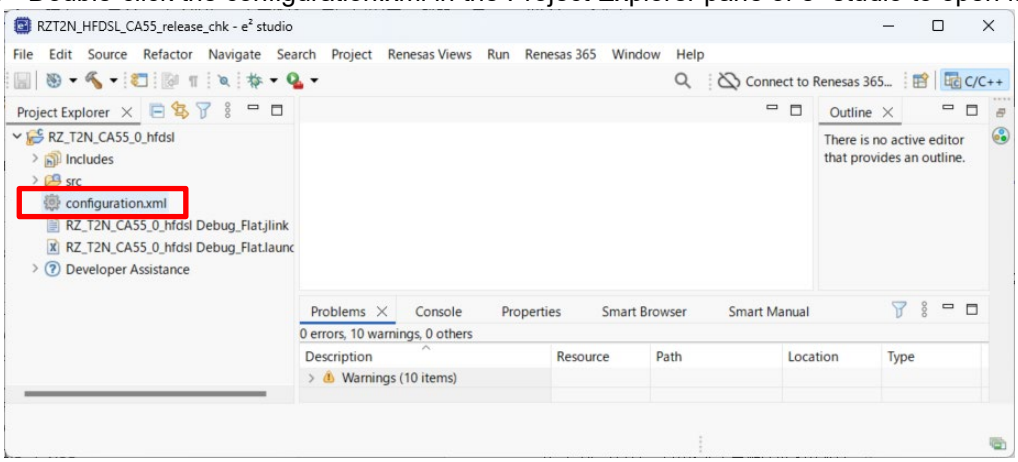
SEGGER J-Link™ v9.44

Connect the JTAG debug probe to J31 and short between the J29 jumper pins. If you use on-board debug probe (J-Link OB) on the target board, open between the J29 jumper pins and connect PC to J32.

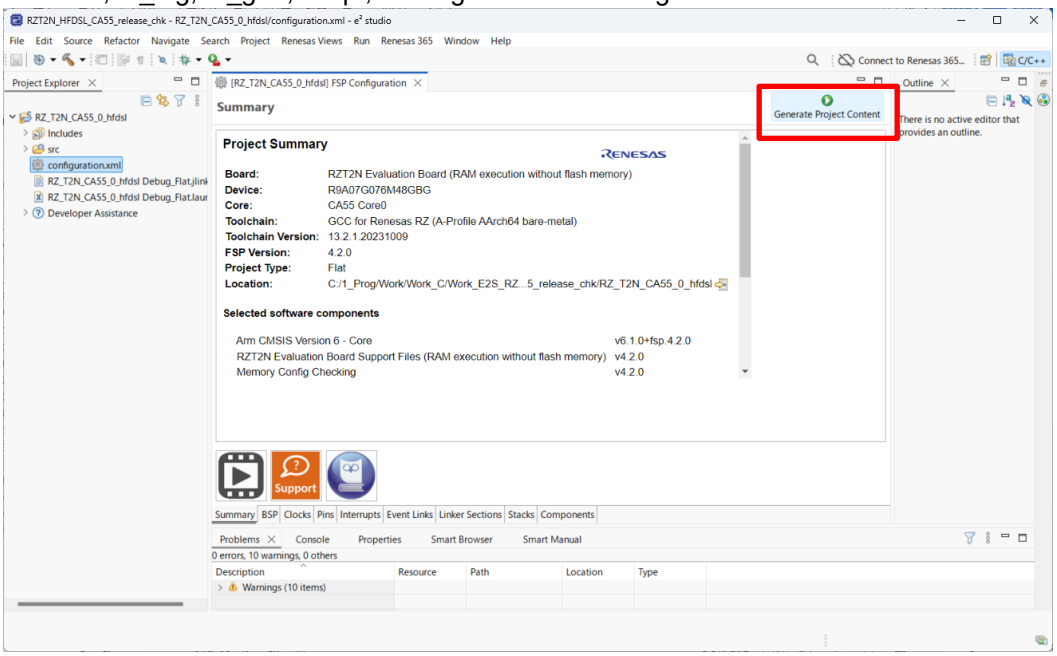
(3) Build Procedure of the Sample Program

The procedure for building the sample program is as follows.

1 Extract RZ_T2N_CA55_hfdsl.zip and copy the extracted source files to the desired location.
2 After launching e² studio and moving to the workspace, click the [File] menu -> [Import] and select General > Existing Projects into Workspace, and click [Next].
3 On the project import screen, select the folder where the sample program was extracted as the root directory.
4 Select a project, check Copy Project to Workspace, and click [Finish].
5 Double-click the configuration.xml in the Project Explorer pane of e² studio to open it.



6 Click Generate Project Content in the FSP Configuration pane of e² studio.
The rz, rz_cfg, rz_gen, script, .settings folders will be generated.



7 Select [Project] menu -> [Build All].
The file Debug\RZ_T2N_CA55_0_hfdsl.elf will be generated.

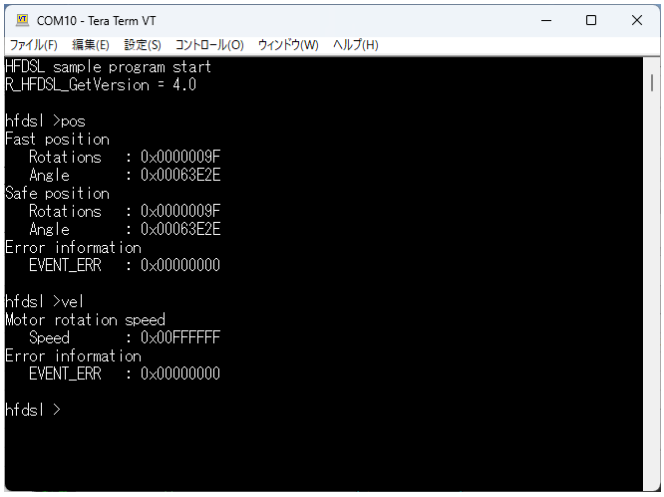
(4) Execution Procedure of the Sample Program

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

1 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging].
2 Click [Debug] to start downloading to internal RAM.
3 Click [Run] menu -> [Resume] to run the sample program.

(5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see “4.11.6 Console Commands” in the “RZ/T2N Group HIPERFACE DSL Sample Program” application note.



Revision History

Rev.	Date	Description	
		Page	Summary
0.50	Jul 22, 25	-	First edition issued
0.80	Mar 27, 26	2, 3	Update revisions of the application note and the release note. Update sample program version to 0.8. (Support FSP v3.1.0-t2n.alpha. Change device to 537-pin version.)
		4	Update memory size information.
		5	Update setting of target board for using 537-pin version.
		6 to 13	Update build environment for FSP v3.1.0-t2n.alpha. Figures are replaced.
4.00	Nov 04, 26	2, 3	Update revisions of the application note and the release note. Update sample program version to 4.0. (Support FSP v4.2.0.)
		3	Add SBOM information.
		4	Update memory size information.
		5	Correct voltage domain on channel 4.
		6 to 13	Update build environment for FSP v4.2.0. Figures are replaced.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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