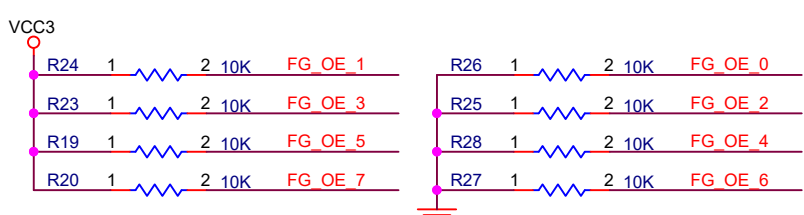
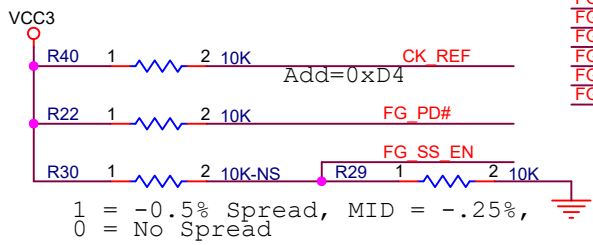
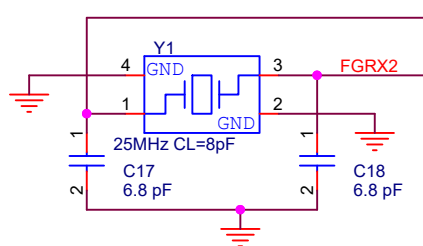
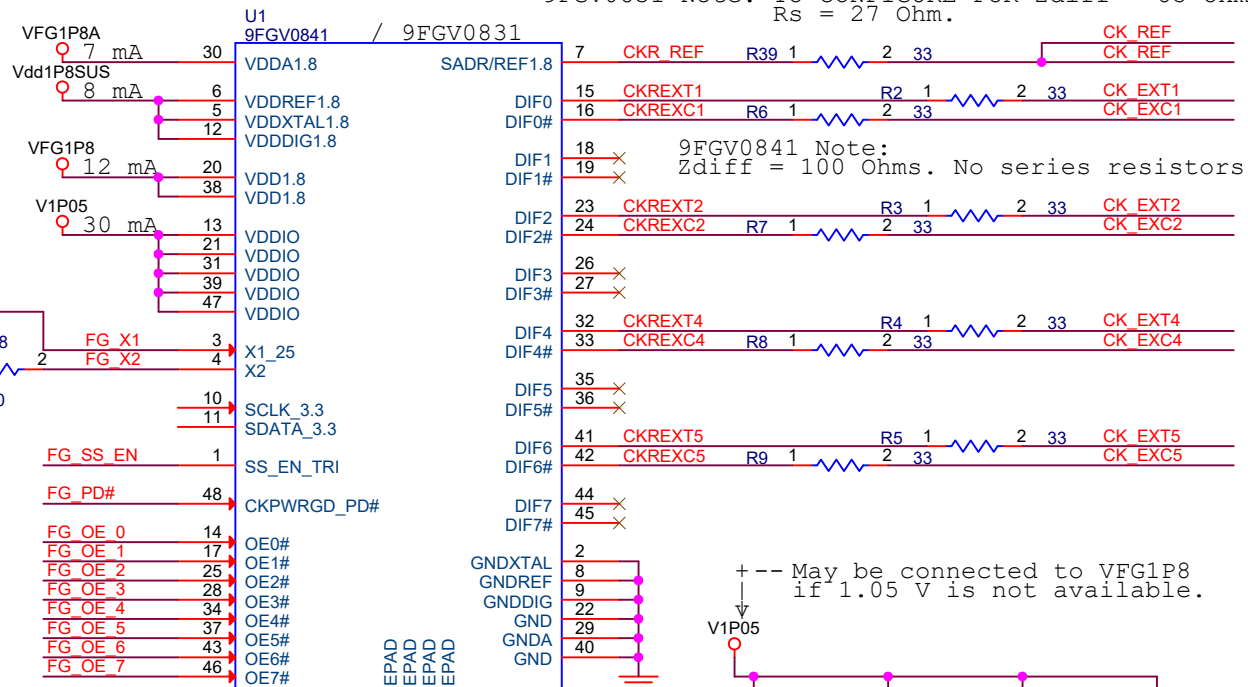


Layout notes.

1. Separate Xout and Xin in traces by 3 x the trace width.
2. Do not share crystal load capacitor ground via with other components.
3. Route power from bead through bulk capacitor pad then through capacitor pad then to clock chip Vdd pad.
4. Do not share ground vias. One ground pin one ground via.

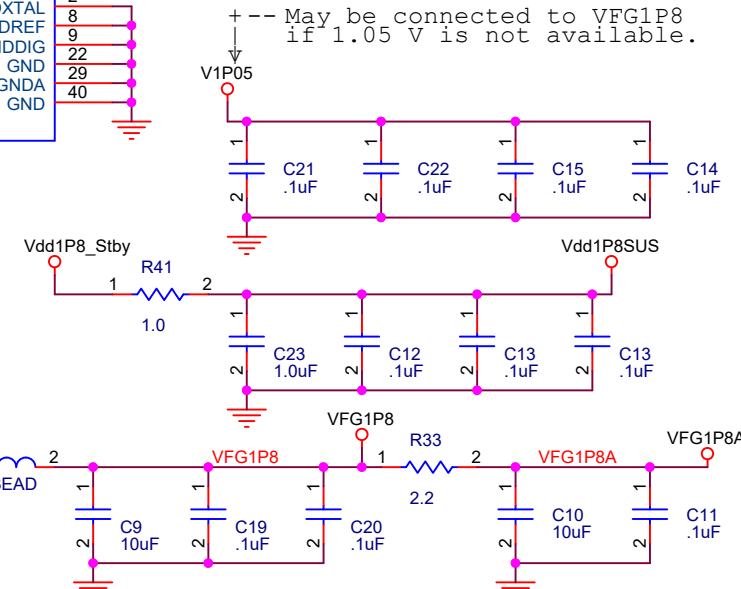
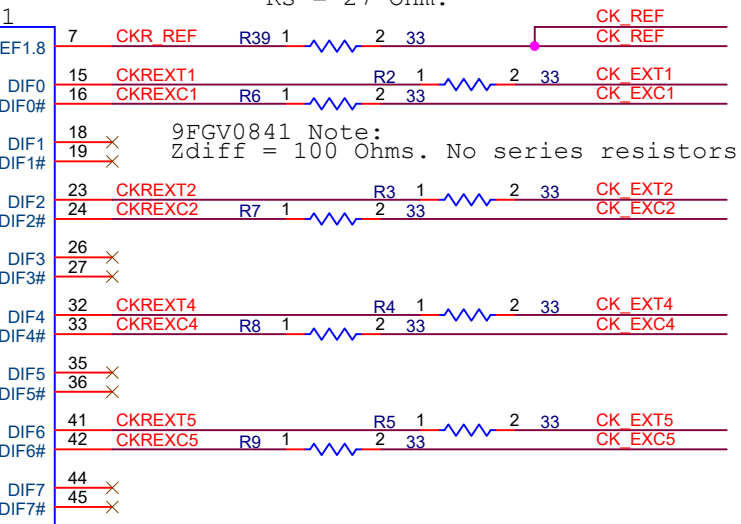
9FGV0831 Note: TO CONFIGURE FOR Zdiff = 85 Ohms
Rs = 27 Ohm.



NOTE: FERRITE BEADS FB1 =

Manufacturer	Part Number	Z@100MHz	PkgSz	DC res.	Current (Ma)
muRata	BLM21AG601SN1	600	0805	0.30	600
TDK	MMZ2012S601A	600	0805	0.30	600
STEWART	HZ0805E601R	600	0805	0.30	600
AssocCmpTch	CBG0805-600-50	600	0805	0.30	600

Manufacturer	Part Number	Z@100MHz	PkgSz	DC res.	Current (Ma)
muRata	BLM18AG601SN1	600	0603	0.50	200
muRata	BLM18BD601SN1_PB	600	0603	0.65	200
Ceratech	HB-1T1608-601	600	0603	0.50	200
TDK	MMZ1608R301A	300	0603	0.20	500



Integrated Device Technology
San Jose, CA

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