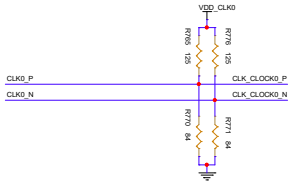
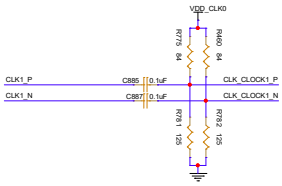
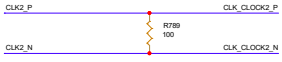
Input Termination Example: Put it close to 8A34001



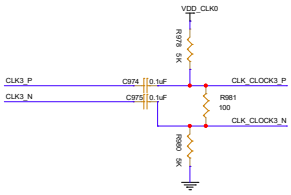
LVPECL DC-Coupled
Note: if the driver is the 8A34x chip, do not use this termination scheme.
Use the LVDS terminations scheme.



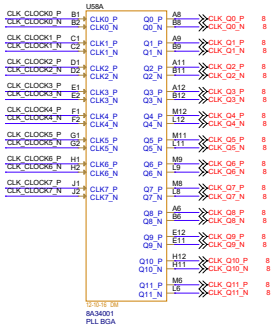
LVPECL AC-Coupled



LVDS DC-Coupled



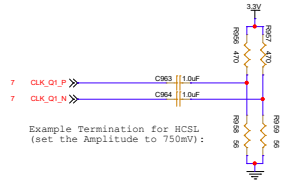
LVDS AC-Coupled



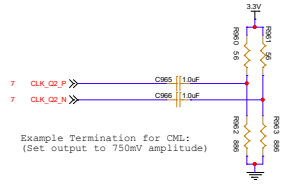
The above input termination of CLK0~CLK3 can be used for CLK4~CLK7.

Output Termination Example: Put it close to the receiver side

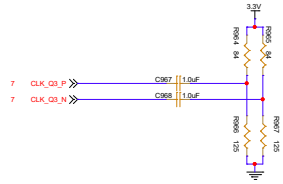
Termination scheme for dc-coupled differential outputs.
This should be used for the standard selections provided in the GUI, such as LVPECL (2.5V/3.3V) or LVDS



Example Termination for HCSL
(set the Amplitude to 750mV):



Example Termination for CML:
(Set output to 750mV amplitude)



Example Termination for ac-coupling to a 3.3V LVPECL receiver.
Note that no pull-downs are used at the driver.

The above output termination of Q0~Q3 can be used for Q4~Q11.

Title	The Simple Ref Design of the Clock Matrix	
Size C	Document Number 8A34001: PLL Inport and Output Clocks	Rev 1
Date: Thursday, July 27, 2023	Sheet 2 of 3	