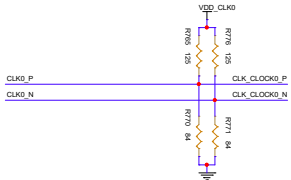
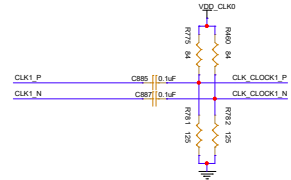


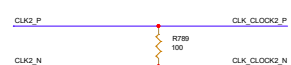
Input Termination Example: Put it close to 8A34001



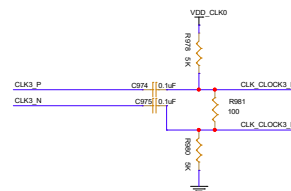
LVPECL DC-Coupled
Note: if the driver is the 8A34x chip, do not use this termination scheme.
Use the LVDS termination scheme.



LVPECL AC-Coupled



LVDS DC-Coupled



LVDS AC-Coupled

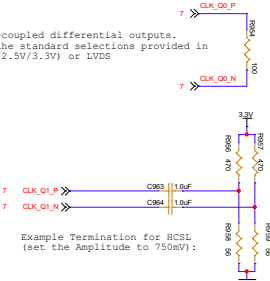
The above input termination of CLK0-CLK3 can be used for CLK4-CLK7.

155A			
CLK_CLOCK0_P	B1	CLK0_P	Q0_P
CLK_CLOCK0_N	B2	CLK0_N	Q0_N
CLK_CLOCK1_P	C1	CLK1_P	Q1_P
CLK_CLOCK1_N	C2	CLK1_N	Q1_N
CLK_CLOCK2_P	D1	CLK2_P	Q2_P
CLK_CLOCK2_N	D2	CLK2_N	Q2_N
CLK_CLOCK3_P	E1	CLK3_P	Q3_P
CLK_CLOCK3_N	E2	CLK3_N	Q3_N
CLK_CLOCK4_P	F1	CLK4_P	Q4_P
CLK_CLOCK4_N	F2	CLK4_N	Q4_N
CLK_CLOCK5_P	G1	CLK5_P	Q5_P
CLK_CLOCK5_N	G2	CLK5_N	Q5_N
CLK_CLOCK6_P	H1	CLK6_P	Q6_P
CLK_CLOCK6_N	H2	CLK6_N	Q6_N
CLK_CLOCK7_P	J1	CLK7_P	Q7_P
CLK_CLOCK7_N	J2	CLK7_N	Q7_N
		Q8_P	A6
		Q8_N	B6
		Q9_P	C12
		Q9_N	E11
		Q10_P	H12
		Q10_N	J11
		Q11_P	L8
		Q11_N	M8

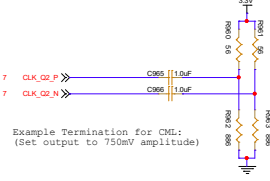
155B 155C
8A34001
PLL BGA

Output Termination Example: Put it close to the receiver side

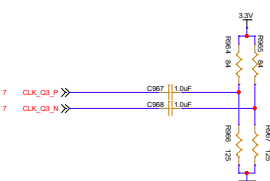
Termination scheme for dc-coupled differential outputs.
This should be used for the standard selections provided in
the GUI, such as LVPECL (2.5V/3.3V) or LVDS



Example Termination for HCSL
(set the Amplitude to 750mV):



Example Termination for CML:
(Set output to 750mV amplitude)



Example Termination for ac-coupling to a 3.3V LVPECL receiver.
Note that no pull-downs are used at the driver.

The above output termination of Q0-Q3 can be used for Q4-Q11.