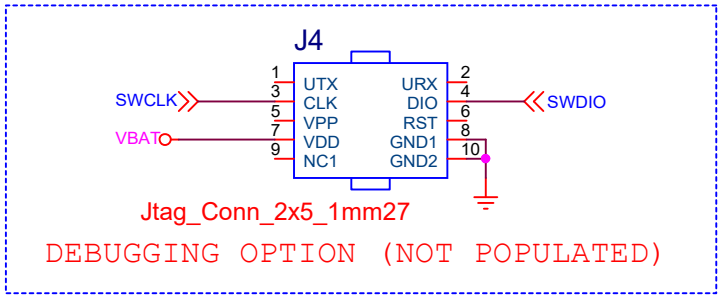
DA14531 Pro Development Kit

Design Name	d2632-db-qfn24_vF2
Ref. Number	376-04-F
Version	F1.2
Date	August 09, 2019
Designer	Kalliopi Liantinioti

History Table

Version	Date	Comments
A00	08 / Aug / 2018	Draft Release
	09 / Aug / 2018	Added option for hardware reset (P0_0 - R30) Added CIB debugging option (J4) Corrected mismatch in function notes (purple names) for MISO/SCLK
A1.0	17 / Aug / 2018	Released to manufacturing
		Added options for SWDIO (R31, R32) Default option for SWDIO set to P0_10 (R31) Version number set to C (matching the layout version)
C1.0	17 / Aug / 2018	Released to manufacturing
		Set default configuration: SPI bus and JTAG: • R1 to R12 changed to 36 Ohms instead of 100 ohms • Y2 (32.768KHz - NP) type changed to SC20S-7PF20PPM • R23 R24 R25 R26 R27 R28 R29 set as not populated
C1.1	30 / Nov / 2018	
		Set JTAG SWDIO on P0_5 (not on P0_10 as in datasheet) • R31 = No pop • R15 = 0 Added Matching circuit Z1, Z3 • Z3 = 4.6nH / LQW15AN4N6B80D • Z1 = 1pF
C1.2	10 / Jan / 2019	
		BOM modifications for DCDC power optimization: • Changed L1 from BRL1608T2R2M to CBMF1608T2R2M • Changed C1, C2 from 10uF to 2.2uF Set JTAG SWDIO on P0_10 (as in datasheet) • R31 = 0 • R15 = No Pop
C1.3	01 / Feb / 2019	
D1.0	04 / Feb / 2019	Changed L1 from CBMF1608T2R2M to DFE201610E-2R2M
E1.0	15 / May / 2019	Changed C2 to 4.7uF Added NP resistor R33 Layout modification: Removed restangle on top legend around U1
F1.0	03/ July / 2019	Added placeholder for pi-shaped CLC filter (Z1, Z2, Z3) Changed RF matching components to : Z4, Z5 , Z6 Added placehold for decoupling capacitors: C6, C7 Added resistors R34, R35
F1.1	10/ July / 2019	Changed C2 from 4.7uF to 10uF
F1.2	09 / Aug / 2019	Changed R11 to N.P.



Configuration note

NOTE box

Changes in this Version.

TP11 FIDUCIAL

TP12 FIDUCIAL

GND

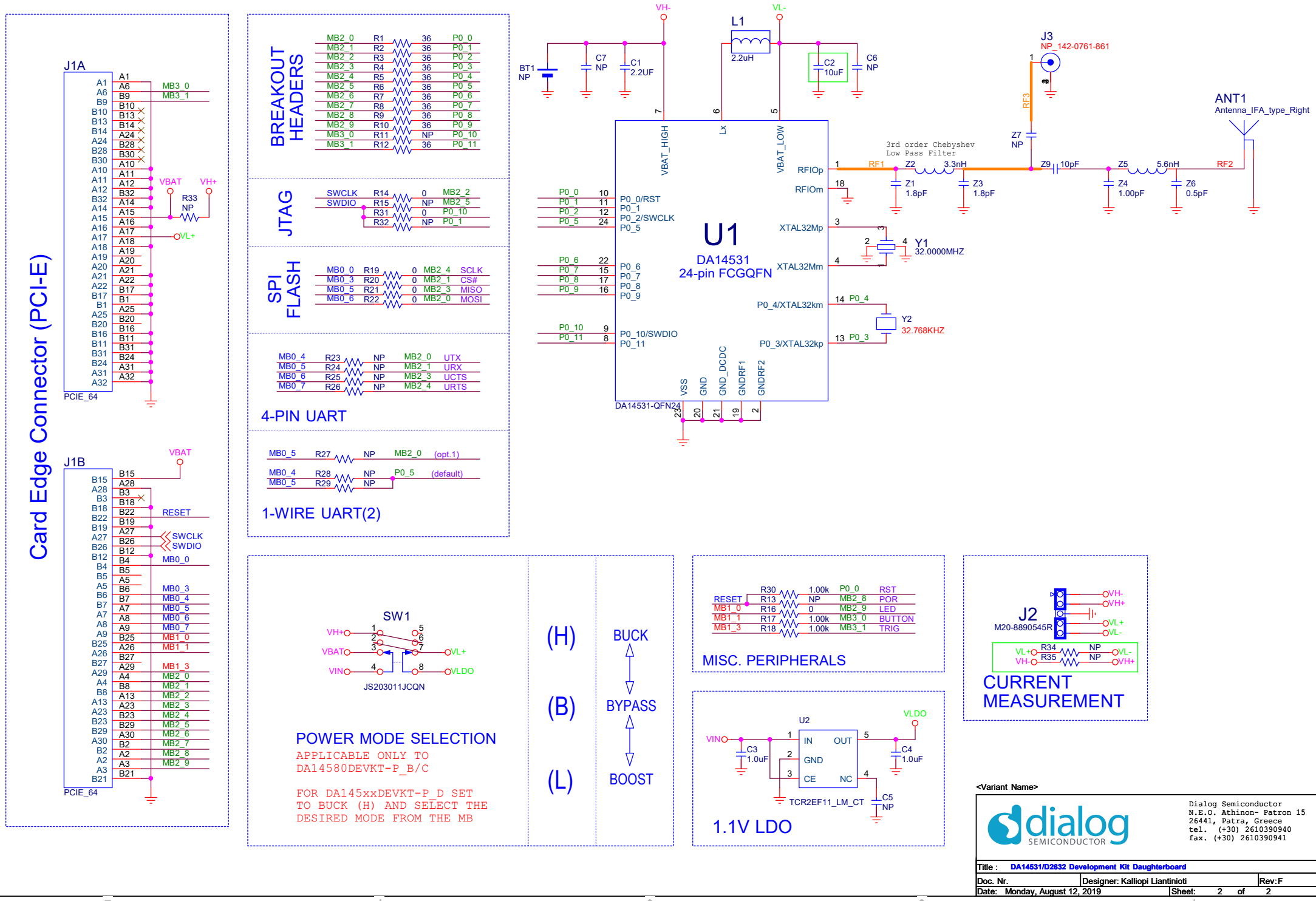
T1

Label_Dialog_L6008

<Variant Name>

Dialog Semiconductor
N.E.O. Athinon- Patron 15
26441, Patra, Greece
tel. (+30) 2610390940
fax. (+30) 2610390941

Title :	DA14531/D2632 Development Kit Daughterboard		
Doc. Nr.	376-04-F	Designer: Kalliopi Liantinioti	Rev:F
Date:	Monday, August 12, 2019	Sheet: 1 of 2	


Card Edge Connector (PCI-E)
J1A
PCIE_64
VBAT
VH+
R33
NP
VL+
J1B
PCIE_64
VBAT
RESET
SWCLK
SWDIO
MB0_0
MB0_3
MB0_4
MB0_5
MB0_6
MB0_7
MB1_0
MB1_1
MB1_3
MB2_0
MB2_1
MB2_2
MB2_3
MB2_4
MB2_5
MB2_6
MB2_7
MB2_8
MB2_9
BREAKOUT HEADERS
JTAG
SPI FLASH
4-PIN UART
1-WIRE UART(2)
(opt.1)
(default)
VH-
VL-
L1
2.2uH
BT1
NP
C7
NP
C1
2.2UF
C2
10uF
C6
NP
U1
DA14531
24-pin FCGQFN
DA14531-QFN24
VBAT_HIGH
Lx
VBAT_LOW
RFIOp
RFIOm
XTAL32Mp
XTAL32Mm
P0_4/XTAL32km
P0_3/XTAL32kp
P0_0/RST
P0_1
P0_2/SWCLK
P0_5
P0_6
P0_7
P0_8
P0_9
P0_10/SWDIO
P0_11
VSS
GND
GND_DCDC
GNDRF1
GNDRF2
Y1
32.0000MHZ
Y2
32.768KHZ
3rd order Chebyshev
Low Pass Filter
RF1
Z1
1.8pF
Z2
3.3nH
Z3
1.8pF
J3
NP_142-0761-861
RF3
Z7
NP
Z9
10pF
Z5
5.6nH
RF2
Z4
1.00pF
Z6
0.5pF
ANT1
Antenna_IFA_type_Right
SW1
JS203011JCQN
VH+
VBAT
VIN
VL+
VLDO
POWER MODE SELECTION
APPLICABLE ONLY TO
DA14580DEVKT-P_B/C
FOR DA145xxDEVKT-P_D SET
TO BUCK (H) AND SELECT THE
DESIRED MODE FROM THE MB
(H)
(B)
(L)
BUCK
BYPASS
BOOST
MISC. PERIPHERALS
RESET
MB1_0
MB1_1
MB1_3
RST
POR
LED
BUTTON
TRIG
1.00k
U2
TCR2EF11_LM_CT
IN
OUT
GND
CE
NC
C3
1.0uF
C4
1.0uF
C5
NP
1.1V LDO
J2
M20-8890545R
CURRENT MEASUREMENT
R34
R35
<Variant Name>
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