



	PROJECT
	CAITLIN PERF. DB
	DRAWING NUMBER 169-02-A_C1
LAYER	TOP SIDE TRACK







PROJECT

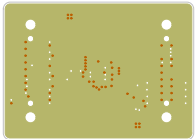
CAITLIN PERF DB


DRAWING NUMBER

169-02-A_C2

LAYER

INNER LAYER 2





PROJECT

CAITLIN PERF. DB

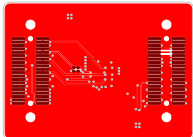
DRAWING NUMBER


169-02-A_C3

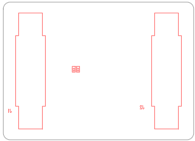


LAYER



INNER LAYER 3





	PROJECT CAITLIN PERF. DB
DRAWING NUMBER 169-02-A_C4	
LAYER	BOTTOM SIDE TRACK



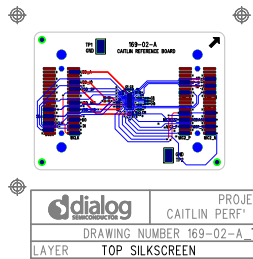


PROJECT

CAITLIN PERF DB

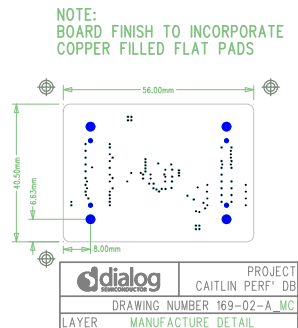
DRAWING NUMBER 169-02-A

LAYER



	PROJECT
	CAITLIN PERF. DB
DRAWING NUMBER 169-02-A TS	
LAYER	TOP SILKSCREEN

IF IN DOUBT ASK!



DRILL DETAIL NOTES	
ALL PLATED HOLES ARE FINISHED SIZES WITH $\pm 0.075\text{mm}$ TOLERANCE	
ALL NON-PLATED HOLES ARE FINISHED SIZES WITH $\pm 0.050\text{mm}$ TOLERANCE	
ALL VIAS ARE DRILLED SIZES WITH ± 0 -DRILL TOLERANCE	
TOTAL PLATED HOLE QTY	105
TOTAL NON-PLATED HOLE QTY	8



COMPANY CONFIDENTIAL

TOLERANCES UNLESS OTHERWISE STATED 0 PLACE DECIMALS +/- 1 1 PLACE DECIMALS +/- 0.5 2 PLACE DECIMALS +/- 0.1	DRAWN BY BL	DATE 29/11/12	DIALOG SEMICONDUCTOR UK LTD 2 MUltrees WALK EDINBURGH EH1 3DQ	© COPYRIGHT 2012	
	CHK'D BY CM	DATE 29/11/12		TITLE MANUFACTURE DETAIL	DRAWING NUMBER 169-02-A

PREFERRED PANEL DRAWING REQUIREMENTS

REFER TO THE PANEL DRAWING IF SUPPLIED OTHERWISE USE DETAILS BELOW

PRINTED CIRCUIT BOARDS THAT REQUIRE FANCLINATION

01 ANY PCB THAT DOES NOT HAVE A 5mm CLEARANCE FROM PCB EDGE TO COPPER/COMPONENTS ALONG THE LONGEST PARALLEL EDGES

02 ANY 'ODD' SHAPE PCB e.g. ROUND

PANEL SIZE, WASTE EDGE (BORDER) AND WEBBING

01 PREFERRED PANEL SIZE TO BE 300mm X 230mm (MAXIMUM 450mm SQUARE)

02 PANEL BORDER TO BE 10mm ON ALL SIDES, FULLY CROSS HATCHED IN COPPER ON BOTH SIDES

03 BOARD EDGE TO BOARD EDGE INTERNAL WEBBING TO BE 10mm

TOOLING HOLES

01 ADD 3 TOOLING HOLES 2.5mm \pm 0.05 DIA. TO PANEL BORDER 5mm FROM BORDER EDGE

FIDUCIALS

01 ADD 3 FIDUCIALS ON BOTH SIDES (1mm Dia./2mm Dia. CLEARANCE) 5mm FROM PANEL EDGE RATBITES (FOR REFERENCE SEE ROUTING DETAIL BELOW)

02 ADD RATBITES IN SAFE AREAS AWAY FROM TRACKS, TOOLING HOLES, SM PADS, VIAS, TEST PADS (GROUND PLANES, VITAL SILKSREEN, THROUGH HOLES, OVERHANGING COMPONENTS ETC.

03 USE LOCATIONS SHOWN BY \pm F PRESENT

04 THERE MUST BE SUFFICIENT RATBITES TO ENSURE PCB STABILITY

05 THE SPACING BETWEEN RATBITES SHOULD BE BETWEEN 40mm TO 50mm

PREFERRED ROUTING / V-SCORING REQUIREMENTS

ROUTING

REQUIRED

01 USE A 2.40mm (\pm 0.10mm) ROUT

The diagram illustrates the required dimensions for routing and V-scoring. It shows a break-off strip with a width of 2.40mm and a circuit board with a thickness of 0.50mm. Key dimensions include a 1.50mm clearance from the edge, a 3.00mm clearance for the full radius (2 POS'NS), and a 1.00mm clearance for the ratbite (0.50mm) drilled hole (3 OFF). The V-scoring angle is indicated as 30°.

V-SCORING

NOT REQUIRED

WHEN V-SCORING IS APPLIED TO THE BOARD AS A METHOD OF REMOVING THE BREAK-OFF STRIPS THE FOLLOWING RULES ARE TO BE APPLIED

01 SOLDER MASK TO EDGE CLEARANCE = 0.50mm (20thou)





02 COPPER TO EDGE CLEARANCE (ON ALL LAYERS) = 1.00mm (40thou)

03 SCORE ANGLE = 30 deg

04 REMAINING WEB AFTER SCORING IS AS ONE THIRD OF THE PCB NOMINAL THICKNESS

The diagram shows the V-scoring process with a 30° angle and a web dimension (WEB = (1/3 Tpcb)). The V-score is shown as a V-shape in the board, with the remaining web dimension indicated.

[illegible]

LAYER/ LAYER TYPE	BOARD STACK	COPPER WEIGHT
01 MIXED		305g/m
02 GROUND		152g/m
03 GROUND		152g/m
04 MIXED		305g/m