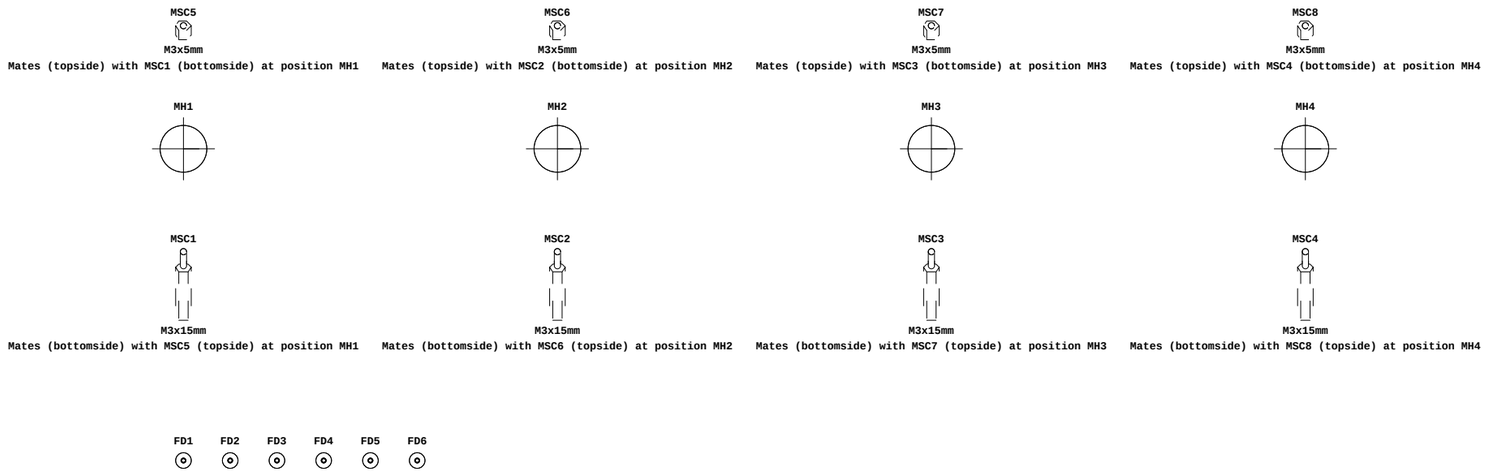
REVISION TABLE

REV.	DATE	ENGINEER	NOTES
A1	05/07/2021	XB	Manufactured version.

MECHANICAL PARTS



SCHEMATIC TEMPLATE REV.xDxD_V8 (10-07-2019)

DESIGNED BY: CH, XB

REVIEWED BY: SK

CONFIDENTIAL INFORMATION

SIZE A3L

TITLE: DA913x Customer Eval Board

VARIANT: Master Sch no Var defined

SAVED DATE: 05/07/2021:11:21

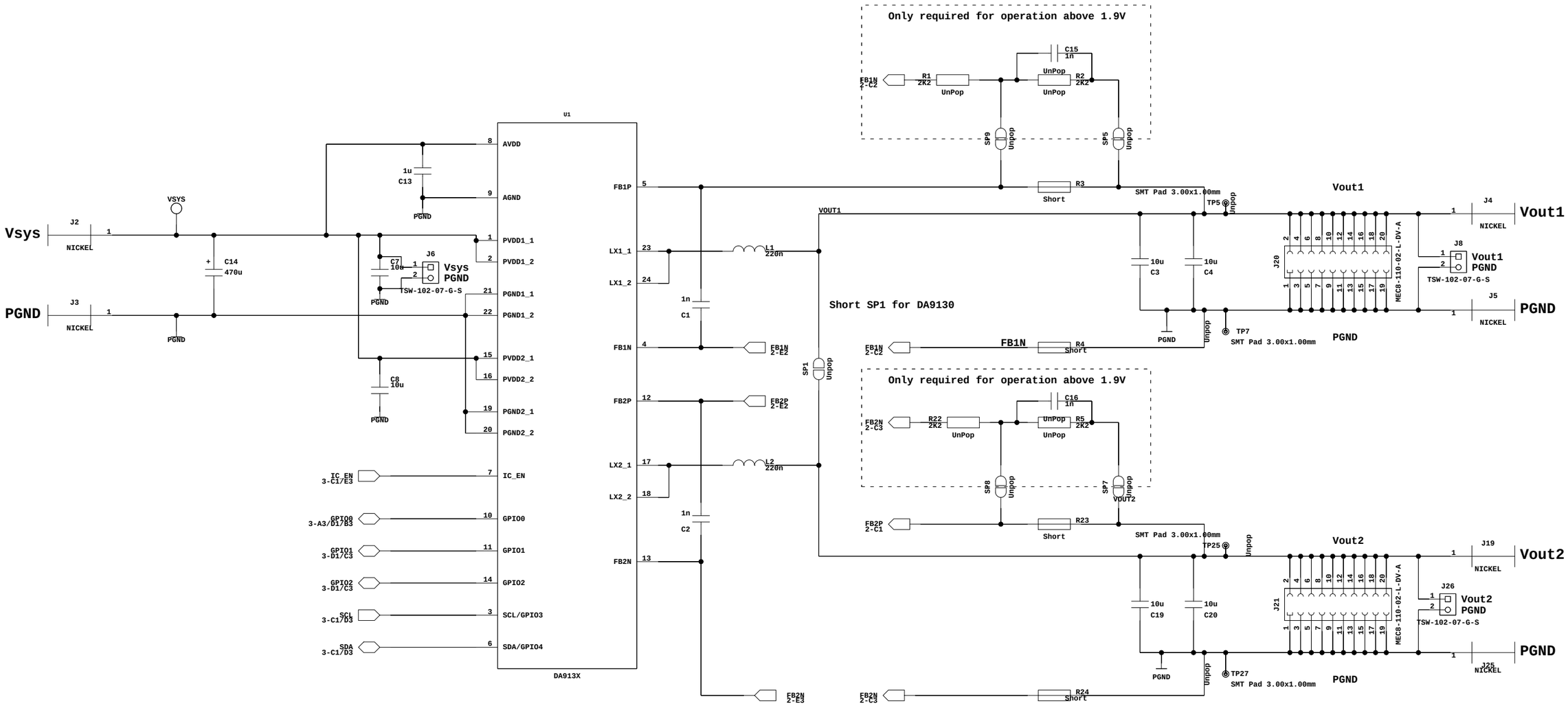
REVIEWED DATE:

DRAWING No: DA913X-30-A 1 (BOARD No. | Sch Rev | Variant No. | Var Rev)

SHEET NAME: Revision and Mechanical

PAGE: 1 of 3

dialog SEMICONDUCTOR



Comments:
- 70um copper planes top/bottom
- Fill copper areas top/bottom
- Place 20 thermal vias under U1 (0.2mm, 1mm Pitch)
- Place 60 thermal vias around U1 (0.2mm, 10mm Pitch)
- 2mm clearance between J15 and the board edge

Specific to DA9130:
- Short SP1
- Open R25 and R24
- Do not populate C2

JMP1 D3082-05 PGND
JMP2 D3082-05 PGND
JMP3 D3082-05 PGND
JMP4 D3082-05 PGND

SCHEMATIC TEMPLATE REV.xDxD_V8 (10-07-2019)

DESIGNED BY: CH, XB	CONFIDENTIAL INFORMATION	SIZE A3L	TITLE: DA913x Customer Eval Board
REVIEWED BY: SK	SAVED DATE: 03/12/2021:15:12		VARIANT: Master Sch no Var defined
	REVIEWED DATE:		DRAWING No: DA913X-30-A 1 (BOARD No. / Sch Rev / Variant No. / Var Rev)
			SHEET NAME: DA913x

dialog SEMICONDUCTOR

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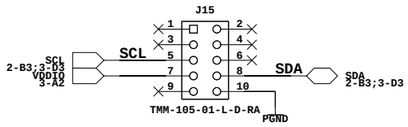
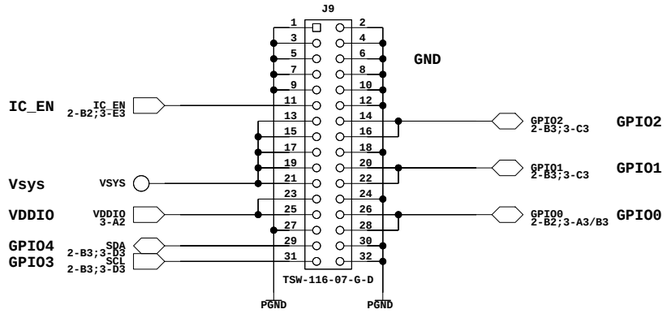
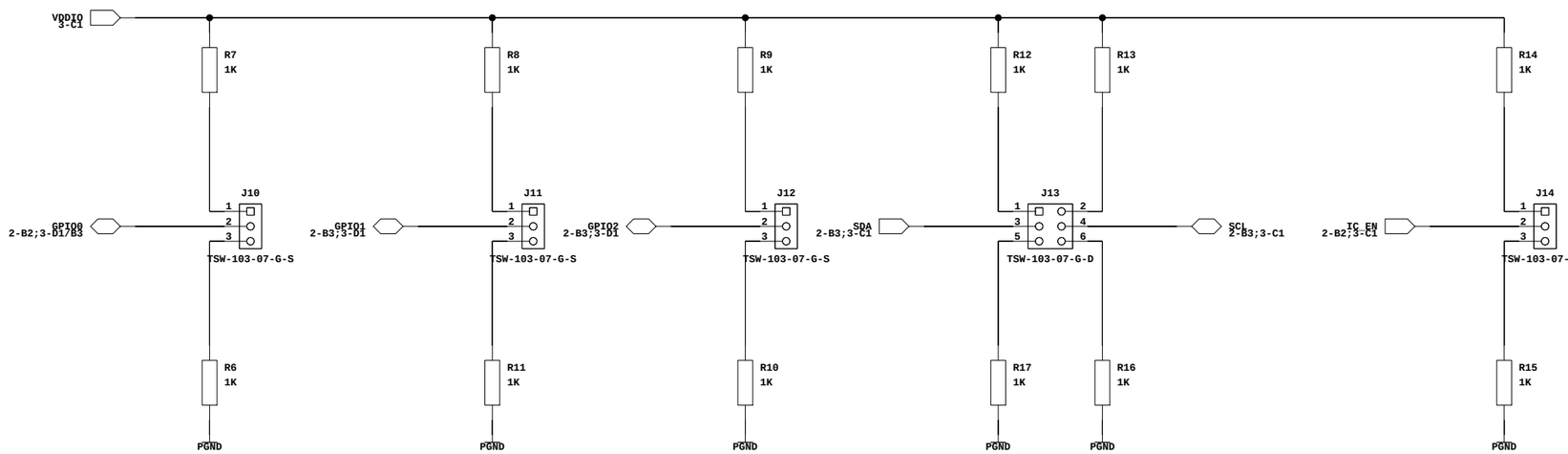
Place J15 2mm from the board edge







SCHEMATIC TEMPLATE REV.xDxD_V8 (10-07-2019)

DESIGNED BY: CH, XB	CONFIDENTIAL INFORMATION	SIZE A3L	TITLE: DA913x Customer Eval Board
REVIEWED BY: SK	SAVED DATE: 25/06/2021:16:59		VARIANT: Master Sch no Var defined
	REVIEWED DATE:		DRAWING No: DA913X-30-A 1 (BOARD No. / Sch Rev / Variant No. / Var Rev)
			SHEET NAME: GPIOs
			PAGE: 3 of 3

dialog SEMICONDUCTOR