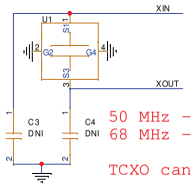
CRYSTAL INPUT



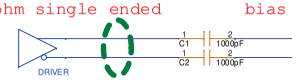
50 MHz - Synth
68 MHz - JA

TCXO can be used

CLKIN0/1

100 ohm differential trace
or two 50 ohm single ended

If AC coupling, VC8 internal bias can be enabled.

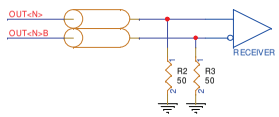


VC8 has built in termination for LVCMOS and HCSL.

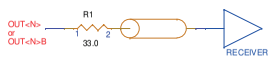
Refer to AN-808, 828, 845, 846. Use suggested components as needed.

LP-HCSL

Pull down resistors are optional
(double termination)

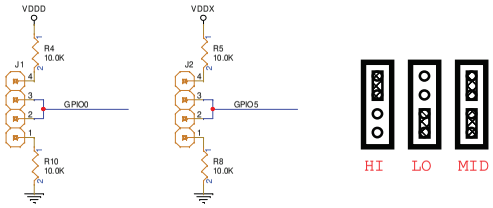


LVCMOS



Adjust R1 to better
match impedance

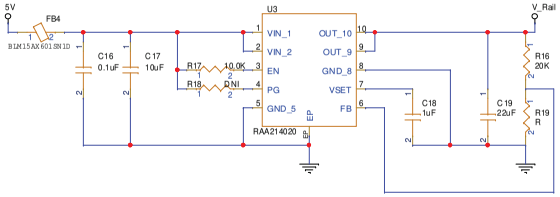
CONFIGURATION LATCHING



GPI/GPIO/PWRGD_PDB

OUT10 and OUT11 can also be used as GPIO1-4
PWRGD_PDB needs to be held hi

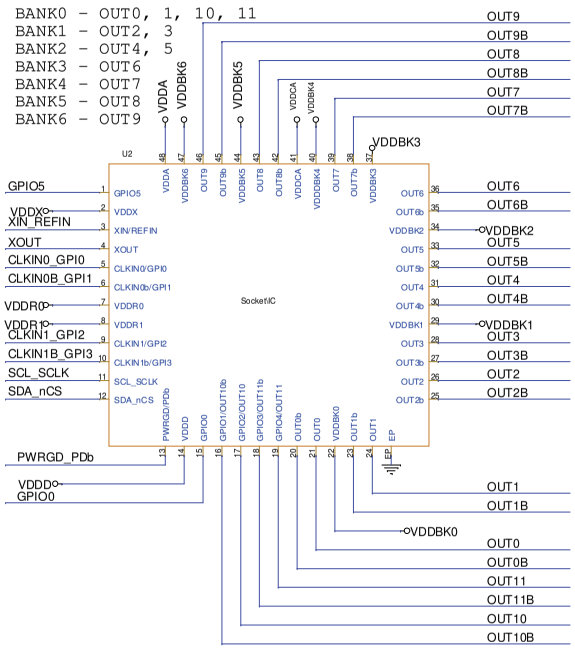
POWER



V Rail	R19
3.3V	7.5K
2.5V	11.1K
1.8V	20.0K

(18K for 1.9V to compensate for voltage drop across FB4)

BANK0 - OUT0, 1, 10, 11
BANK1 - OUT2, 3
BANK2 - OUT4, 5
BANK3 - OUT6
BANK4 - OUT7
BANK5 - OUT8
BANK6 - OUT9



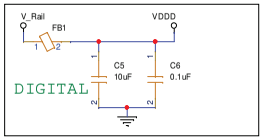
SERIAL COMMUNICATION

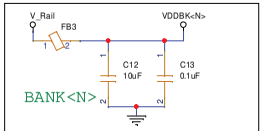
Use a level translator that will support
the serial communication speed that is needed.

I2C - Use Pull up resistors to VDDD on the VC8 side.
SPI - Route respective signals.

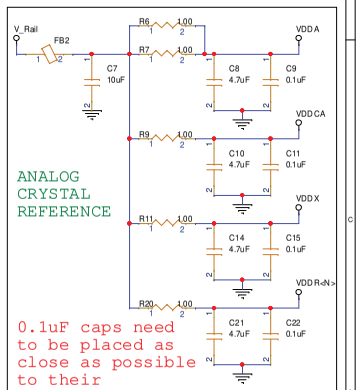
Consider adding steering jumper to GPIO0/GPIO5

POWER FILTER





Power filter when out
freq are different.
In general, use one
ferrite bead, one 10uF
and one 0.1uF cap for
each frequency. Banks
with same frequency,
use additional 0.1uF
near VDDBK<N>



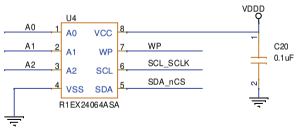
0.1uF caps need
to be placed as
close as possible
to their
corresponding VDD pins.

Ferrite bead part number is

BLM15AX601SN1D

EEPROM (001 or Q01)

A0-2 - pull hi or lo to set EEPROM address 0x50 - 0x57
WP - pull hi to prevent writing



RENESAS
Renesas
1140 West Warner Rd.
Tempe, AZ 85284

Title: RC31312A_VC8_Reference

Size	HW Number:	Engineer:	Rev.
C	Date: 02/17/2026	Sheet: 1 of 1	C