

Engineering Change Notice

The following table contains a list of engineering changes that are not reflected in the Tsi382 (BGA) Evaluation Board Schematics.

Table 1: ECN for E2010_AS001_02 (Board order number Tsi382-RDK1 V2.0)

No.	Item(s)	Original	Change To
1	Tsi382 Device	Tsi382-66ILVZ1	Tsi382-66ILVZ2
2	JTAG signals pull-ups	2K pull-up on R288, R293, R294, and R295	10K pull-up on resistors
3	EEPROM socket	No EEPROM installed in DIP-8 socket U23	Installed AT25604A-10PU-2.7 Atmel EEPROM in DIP-8 socket U23.
4	PCI reset time too short	C231	10uF, ECJ-1VB0J106M

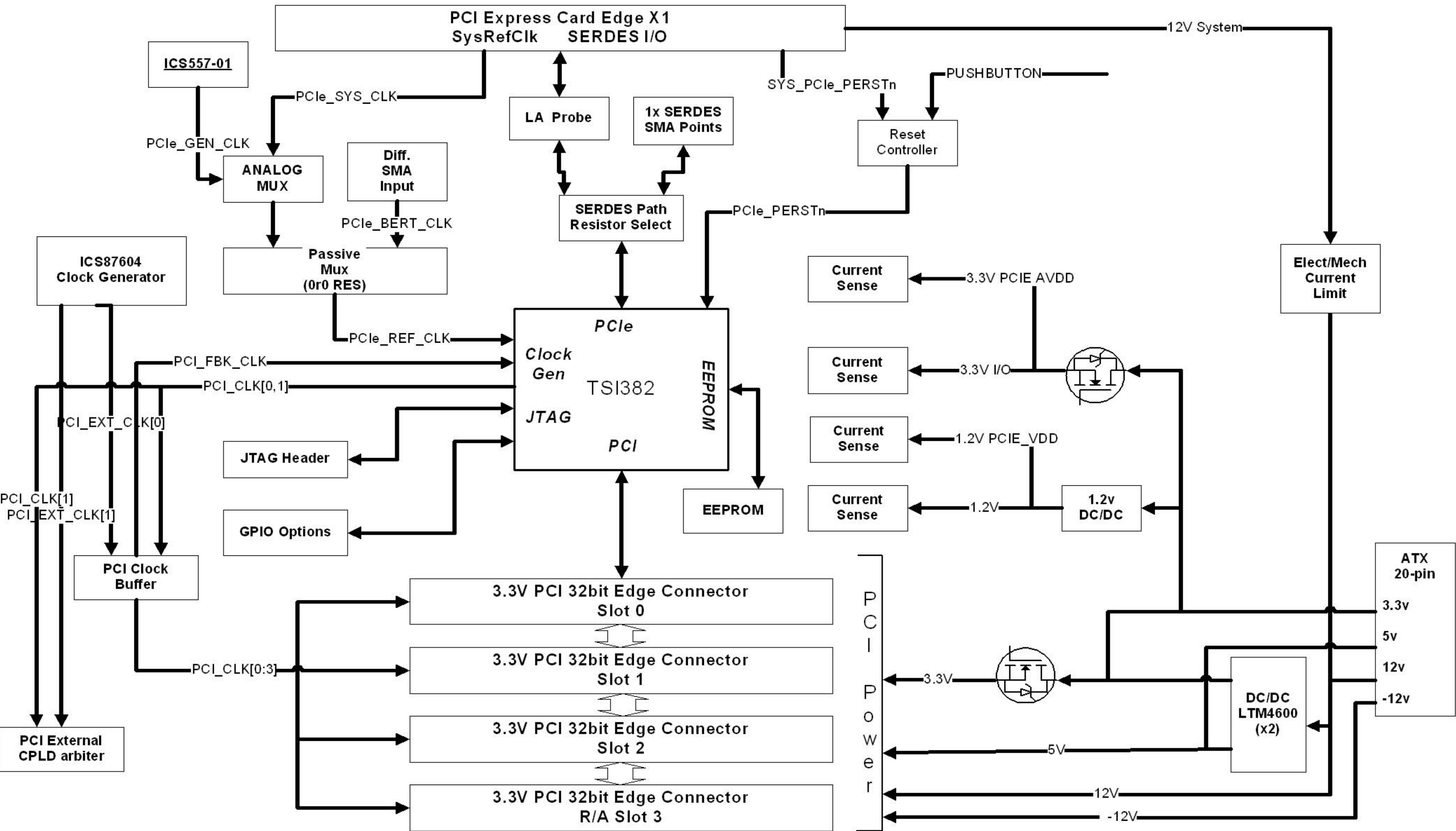
Tsi382 Evaluation Board Schematics

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C	60E2010_SC001	1.0	PHILIP LAUZON
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BLOCK DIAGRAM



TITLE : BLOCK DIAGRAM			
SIZE C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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TSI382 PCIE/MISCELLANEOUS

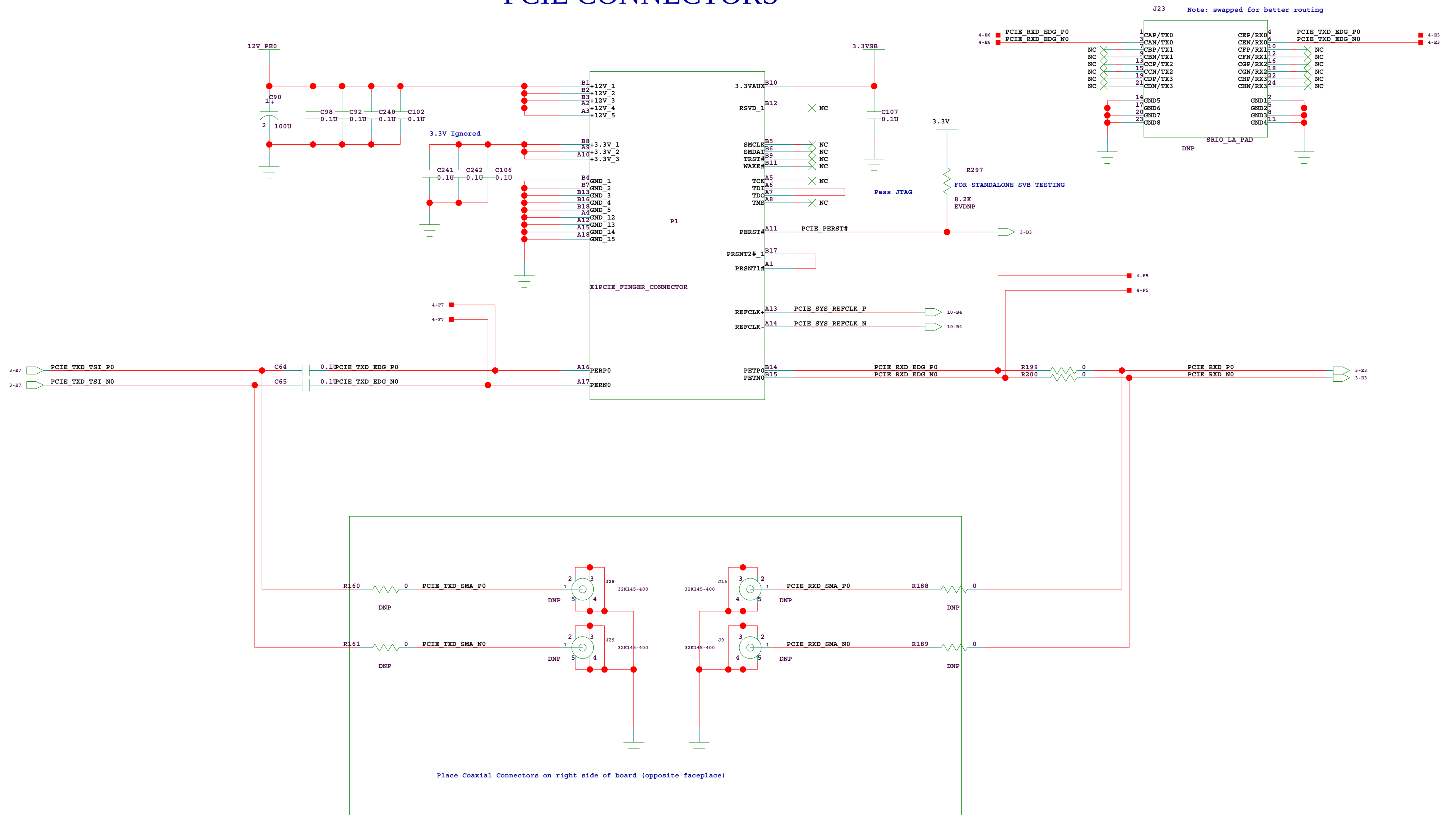
TSI382 STRAPS

RESET CONTROLLER

TSI382 JTAG

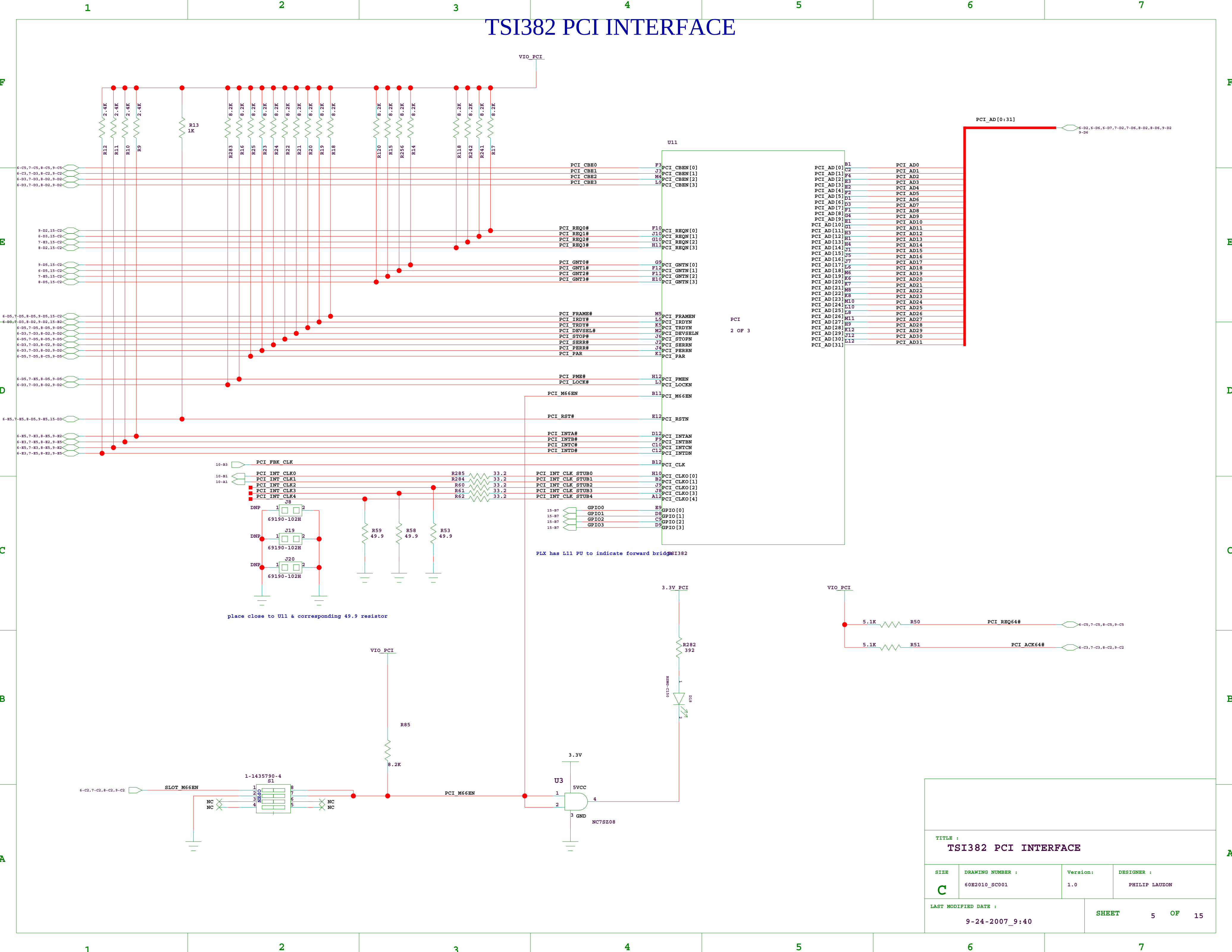
TITLE :			
TSI382 PCIE/MISC			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2010_SC001	1.0	PHILIP LAUZON
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TITLE : PCIE CONNECTORS			
SIZE C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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TSI382 PCI INTERFACE



TITLE : TSI382 PCI INTERFACE			
SIZE C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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IDSEL AD16

- Required Interrupt Routing

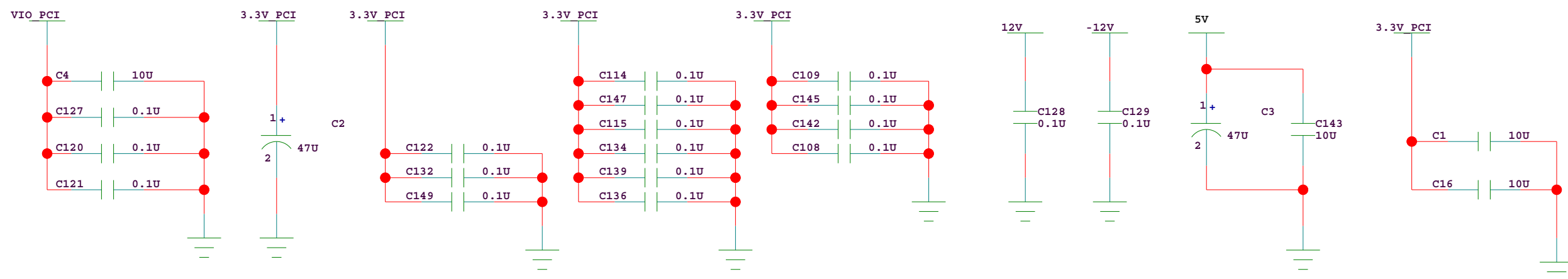
    SLOT : BRIDGE

    INTA -> INTA
    INTB -> INTB
    INTC -> INTC
    INTD -> INTD

- PCI Clock PCI_CLK0

- PCI Arbitration PCI_GNT#1/PCI_REQ#1

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TITLE : PCI SLOT 0			
SIZE C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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PCI SLOT 1 (Vertical)

IDSEL AD17

- Required Interrupt Routing

SLOT : BRIDGE

INTA -> INTB

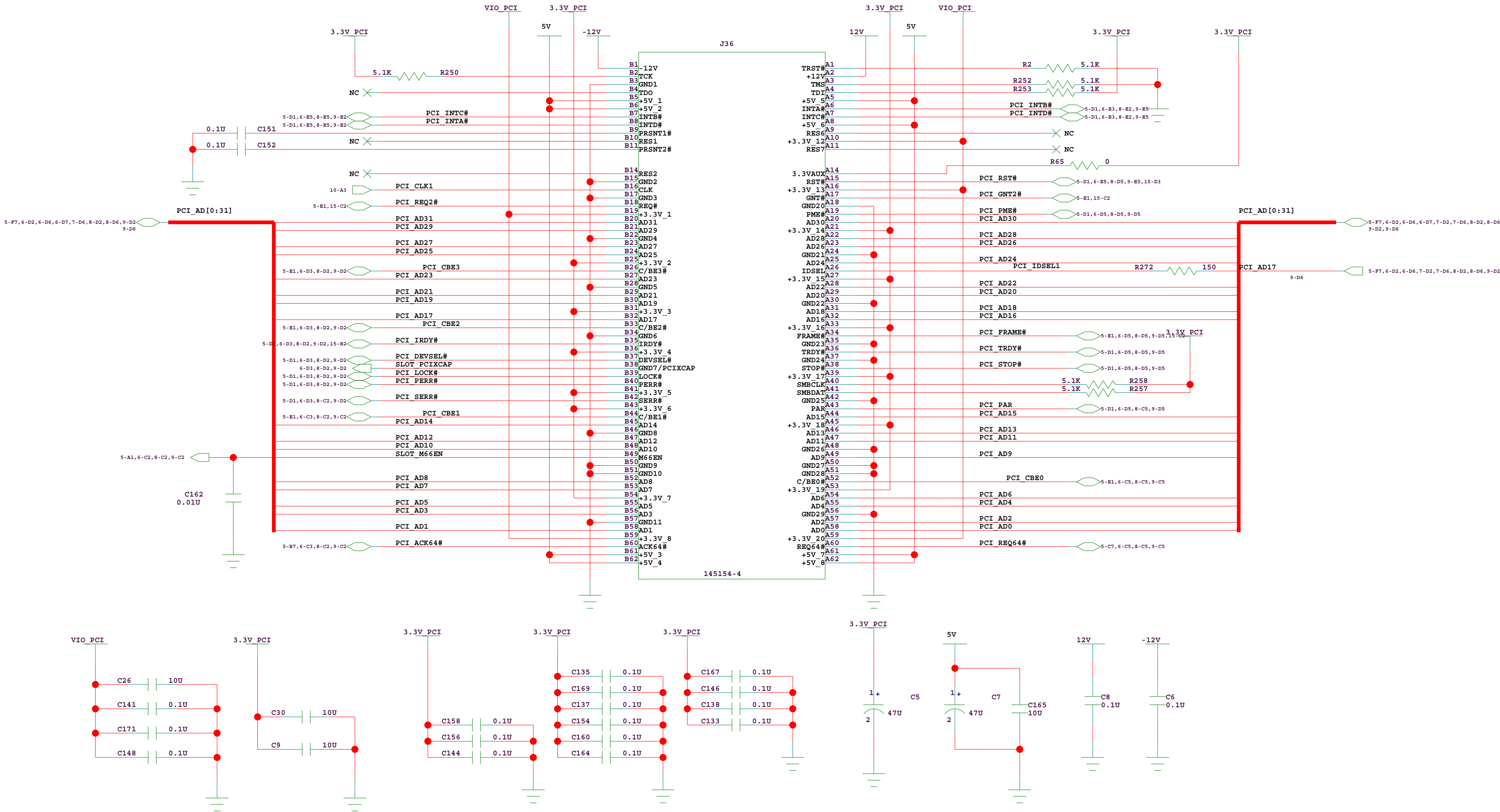
INTB -> INTC

INTC -> INTD

INTD -> INTA

- PCI Clock PCI_CLK1

- PCI Arbitration PCI_GNT#2/PCI_REQ#2



TITLE :			
PCI SLOT 1			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2010_SC001	1.0	PHILIP LAUZON
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PCI SLOT 3 (Vertical)

IDSEL AD18

- Required Interrupt Routing

SLOT : BRIDGE

INTA -> INTC

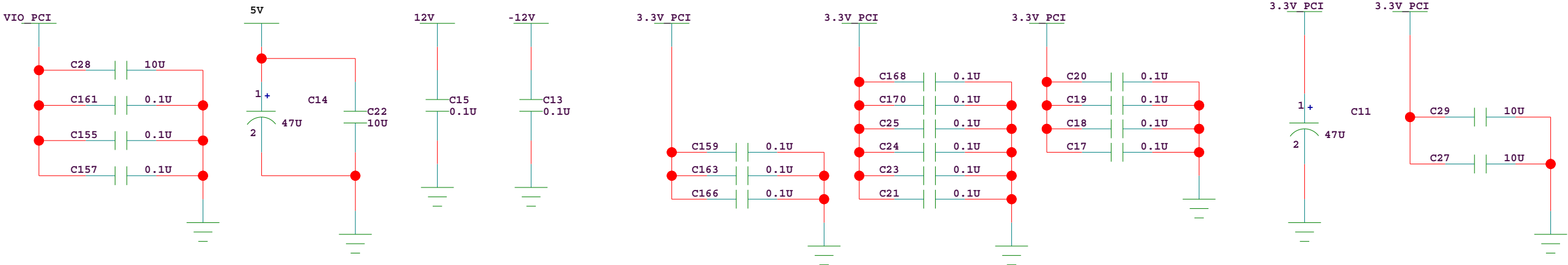
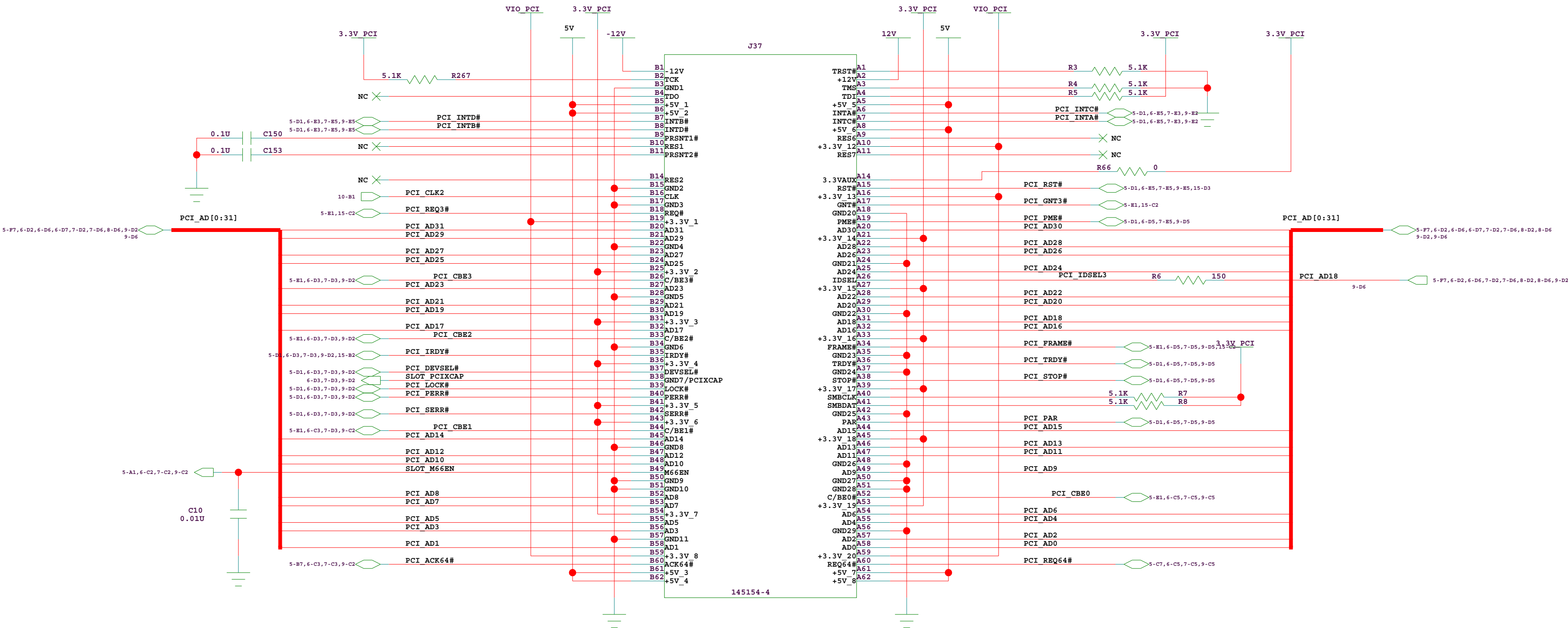
INTB -> INTD

INTC -> INTA

INTD -> INTB

- PCI Clock PCI_CLK2

- PCI Arbitration PCI_GNT#3/PCI_REQ#3



TITLE :			
PCI SLOT 3			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2010_SC001	1.0	PHILIP LAUZON
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PCI SLOT 2 (Vertical)

IDSEL AD19

- Required Interrupt Routing

SLOT : BRIDGE

INTA -> INTD

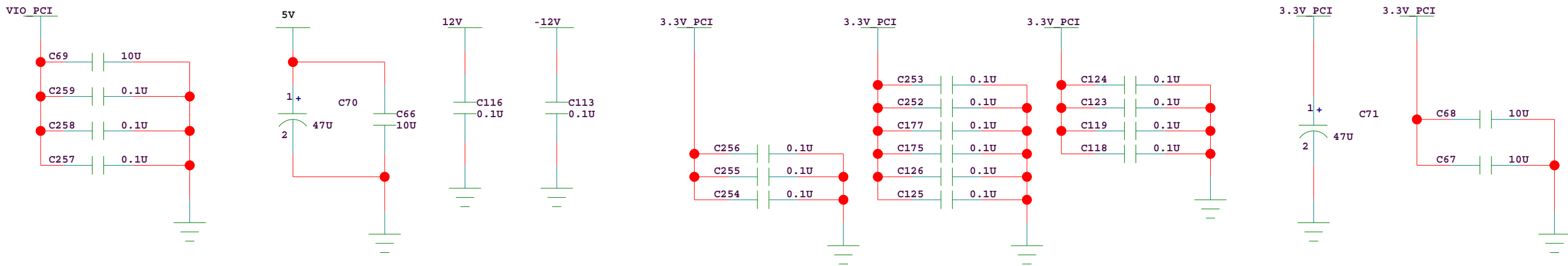
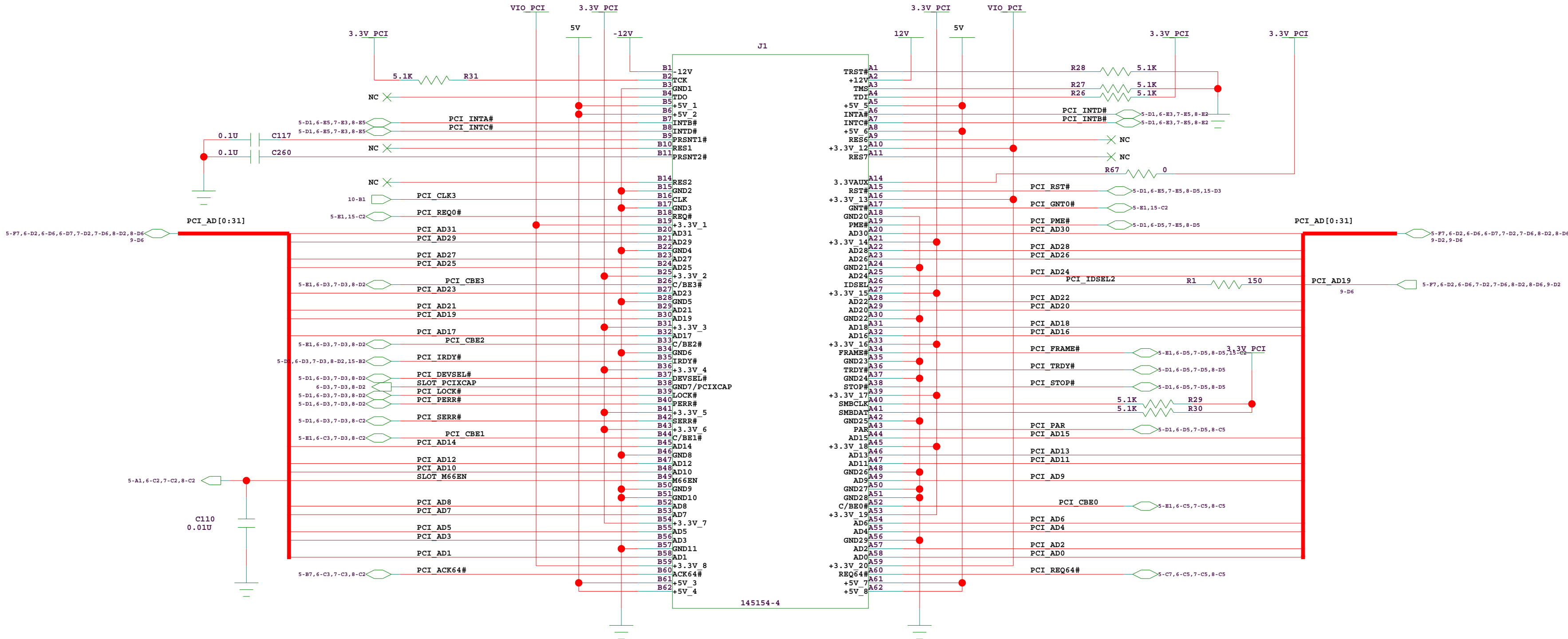
INTB -> INTA

INTC -> INTB

INTD -> INTC

- PCI Clock PCI_CLK3

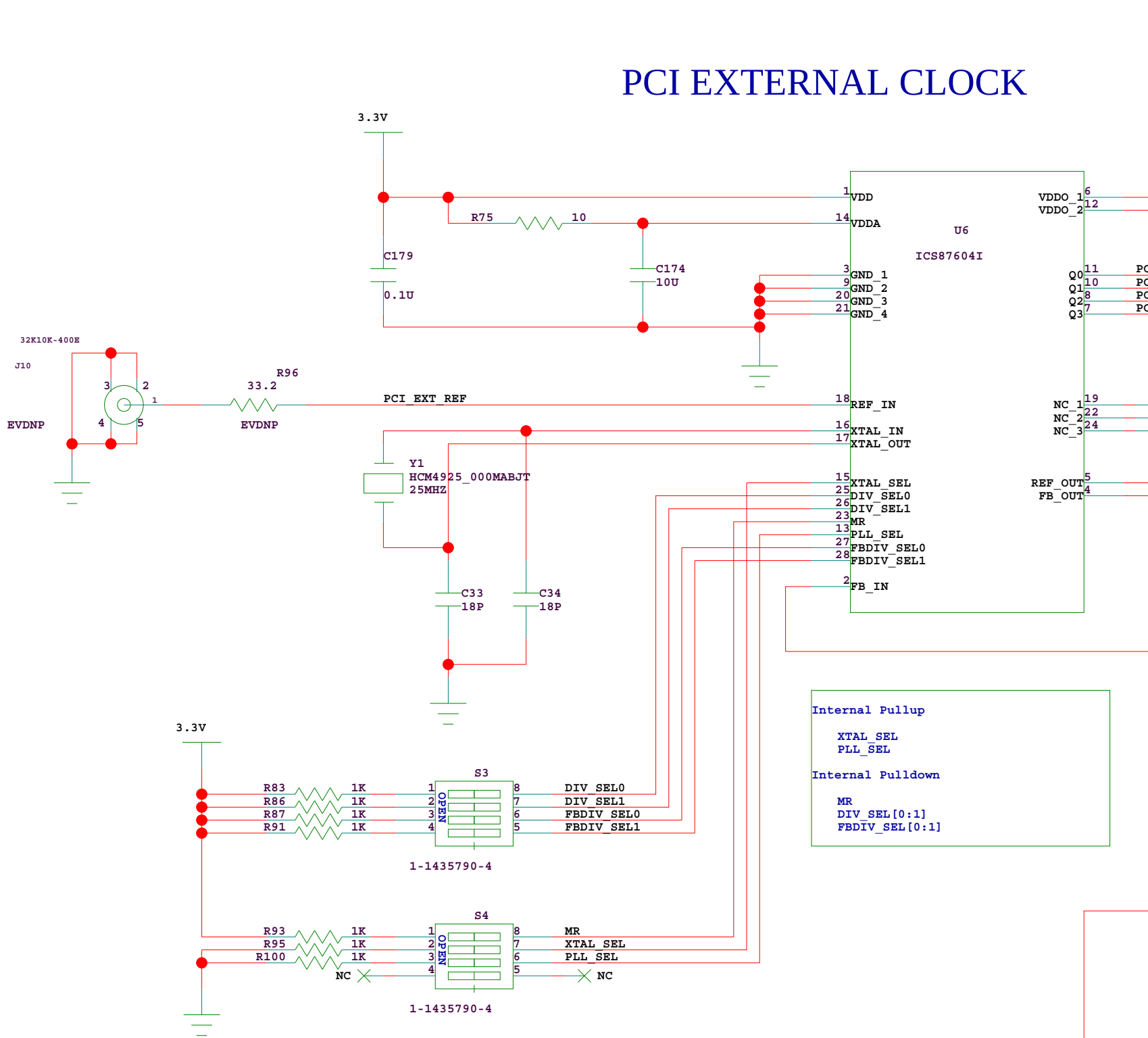
- PCI Arbitration PCI_GNT#0/PCI_REQ#0



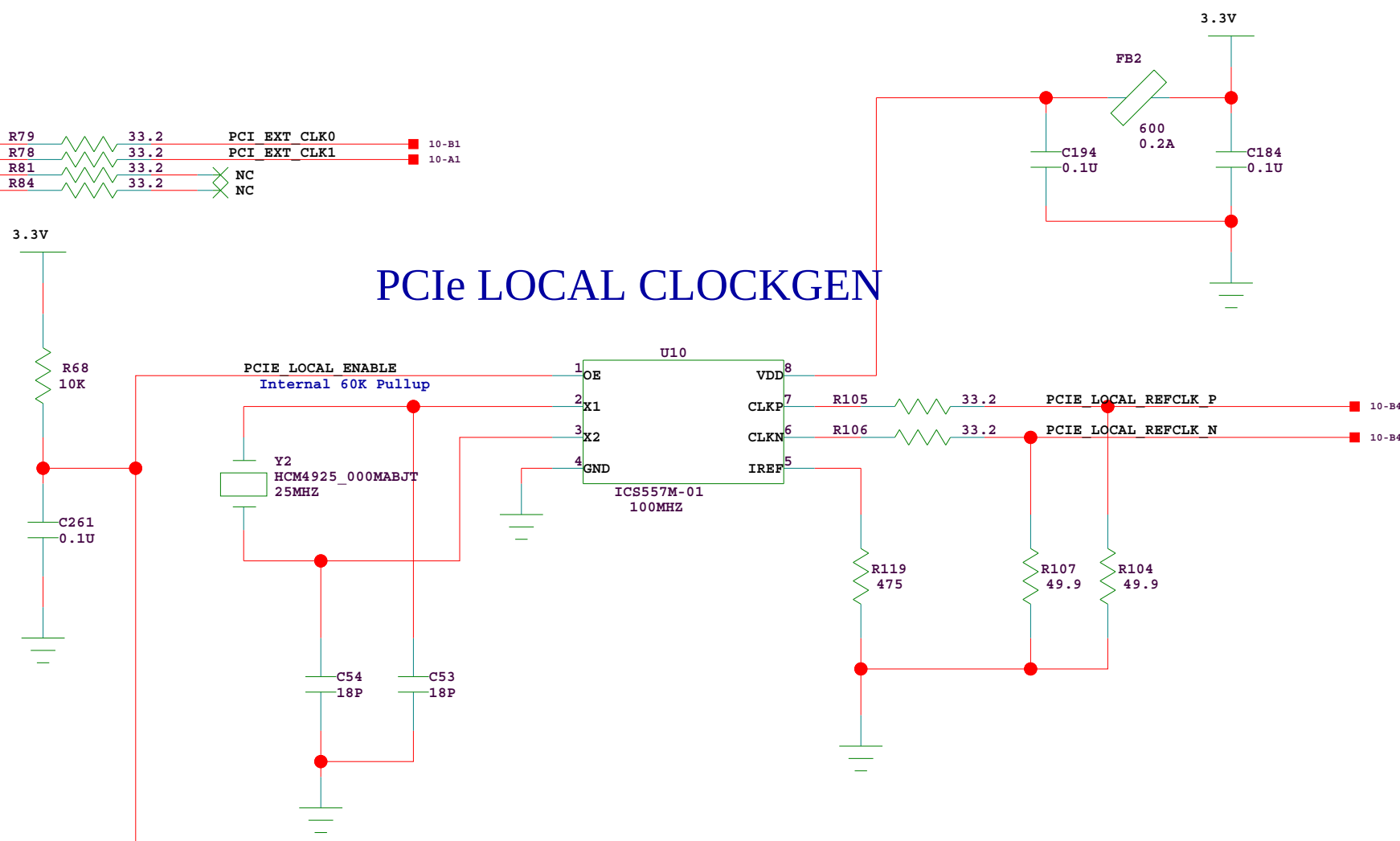
TITLE :			
PCI SLOT 2			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2010_SC001	1.0	PHILIP LAUZON
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CLOCK DISTRIBUTION

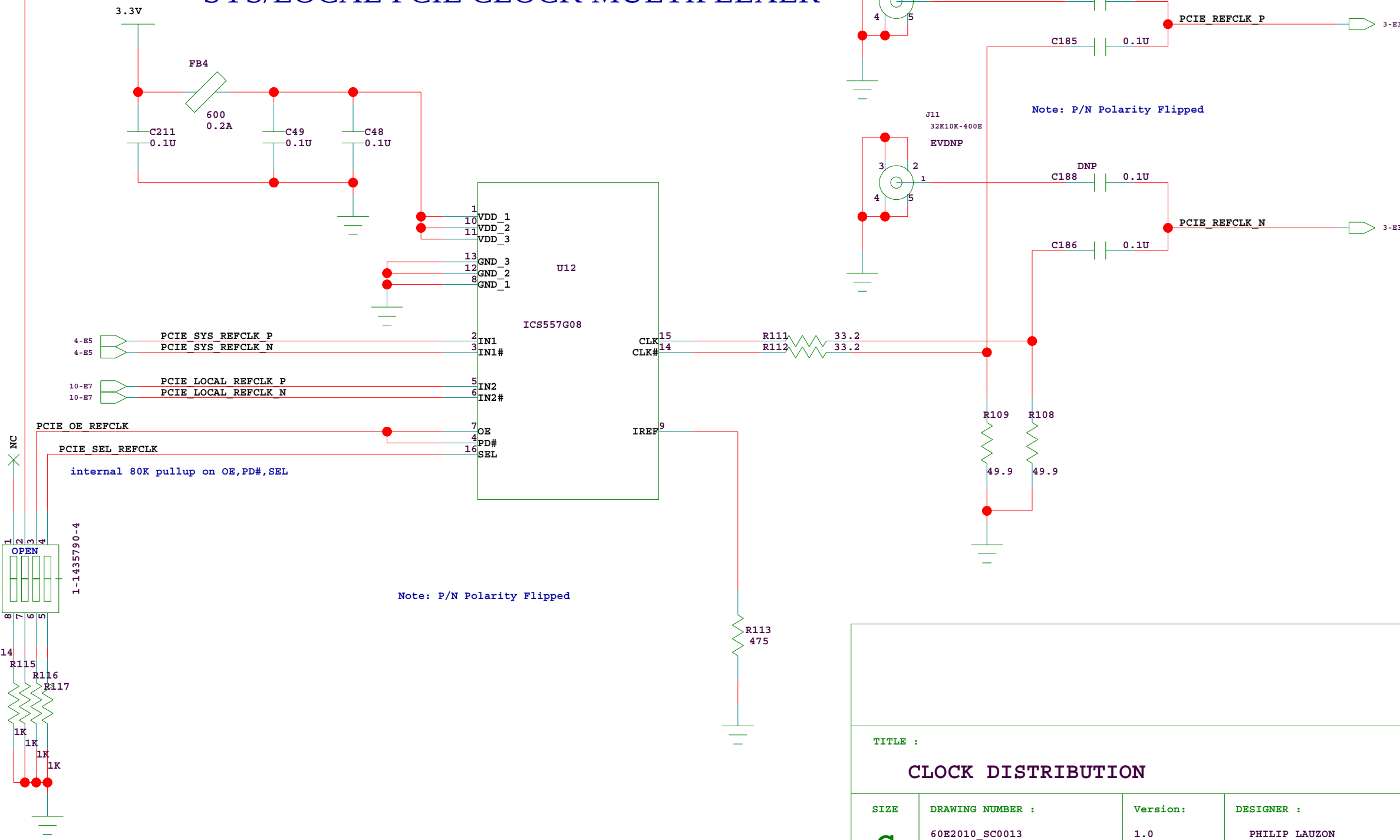
PCI EXTERNAL CLOCK



PCIe LOCAL CLOCKGEN



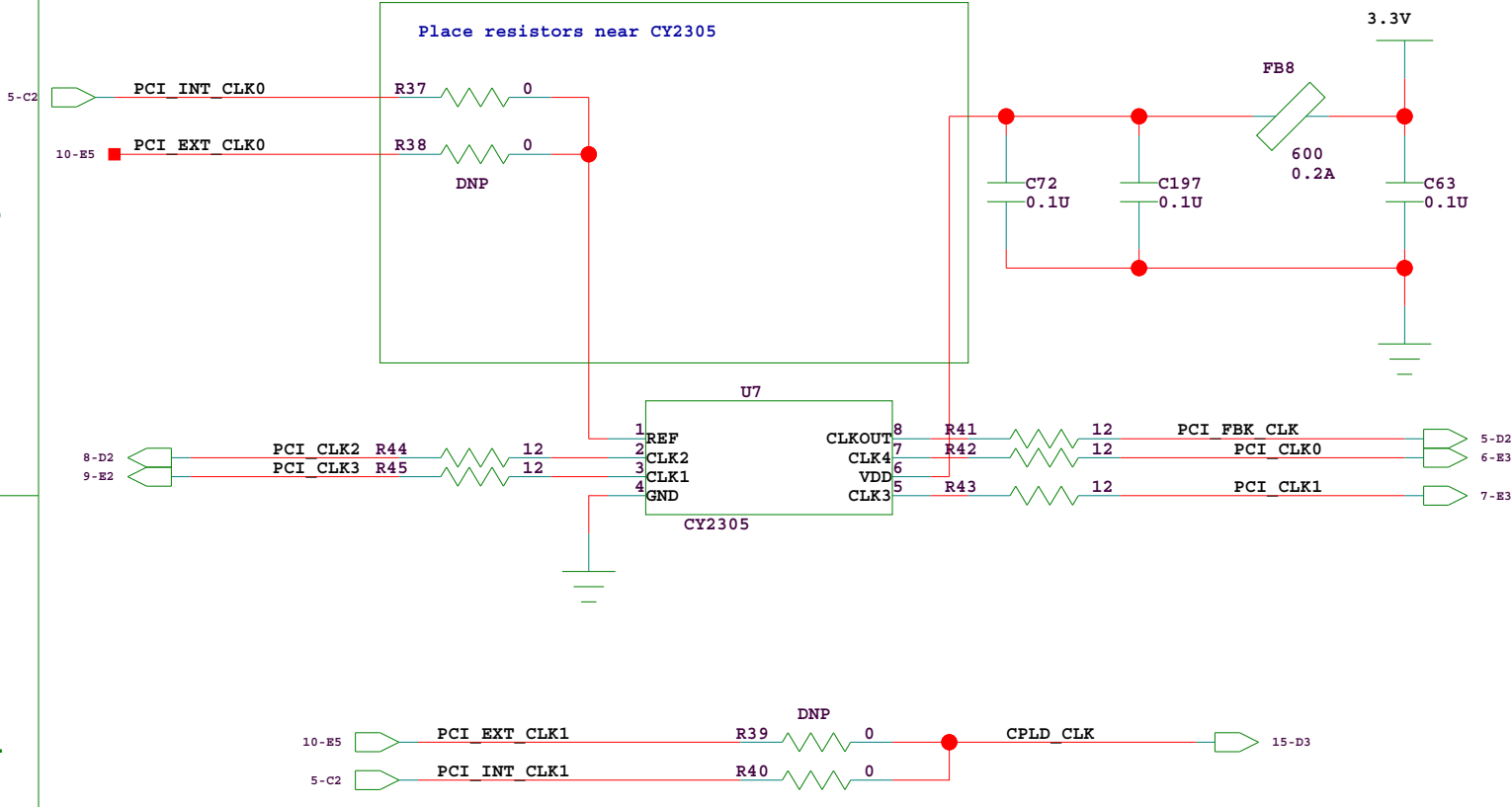
SYS/LOCAL PCIe CLOCK MULTIPLEXER



Frequency Select (ICS87604I)

FBDIV_SEL[0:1]	DIV_SEL[0:1]	OUTPUT
0:0	0:0	100Mhz
0:0	1:0	50Mhz
0:0	1:1	25Mhz
0:1	0:0	133Mhz
0:1	1:0	66Mhz
0:1	1:1	33Mhz

Place resistors near CY2305



TITLE :
CLOCK DISTRIBUTION

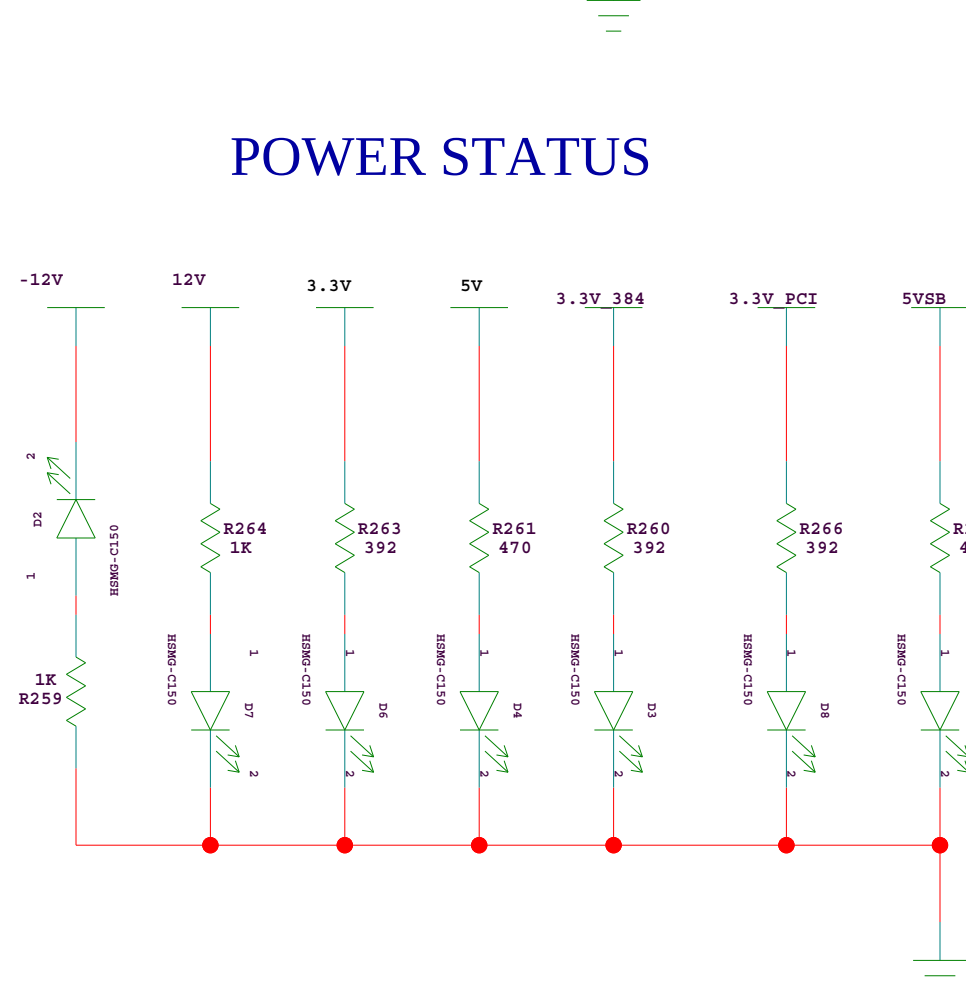
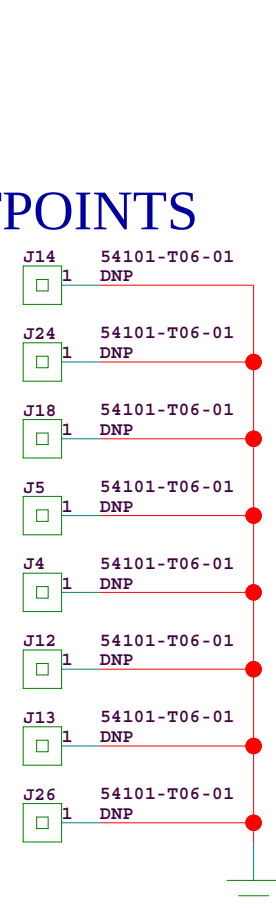
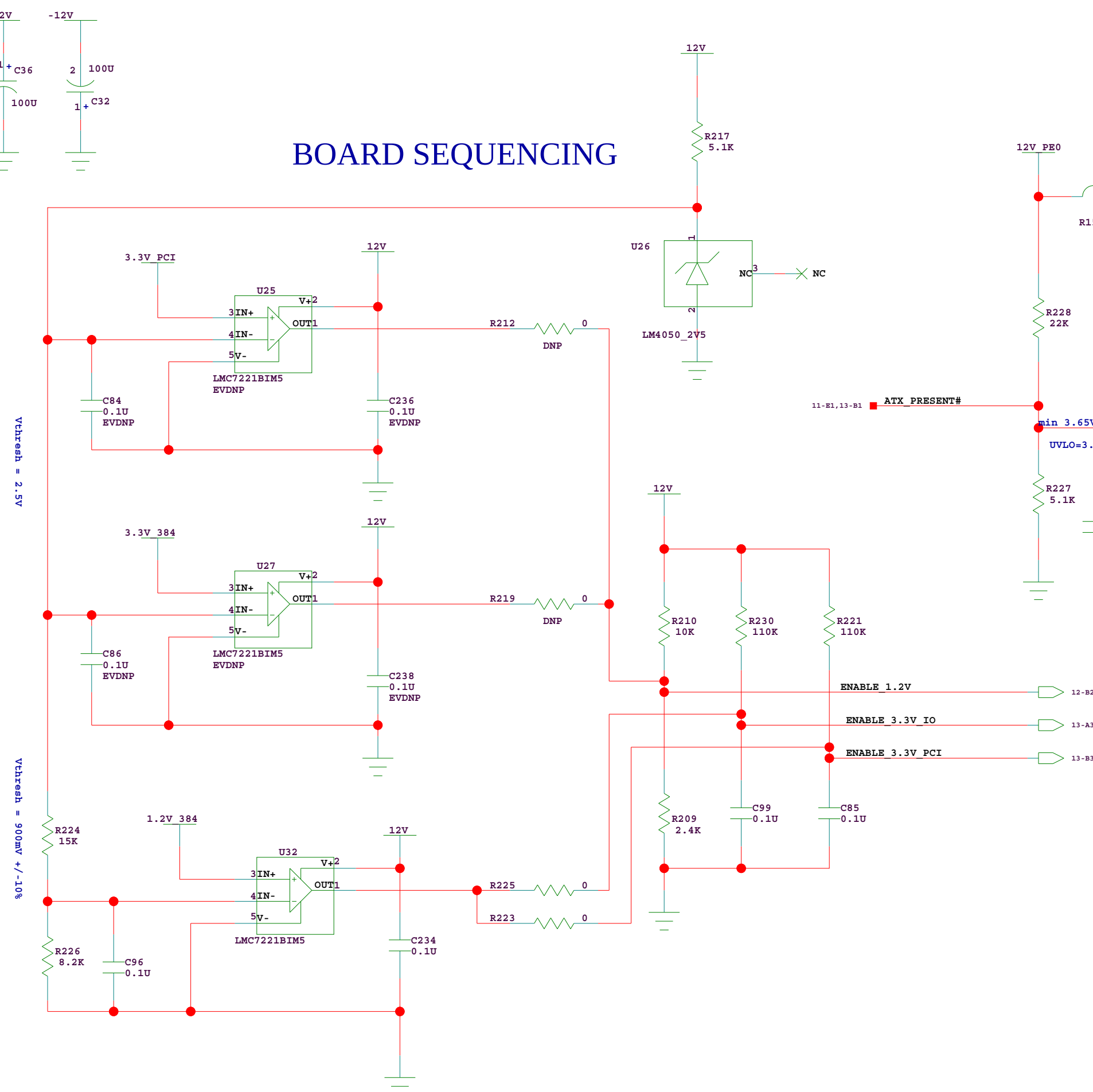
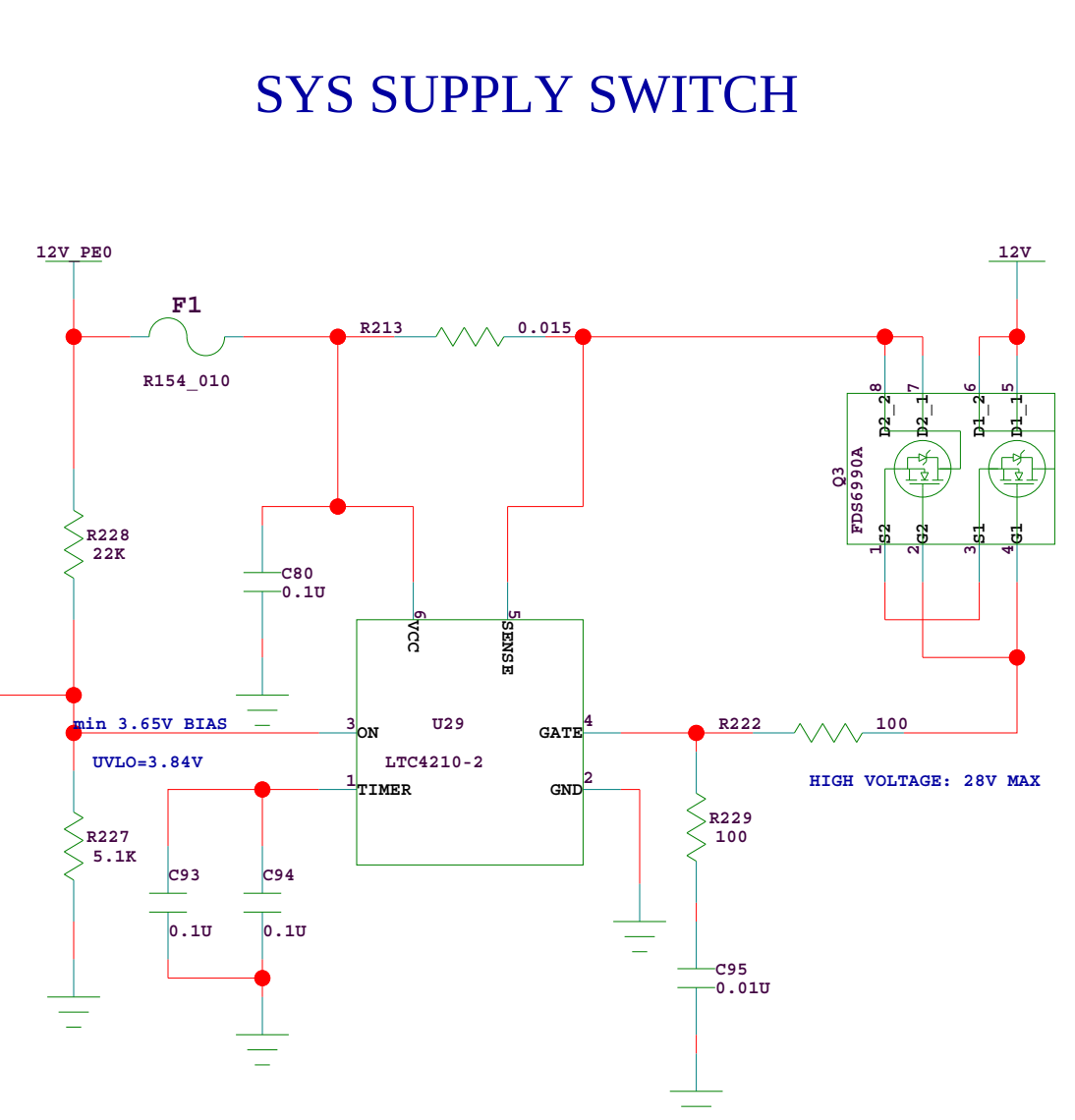
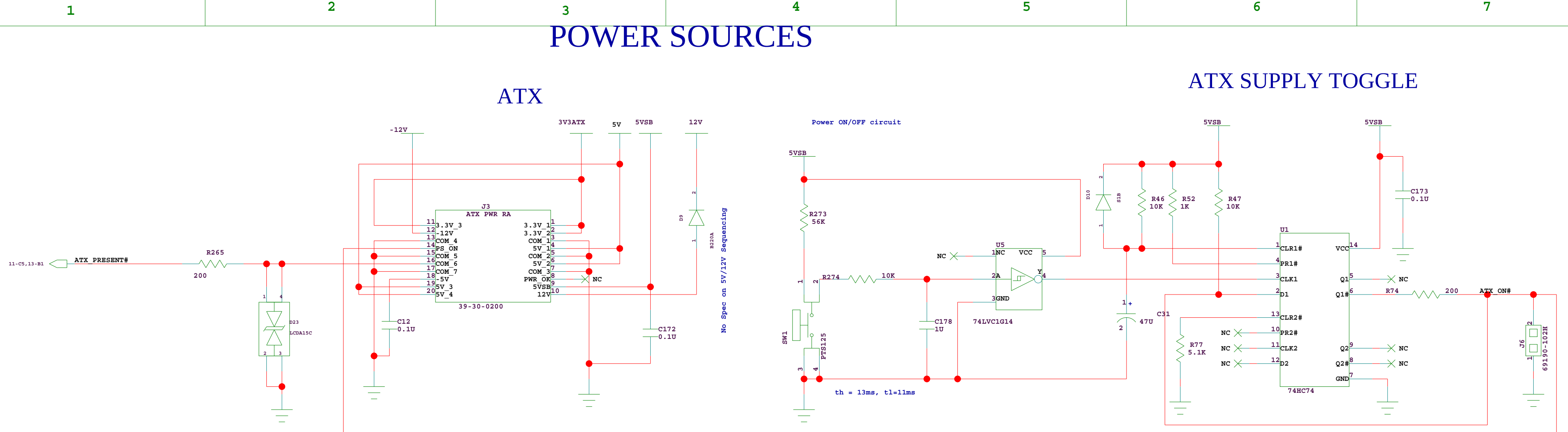
SIZE C	DRAWING NUMBER : 60E2010_SC0013	Version: 1.0	DESIGNER : PHILIP LAUZON
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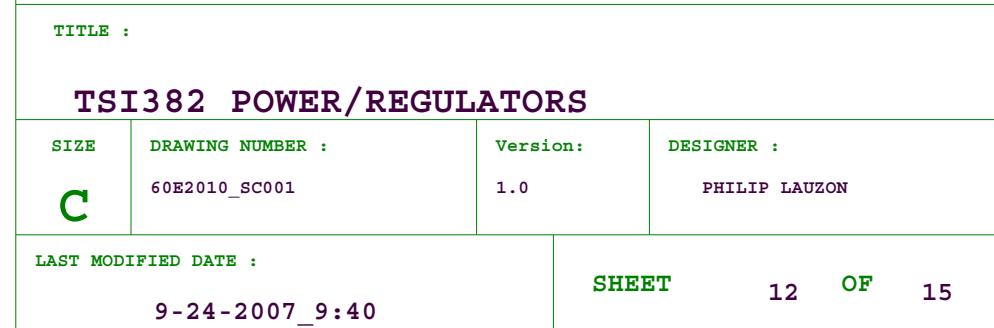
6



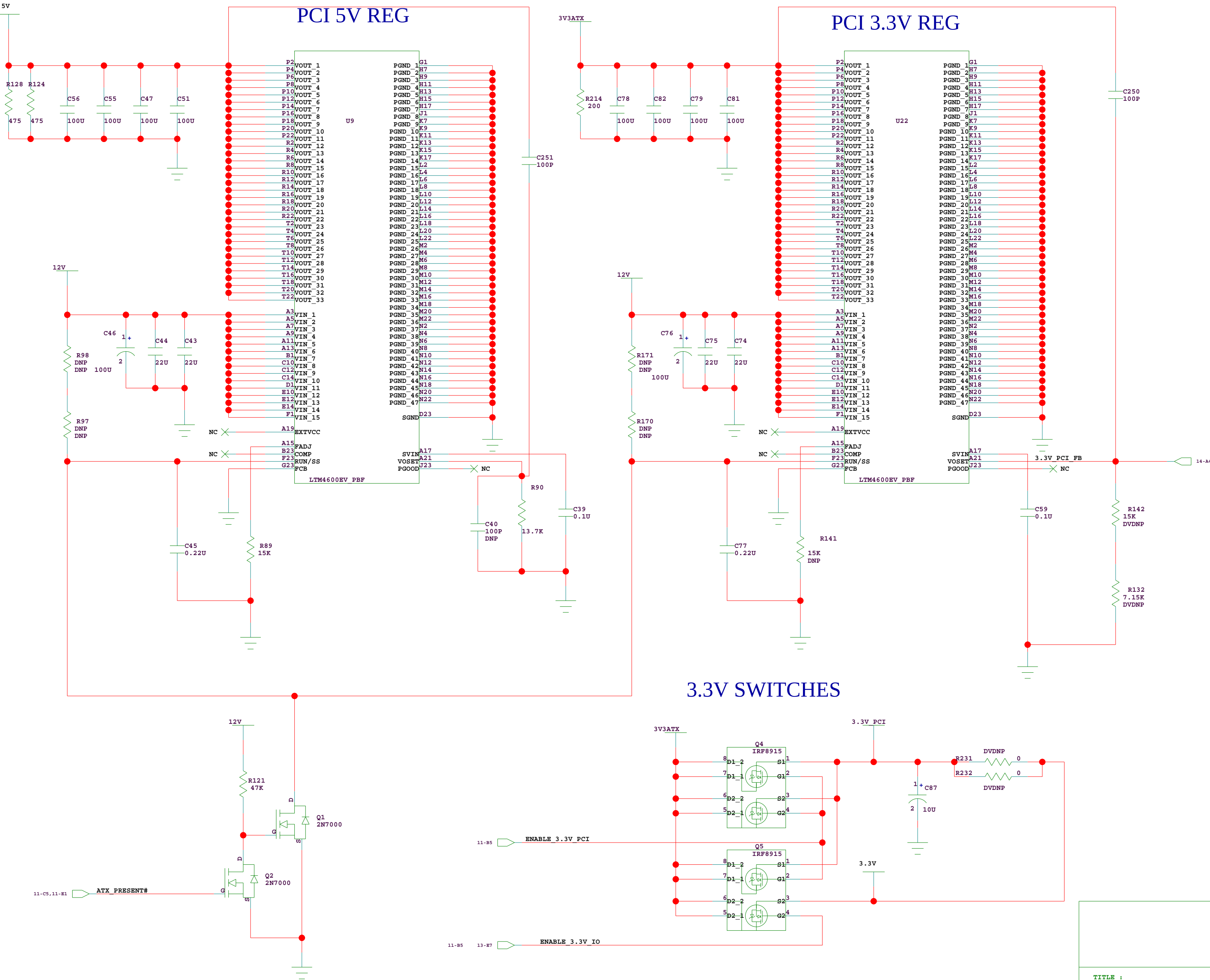
TITLE : POWER SOURCES			
SIZE C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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TSI382 VDD REG

TSI382 POWER/REGULATORS



PCI POWER REGULATORS



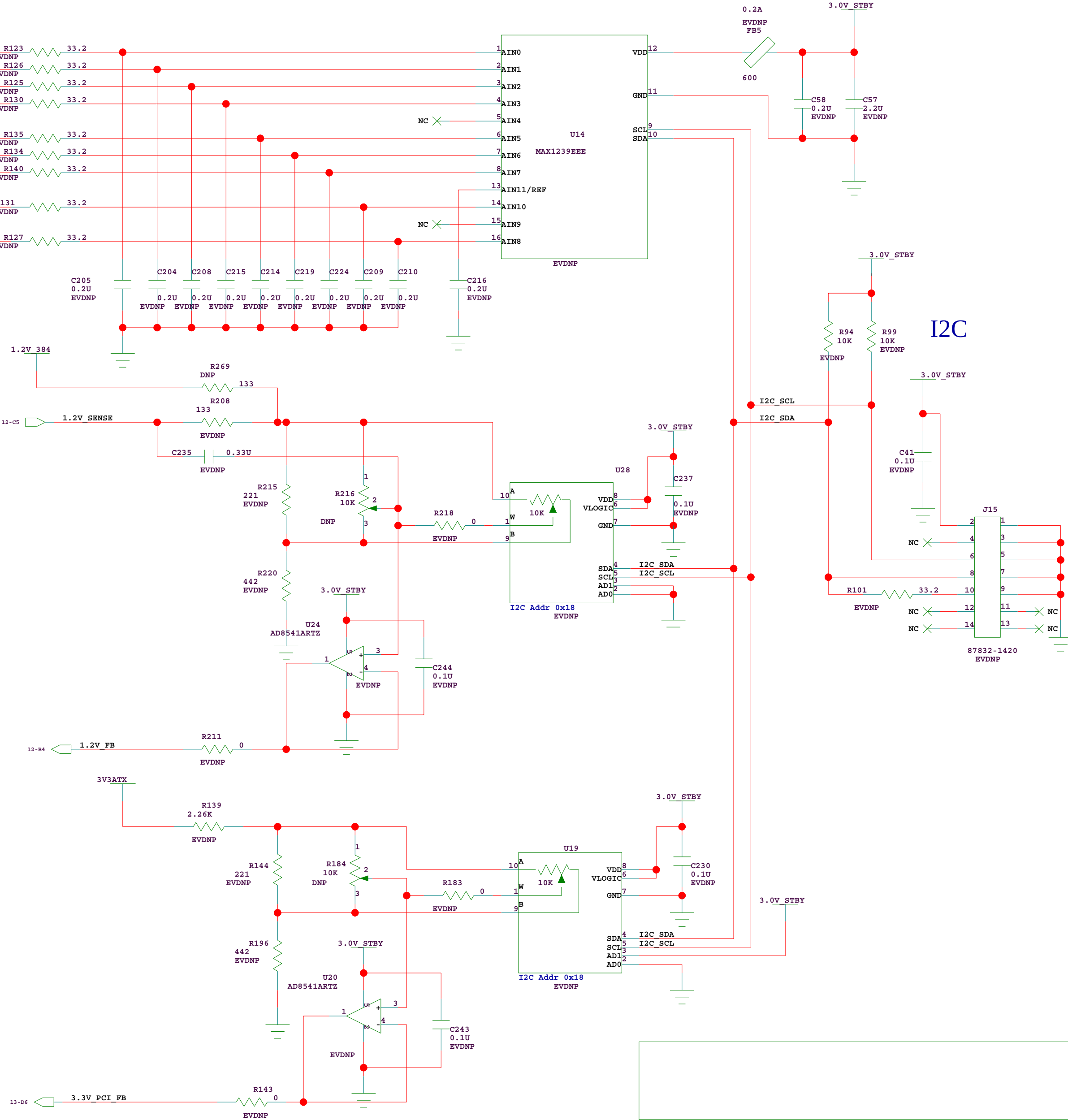
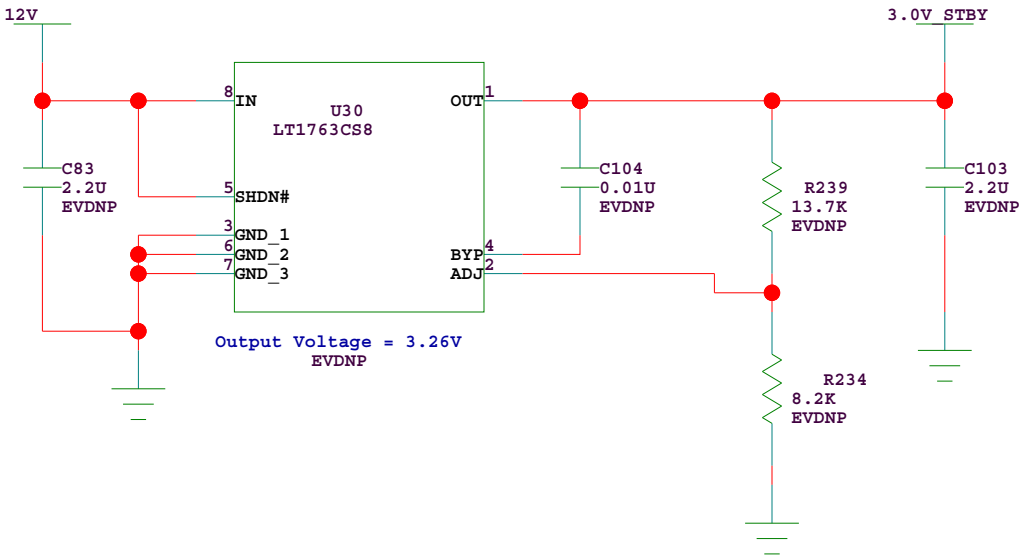
TITLE :			
PCI POWER REGULATORS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2010_SC001	1.0	PHILIP LAUZON
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TEST DEVICES

TSI382 V/I ADC

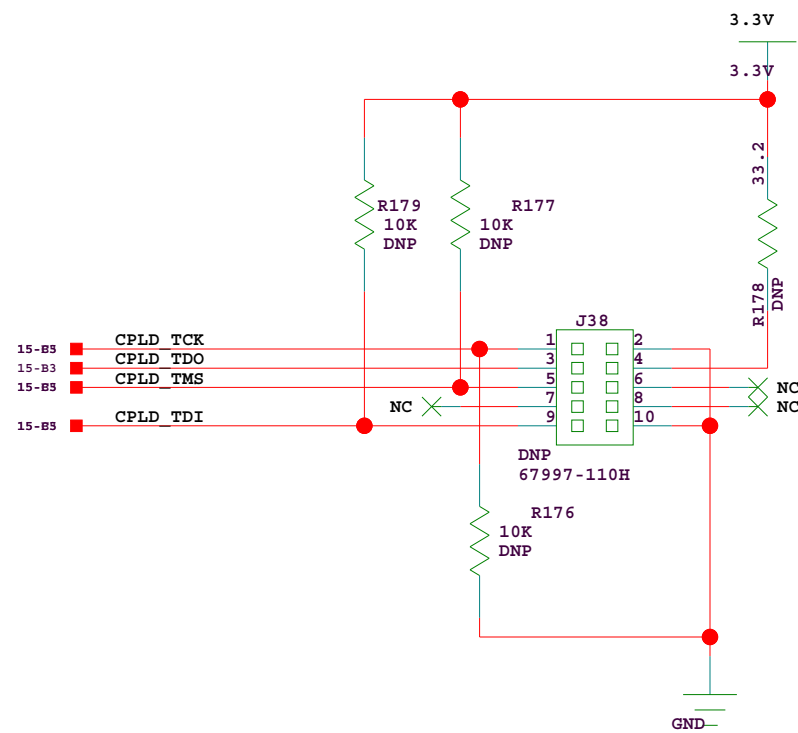
ANALOG SUPPLY

I2C

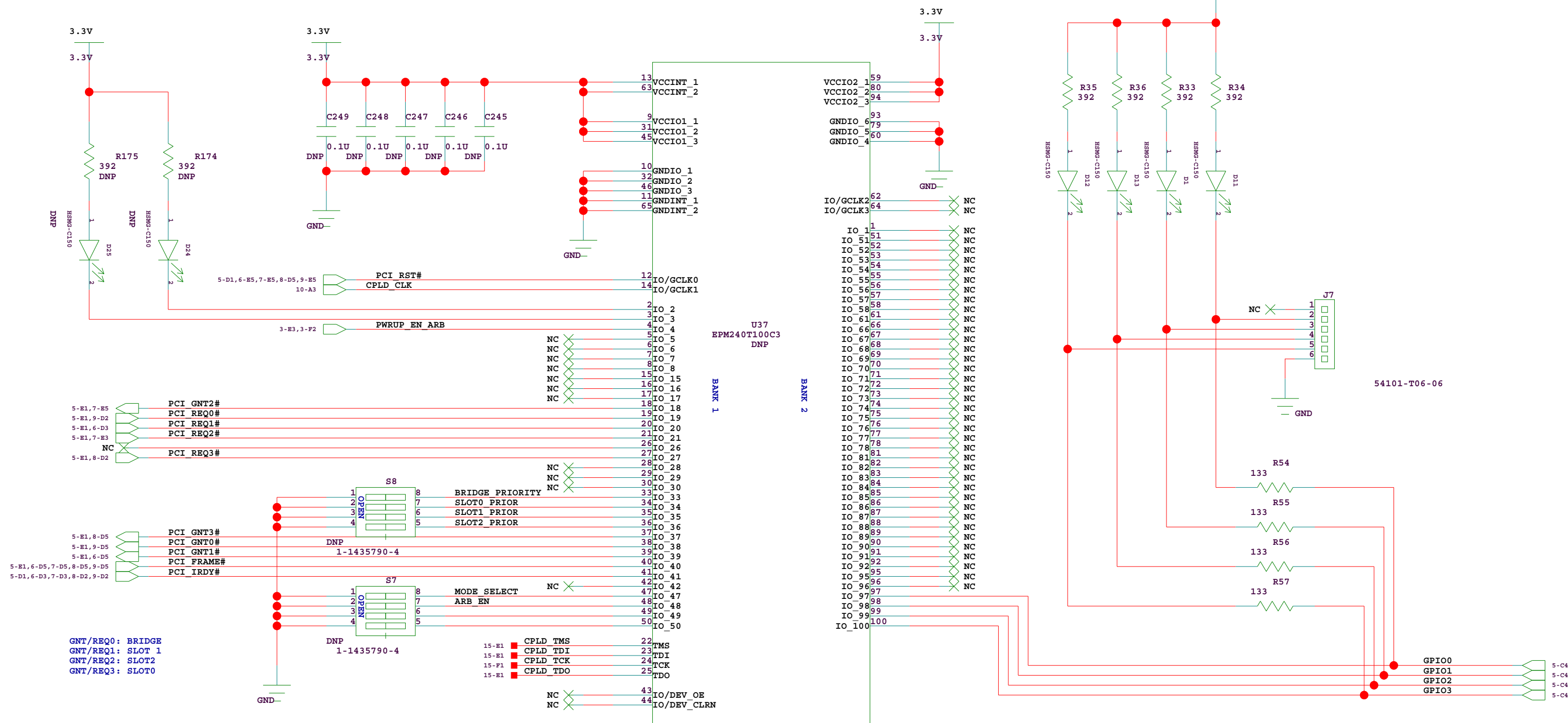


TITLE : TEST DEVICES			
SIZE C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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TEST DEVICES CONT'D



PCIARBITER/GPIO CONTROL



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TEST DEVICES CONT'D			
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