4RCD0232KC1

DDR4RCD02 Register Command Address Buffer and Parity

The 4RCD0232KC1 is a 32-bit 1:2 register command, address buffer with parity, designed for 1.2V VDD operation. The device is intended for RDIMM/LRDIMM applications.

[Planned] decode logic to support DIMMs that populate eight ranks of memory or higher. [Planned] additional SI features to support DIMMs greater than 30mm height.

All inputs are pseudo-differential with an external or internal voltage reference. All outputs are full swing CMOS drivers optimized to drive single terminated 25Ω to 50Ω traces in DDR4 RDIMM and LRDIMM applications. The clock outputs Yn_t and Yn_c and the control net outputs QxCKEn, QxCSn and QxODTn can be driven with a different strengths to compensate for different DIMM net topologies. By disabling unused outputs the power consumption is reduced.

The 4RCD0232KC1 operates from a differential clock, CK_t and CK_c. Inputs are registered at the crossing of CK_t going HIGH, and CK_c going LOW. The input signals could be either re-driven to the outputs or they could be used to access device internal control registers when certain input conditions are met. The control word mechanism is described in more detail in the “Control Word Decoding” section of the datasheet.

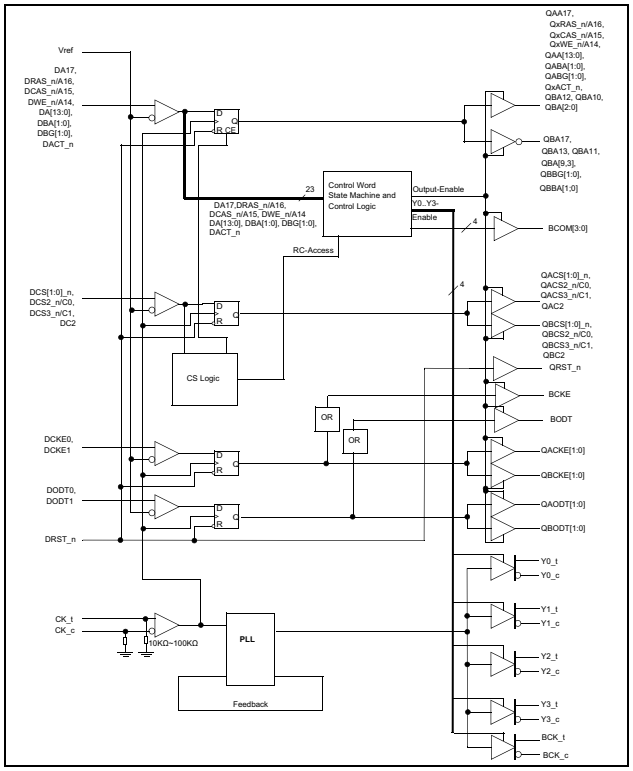
Applications

- DDR4 RDIMM
- DDR4 LRDIMM

Features

- Pinout optimized DDR4 RDIMM PCB layout
- DDR4-1600/1866/2133/2400/2666/2933/3200
- Supports CKE Power Down operation modes
- Support Quad Chip Select Operation
  - Direct Dual CS Mode
  - Direct QuadCS Mode
  - Encoded QuadCS Mode
- Provides access to internal control words for configuring the device features and adapting in different RDIMM and system applications
- Compliant to *JEDEC DDR4RCD02 Specification, Revision 1.0*
- Packaging: 253-ball dual-pitch (0.50mm/0.65mm), 15 × 20 grid, rectangular BGA
  - Available in commercial temp. range (0°C to 70°C) and industrial temp. range (-40°C to 85°C)

Block Diagram



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