9QXL1200

DB1206 PCIe Gen7 Fanout Buffer with LOS

Description

The 9QXL1200 is an ultra-high performance fanout buffer supporting PCIe Gen1 through Gen7. It provides a Loss-Of-Signal (LOS) output for system monitoring and resiliency. The device also incorporates Power Down Tolerant (PDT) and Flexible Startup Sequencing (FSS) features, easing system design. It can drive both source-terminated and double-terminated loads, operating up to 400MHz. The Renesas 9QXL1200 also enhances system security with two modes of SMBus write protection.

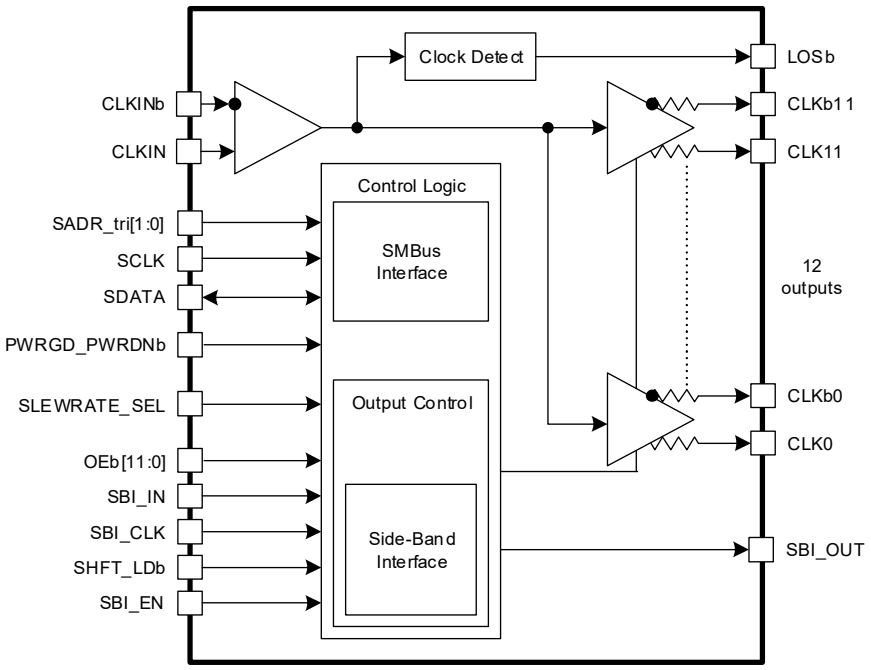
The 9QXL1200 provides 12 Low-Power (LP) HCSL output pairs in a 5.0 × 5.0 mm dual-row LGA package. The 9QXL1200 devices offer higher output counts in smaller packages compared to earlier buffer families. The buffers support both Common Clock (CC) and Independent Reference (IR) PCIe clock architectures.

Applications

- Cloud/High-performance computing
- nVME storage
- Networking
- AI Accelerators

Features

- PCIe Gen6 additive phase jitter: 4fs RMS
- PCIe Gen7 additive phase jitter: 2.8fs RMS
- DB2000Q/DB1206 additive phase jitter: 12fs RMS
- 12kHz–20MHz additive phase jitter: 36fs RMS at 156.25MHz
- Power Down Tolerant (PDT) inputs
- Flexible Startup Sequencing (FSS)
- SMBus enabled Automatic Clock Parking (ACP)
- Two software-controlled SMBus write protection modes
- Spread-spectrum tolerant
- CLKIN accepts HCSL or LVDS signal levels
- Selectable output slew rate via pin/SMBus
- 4-wire Side-Band Interface supports high-speed serial output enable and device daisy-chaining
- Nine SMBus addresses plus write protection
- 12 LP-HCSL 85Ω impedance outputs
- 12 dedicated output enable pins
- -40°C to +105°C, 3.3V ±10% operation



Note: The SBI pins are muxed with specific OEb pins. See details in the datasheet.

Figure 1. 9QXL1200 Block Diagram

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