

DA14495

Multi Level Modulation 1.9 GHz DECT SoC

This short datasheet is an addendum to the DA14495 datasheet.

The DA14495 is a CMOS IC with integrated radio transceiver with RFPA and baseband processors for DECT, DECT 6.0, Japanese DECT, Korean DECT, and CAT-iq applications and is optimized for HiFi wireless Audio applications. It supports multilevel modulation up to D8PSK for bit rates from 1.152 Mbit/s up to 3.456 Mbit/s. The program memory and data storage reside in an external low pin count Quad SPI (QSPI) Serial Flash or RAM.

Key Features

- Complies with DECT EN 300 175-2,3,8, DECT 6.0, Japanese DECT, and Korean DECT (1.7 GHz)
- Processing power
 - 165.888 MHz 32-bit Arm® Cortex®-M0
 - 290.304 MHz 32-bit Tensilica LX4/HiFi-3 DSP
 - Triple Stereo Hardware Sample Rate Converter (SRC) supporting 2xPCM, SPDIF, and 6xPDM
 - DIP-V2 with DSAA1/2, DSC1/2, AES256, FEC
 - Crypto engine supporting AES128/256, ECB with CBC and CTR modes and HASH-256, Random Number Generator FIPS140-2 compliant
 - 4-ch SYS-DMA, 12-ch DSP-DMA controllers
- Development/Debug support
 - Arm 2-wire SWD with 8 hardware breakpoints and 2 watch points
 - Arm instruction, DIP and DSP event trace
 - DSP debugger with 1 and 5-wire JTAG interfaces
- Memories
 - Arm Cortex-M0 16 kB instruction/data cache
 - 64 kB state retainable shared System RAM
 - 256 kB multibank shared DSP-RAM
 - 64 B factory programmed OTP with device unique number
- Power management
 - 1.9 V to 5 V Battery voltage, 1.2 V Core voltage
 - On-chip LDOs, 1.8 V, 3.3 V, 1.2 V
 - On-chip LDO 1.4 V to prevent battery wear
 - Integrated DC-DC step-down converter to 1.4 V
 - Ultra Low Energy (ULE) support with port wake-up, port and RAM retention and retention LDOs 1.2 V, 1.8 V, 3.3 V
 - 4 Independent VDDIO pin groups 1.8 V to 3.45 V
 - Integrated Battery Charging circuit for Li-Ion/Li-Po with NTC protection circuit
- Analog interfaces
 - 2 input 10-bit ADC, single ended/differential
 - Integrated Temperature sensor
 - Brown-out supply voltage detectors
 - USB Charging detection (Complies to Battery Charging Specification version 1.2 (BC v1.2)) + 1.2 V comparators + ADC measurement of D+/D-
- Oscillators and PLLs
 - 20.736 MHz Crystal oscillator with low power mode
 - 16 MHz RC oscillator
 - 32.768 kHz Crystal oscillator
 - 32 kHz RC oscillator
 - 290.304 MHz SYS-PLL, 48 MHz PLL for USB
- Digital interfaces
 - USB 2.0 HS/FS Device/Host MAC/PHY with DMA
 - 82.944 MHz.1.8 V to 3.3 V QSPI Flash/RAM interface
 - Programmable Pin Assignment
 - 41 IO pads with state retention and slope control
 - Three back-drive protected PADs for LEDs
 - Keyboard interface with per pin debouncing
 - Dual UART Full duplex 9.6 kBd to 812.5 kBd with FIFO and DMA support
 - Dual SPI™ interface 20.736 MHz (Master/Slave)
 - I2C interface 100 kHz, 400 kHz, 1.152 MHz (M/S)
 - Dual PCM Interface, 2x32 bits, 192 kHz M/S, I2S
 - Three stereo PDM I/O for digital microphones
 - Single S/PDIF analog/digital stereo I/O

- Dual 16-bit timer, triple PWM timer, 32-bit capture timer, dual watchdog timer, 32-bit real time clock
- Radio transceiver
 - Modulation types and Receiver sensitivities:
 - GFSK (-95 dBm), DBPSK (-98 dBm),
 - DQPSK (-94 dBm), D8PSK (-89 dBm)
 - Zero Blind Slot capable with prolonged preamble
 - Integrated RFPA up to 12 dBm output power
 - Integrated Fast Antenna Diversity
- VFBGA-116 Package, 0.5 mm pitch, 7 × 7 mm

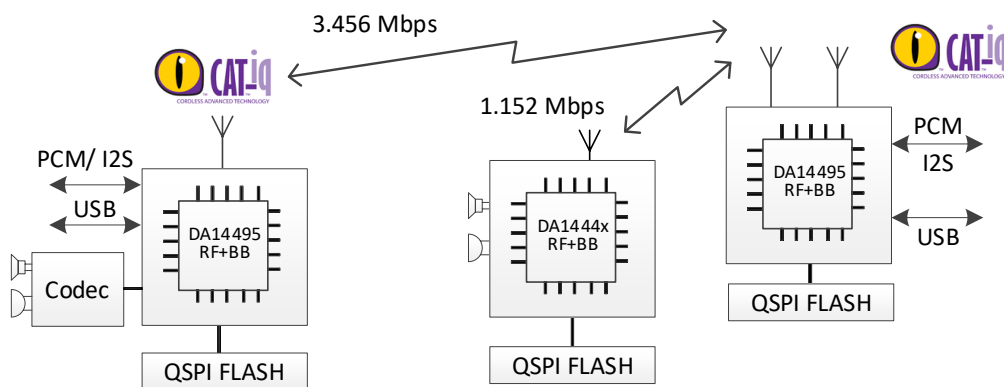


Figure 1. System diagram

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1. Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60% RH before the solder reflow process.

The VFBGA packages are qualified for MSL 3.

Table 1. MSL classification

MSL level	Floor lifetime
MSL 3	168 hours
MSL 1	Unlimited at 30 °C/85% RH

1.1 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from <http://www.jedec.org>.

2. Package Outline Drawings

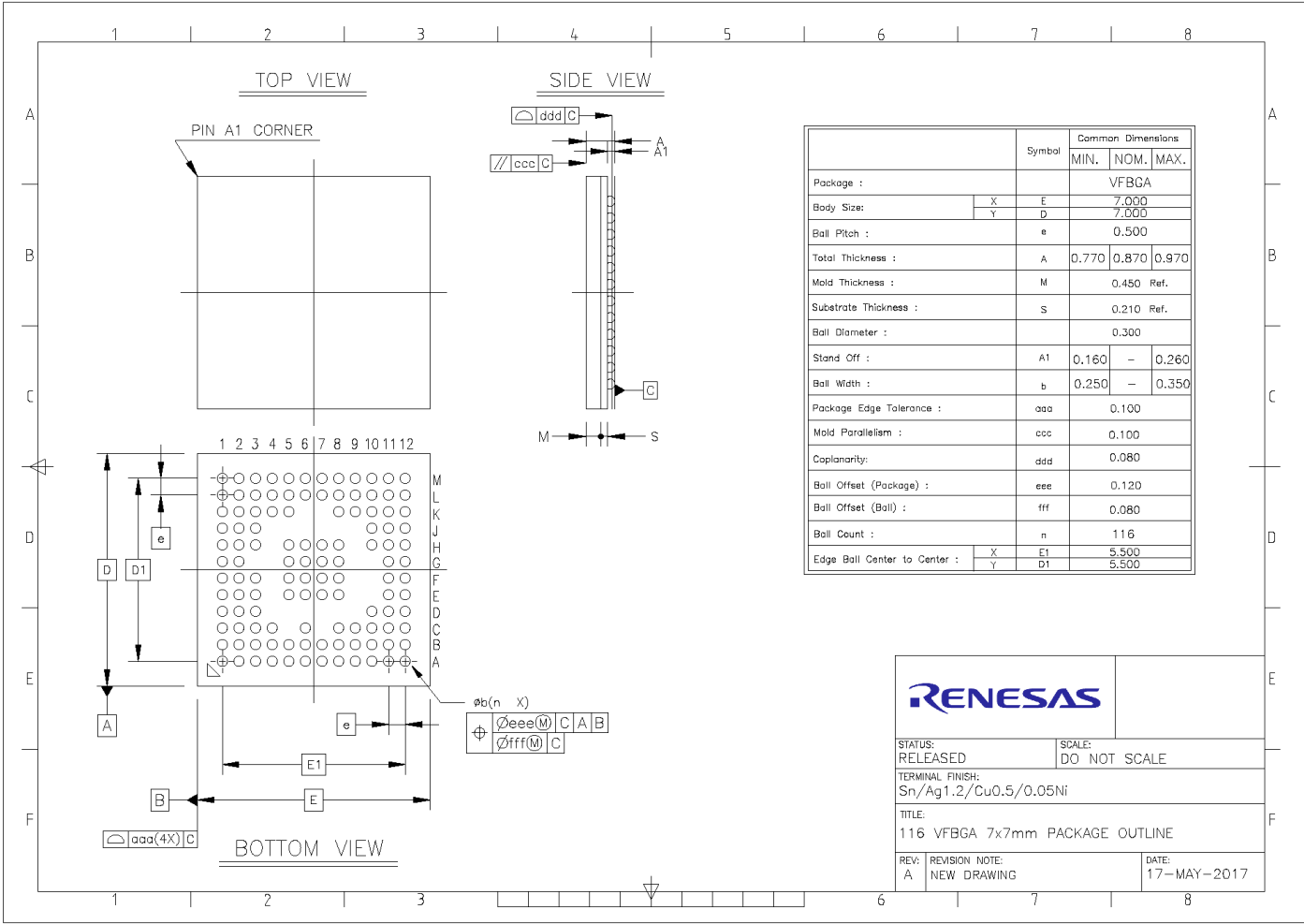


Figure 2. VFBGA 116 package outline drawing

3. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas local sales representative.

Table 2. Ordering information (samples)

Part number	Package	Size (mm)	Shipment form	Pack quantities
DA14495-00HP2	VFBGA116	7 × 7 × 0.87	Reel	100/1000
DA14495-00D01HP2	VFBGA116	7 × 7 × 0.87	Reel	100/1000
DA14495-00R01HP2	VFBGA116	7 × 7 × 0.87	Reel	100/1000

Table 3. Ordering information (production)

Part number	Package	Size (mm)	Shipment form	Pack quantities
DA14495-00HP2	VFBGA116	7 × 7 × 0.87	Reel	3000
DA14495-00D01HP2	VFBGA116	7 × 7 × 0.87	Reel	3000
DA14495-00R01HP2	VFBGA116	7 × 7 × 0.87	Reel	3000
DA14495-00S01HP2	VFBGA116	7 × 7 × 0.87	Reel	3000
DA14495-00S02HP2	VFBGA116	7 × 7 × 0.87	Reel	3000

Part number legend:

DA14495 RR[XXX]YYZ

RR: Chip Revision Number

XXX: Optional Family derivative

D01: Active Noise Canceling (ANC) enabled

R01: RTX low latency Sheersound CODEC enabled

S01: Custom

S02: Custom

YY: Package code

Z: Shipment code

Marking code

DA14495RR[XXX]

4. Revision History

Revision	Date	Description
01.00	June 19, 2024	First release.

RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.