

RC313xx

VersaClock 8 Programmable Synthesizer / Jitter Attenuator Family

Description

The RC313xx (RC31312, RC31309) is a high-performance jitter attenuator, universal-frequency-translator, and clock synthesizer. The device is comprised of a fractional-N digital PLL (DPLL) to track CLKIN inputs, an Analog PLL (APLL) for synthesis, three independent low-phase noise fractional output dividers (FOD), and seven Integer Output Dividers (IOD).

Applications

- High-performance computing
- AI accelerators
- Enterprise storage
- Switches and routers

Features

- 156.25MHz Phase Jitter (12kHz-20MHz) 102fs RMS (typical)
- PCIe Gen7 CC jitter: 10fs RMS (maximum)

- PCIe® Common Clock (CC) and Independent Reference clock (IR) support
- 8kHz to 200MHz LVCMOS outputs
- 8kHz to 650MHz LP-HCSL outputs
- Simple AC-coupling to LVDS, LVPECL and CML
- CLKINs support LVCMOS, CML, LVDS, HCSL, and LVPECL input types
- Programmable General Purpose Inputs (GPI × 4) and General Purpose Input/Outputs (GPIO × 5)
- I²C, SMBus, or SPI serial interface support
- Configuration via factory-programmed One-Time Programmable (OTP) memory, serial interface or external I²C EEPROM
- Internal OTP holds up to 18 configurations
- 1V, 1.8V, 2.5V, and 3.3V LVCMOS outputs
- 1.8V, 2.5V, 3.3V, -40° to +105°C operation
- RC31312 – 12 LP-HCSL / 10 LVCMOS output pairs
 - 6 × 6 mm 48-QFN
- RC31309 – 9 LP-HCSL / 8 LVCMOS output pairs
 - 5 × 5 mm 40-QFN

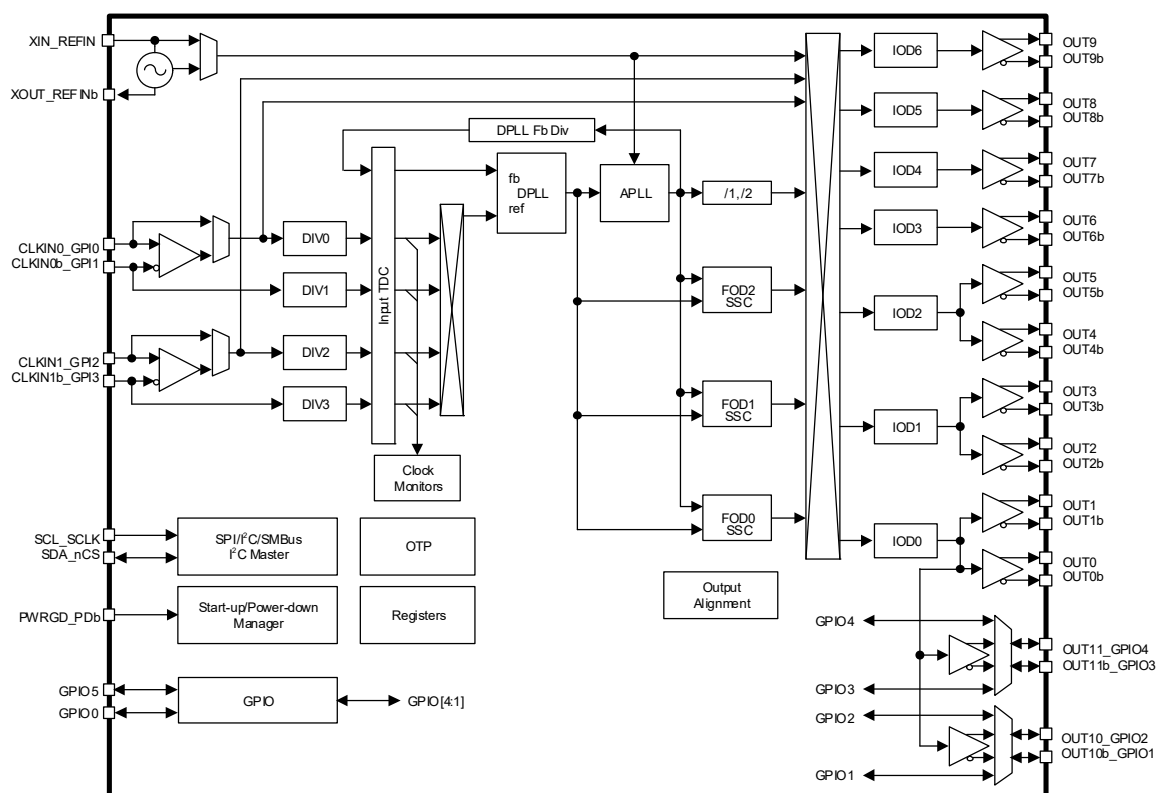


Figure 1. RC313xx Block Diagram

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