

RG5C172C0C0GBX
DDR5 Clock Driver

Description

The RG5C172C0C0GBX(CKD) is a clock driver used on DDR5 UDIMMs and SODIMMs. Its primary function is to buffer the DDR clock between the host controller and the DRAMs.

The RG5C172C0C0GBX operates in one of three modes: Single PLL, with one input clock pair active; Dual PLL, with two input clock pairs active; and Bypass, where each input clock pair can drive two output clock pairs without a PLL.

The following block diagram shows the RG5C172C0C0GBX.

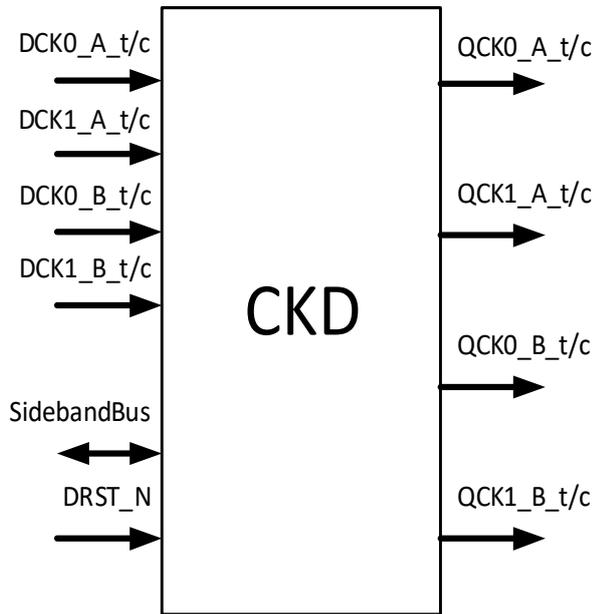
Features

- Clock rates up to 3600MHz
- Supports power-down modes to conserve power
- Provides access to internal control words for configuring device features and adapting to different U/SODIMM and system applications
- I²C/I³C Basic sideband access for asynchronous control
- Package: 2.3 mm x 5.8 mm 35-FCBGA
- Dual Sideband Bus addresses
- Four clock inputs for legacy bypass mode support

Typical Applications

- UDIMM and SODIMM for Clients

Block Diagram



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