RG5R188B0AIGBY
DDR5 Multiplex Registering Clock Driver

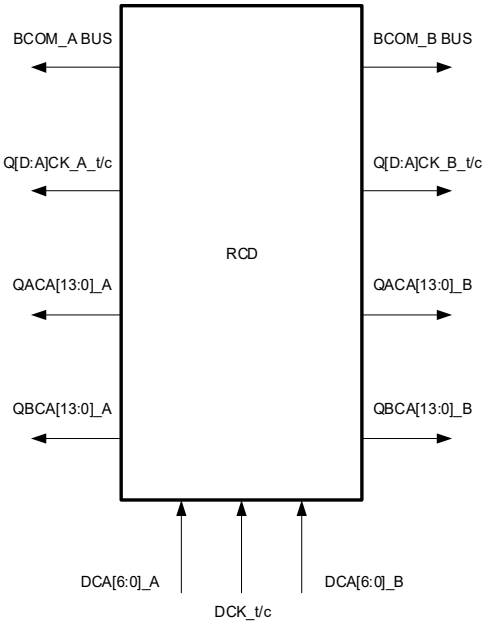
Description

The DDR5 MRCD is a registering clock driver used on DDR5 MRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the Host Controller and the DRAMs. It also creates a BCOM bus which control the data buffers.

The RG5R188B0AIGBY contains two separate channels with some common logic such as clocking, but which otherwise operate independently of each other. For each channel, the Host interface is a 7-bit + parity CA bus with two chip-select inputs. It is double data rate, carries two multiplexed pseudo-channels which can operate in the same direction simultaneously, and runs at twice the frequency of the DRAM interfaces. The MRCD demultiplexes the pseudo-channels and transmits each to a separate DRAM output interface. Each DRAM interface is a 14-bit single data rate CA bus output with a chip-select. The MRCD also transcodes commands from the CA bus onto a per-channel BCOM bus for Data Buffer control.

The RG5R188B0AIGBY has a common clock input and PLL, but produces 4 separate clock pairs to the DRAM channels.

Block Diagram



Applications

- MRDIMM modules for Enterprise Servers

Features

- DDR5 MR server speeds up to 8800MT/s
- Supports powerdown modes to conserve server power
- Supports 1 or 2 ranks per Pseudo-channel in both x4 and x8 mode
- Supports SDP, DDP, 3DS DRAM types
- Provides access to internal control words for configuring device features and adapting to different system applications
- I^2C/I3C sideband access for asynchronous register access control
- BCOM data buffer control
- Loopback and pass-through modes
- Package: 8.7 × 13.5 mm, 240-FCCSP

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