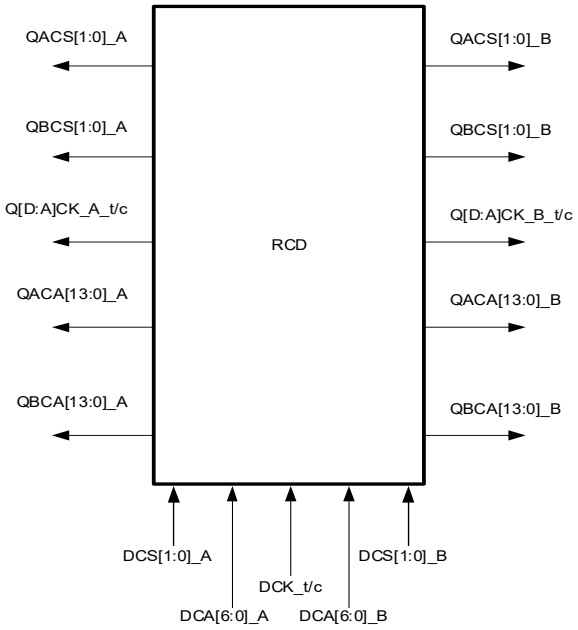
RRG5004x-A00

Gen-4 DDR5 Registering Clock Driver

The RRG5004x-A00 is a registering clock driver used on DDR5 RDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the Host Controller and the DRAMs.

The RRG5004x-A00 contains two separate channels which have some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip select inputs, and produces two copies of 14-bit single data rate CA bus outputs, and two copies of the chip select outputs. The RCD has a common clock input and PLL, but produces four separate clock pairs to the DRAM channels.

Block Diagram



Features

- Pinout optimized for DDR5 RDIMM PCB layout
- DDR5 server speeds up to 7200MT/s
- Supports power-down modes to conserve server power
- Supports 1-rank/2-rank DIMM configurations
- Supports SDP, DDP, 3DS DRAM types
- Provides access to internal control words for configuring device features and adapting to different RDIMM system applications
- I^2C and I3C SideBand access for asynchronous register access control
- Loopback and pass-through modes
- Package: 8.7 × 13.5 mm, 240-FCCSP

Applications

- RDIMM modules for Enterprise Servers
- Memory down server motherboards

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