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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0150A/E	Rev.	1.00
Title	Addition of Clock restriction for CANFD		Information Category	Technical Notification		
Applicable Product	RA6M5 Group	Lot No. All	Reference Document	RA6M5 Group User's Manual Hardware Rev 1.40		

The following Clock restriction for CANFD is added.

32.1.2 Clock restriction

For the CAN communication the following restriction for the clocks should be satisfied:

- PCLKA / 2 = PCLKB ≥ CANFDCLK
- PCLKA / 2 = PCLKB ≥ CANMCLK

To avoid missing events the CAN engine clock (CANFDCLK or CANMCLK) frequency must be less than the PCLKB clock frequency.

To avoid loss of CAN message, the PCLKB should be set to a clock with a frequency depend on the CAN communication Baud Rate. The constraint of a baud rate and a PCLKB clock is shown in Table 32.2.

Table 32.2 Clock restriction

	Baud rate	PCLKB
CANFD	1Mbps Nominal 8Mbps Data*1	PCLKB ≥ 32MHz
	1Mbps Nominal 5Mbps Data*1	PCLKB ≥ 28MHz
	1Mbps Nominal 2Mbps Data	PCLKB ≥ 20MHz
Classical CAN	1Mbps Data	PCLKB ≥ 16MHz

Note 1. The bit rate for communications depends on the board design and external environment. Determine it following sufficient evaluation.

The frequency of CANFD and CANMCLK depend on the required baud rate. For information how to configure the baud rate, refer to section 32.4.1.3. Baud Rate.