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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0153A/E	Rev.	1.00
Title	Update of Secure Cryptographic Engine event		Information Category	Technical Notification		
Applicable Product	Each Group of RA4M1, RA4M2, RA4M3, RA4W1, RA6M1, RA6M2, RA6M3, RA6M4, RA6M5, RA6T1, RA6T2	Lot No. All	Reference Document	Refer the table 1		

Table 1 Reference Document List

No	Reference Document Name	Rev	Document Control Number
1	RA4M1 Group User's Manual Hardware	1.10	R01UH0887EJ0110
2	RA4M2 Group User's Manual Hardware	1.40	R01UH0892EJ0140
3	RA4M3 Group User's Manual Hardware	1.50	R01UH0893EJ0150
4	RA4W1 Group User's Manual Hardware	1.00	R01UH0883EU0100
5	RA6M1 Group User's Manual Hardware	1.20	R01UH0884EJ0120
6	RA6M2 Group User's Manual Hardware	1.20	R01UH0885EJ0120
7	RA6M3 Group User's Manual Hardware	1.20	R01UH0886EJ0120
8	RA6M4 Group User's Manual Hardware	1.50	R01UH0890EJ0150
9	RA6M5 Group User's Manual Hardware	1.40	R01UH0891EJ0140
10	RA6T1 Group User's Manual Hardware	1.20	R01UH0897EU0120
11	RA6T2 Group User's Manual Hardware	1.40	R01UH0951EJ0140

The following Secure Cryptographic Engine event (SCE_TADI) is added.

1. The changes to the RA4M1 microcontroller group are as follows.

＜Current description＞ Page 245

Table 13.4 Event table (5 of 5)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC		
0A8h	SCI9	SCI9_RXI	✓	✓	✓	-	-
0A9h		SCI9_TXI	✓	✓	✓	-	-
0AAh		SCI9_TEI	✓	-	-	-	-
0ABh		SCI9_ERI	✓	-	-	-	-
0ACh		SCI9_AM	✓	-	-	-	-
0ADh	SPI0	SPI0_SPRI	✓	✓	✓	-	-
0AEh		SPI0_SPTI	✓	✓	✓	-	-
0AFh		SPI0_SPII	✓	-	-	-	-
0B0h		SPI0_SPEI	✓	-	-	-	-
0B1h		SPI0_SPTEND	✓	-	-	-	-
0B2h	SPI1	SPI1_SPRI	✓	✓	✓	-	-
0B3h		SPI1_SPTI	✓	✓	✓	-	-
0B4h		SPI1_SPII	✓	-	-	-	-
0B5h		SPI1_SPEI	✓	-	-	-	-
0B6h		SPI1_SPTEND	✓	-	-	-	-

Note 1. Only supported when KRCTL.KRMD = 1.
Note 2. Only the first edge detection is valid.
Note 3. Only interrupts after DTC transfer are supported.
Note 4. Using SELSR0.

＜Current description＞ Page 1305

Table 46.1 SCE5 specifications

Item	Description
Access control	Access management circuit • In case of irregular access to the SCE5 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE5.

<Changed description>

Table 13.4 Event table (5 of 5)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC		
0A8h	SCI9	SCI9_RXI	✓	✓	✓	-	-
0A9h		SCI9_TXI	✓	✓	✓	-	-
0AAh		SCI9_TEI	✓	-	-	-	-
0ABh		SCI9_ERI	✓	-	-	-	-
0ACh		SCI9_AM	✓	-	-	-	-
0ADh	SPI0	SPI0_SPRI	✓	✓	✓	-	-
0AEh		SPI0_SPTI	✓	✓	✓	-	-
0AFh		SPI0_SPII	✓	-	-	-	-
0B0h		SPI0_SPEI	✓	-	-	-	-
0B1h		SPI0_SPTEND	✓	-	-	-	-
0B2h	SPI1	SPI1_SPRI	✓	✓	✓	-	-
0B3h		SPI1_SPTI	✓	✓	✓	-	-
0B4h		SPI1_SPII	✓	-	-	-	-
0B5h		SPI1_SPEI	✓	-	-	-	-
0B6h		SPI1_SPTEND	✓	-	-	-	-
0DBh	SCE5	SCE_TADI	✓	-	-	-	-

Note 1. Only supported when KRCTL.KRMD = 1.
Note 2. Only the first edge detection is valid.
Note 3. Only interrupts after DTC transfer are supported.
Note 4. Using SELSR0.

Table 46.1 SCE5 specifications

Item	Description
Access control	Access management circuit • In case of irregular access to the SCE5 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE5. Interrupt SCE_TADI is generated in response.

2. The changes to the RA4M2 microcontroller group are as follows.

＜Current description＞ Page 276

Table 13.4 Event table (7 of 7)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x1C0	SCIX1*5	SCIX1_SCIX0	✓	—	—	—	—	—
0x1C1		SCIX1_SCIX1	✓	—	—	—	—	—
0x1C2		SCIX1_SCIX2	✓	—	—	—	—	—
0x1C3		SCIX1_SCIX3	✓	—	—	—	—	—
0x1C4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1C5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1C6		SPI0_SPII	✓	—	—	—	—	—
0x1C7		SPI0_SPEI	✓	—	—	—	—	—
0x1C8		SPI0_SPCEND	✓	—	—	—	—	—
0x1DA	QSPI	QSPI_INTR	✓	—	—	—	—	—
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*3	—	—

Note 1. Only the first edge detection is valid.
Note 2. Only interrupts after DTC transfer are supported.
Note 3. Using SELSR0.
Note 4. SCIX0_SCIXn (n = 0 to 3) links to extended serial interface of SCI1.
Note 5. SCIX1_SCIXn (n = 0 to 3) links to extended serial interface of SCI2.

＜Current description＞ Page 1362

Table 36.1 SCE9 specifications (1 of 2)

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE9 due to a tampered program or CPU runaway, this circuit blocks all subsequent accesses and stops data output from the SCE9

＜Changed description＞

Table 13.4 Event table (7 of 7)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x1C0	SCIX1*5	SCIX1_SCIX0	✓	—	—	—	—	—
0x1C1		SCIX1_SCIX1	✓	—	—	—	—	—
0x1C2		SCIX1_SCIX2	✓	—	—	—	—	—
0x1C3		SCIX1_SCIX3	✓	—	—	—	—	—
0x1C4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1C5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1C6		SPI0_SPII	✓	—	—	—	—	—
0x1C7		SPI0_SPEI	✓	—	—	—	—	—
0x1C8		SPI0_SPCEND	✓	—	—	—	—	—
0x1DA	QSPI	QSPI_INTR	✓	—	—	—	—	—
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*3	—	—
0x1E9	SCE9	SCE_TADI	✓	—	—	—	—	—

Note 1. Only the first edge detection is valid.
Note 2. Only interrupts after DTC transfer are supported.
Note 3. Using SELSR0.
Note 4. SCIX0_SCIXn (n = 0 to 3) links to extended serial interface of SCI1.
Note 5. SCIX1_SCIXn (n = 0 to 3) links to extended serial interface of SCI2.

Table 36.1 SCE9 specifications (1 of 2)

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE9 due to a tampered program or CPU runaway, this circuit blocks all subsequent accesses and stops data output from the SCE9. Interrupt SCE_TADI is generated in response.

3. The changes to the RA4M3 microcontroller group are as follows.

＜Current description＞ Page 279

Table 13.4 Event table (7 of 7)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x1C4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1C5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1C6		SPI0_SPII	✓	—	—	—	—	—
0x1C7		SPI0_SPEI	✓	—	—	—	—	—
0x1C8		SPI0_SPCEND	✓	—	—	—	—	—
0x1DA	QSPI	QSPI_INTR	✓	—	—	—	—	—
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*3	—	—

Note 1. Only the first edge detection is valid.
Note 2. Only interrupts after DTC transfer are supported.
Note 3. Using SELSR0.
Note 4. SCIX0_SCIXn (n = 0 to 3) links to extended serial interface of SCI1.
Note 5. SCIX1_SCIXn (n = 0 to 3) links to extended serial interface of SCI2.

＜Current description＞ Page 1380

Table 36.1 SCE9 specifications (1 of 2)

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE9 due to a tampered program or CPU runaway, this circuit blocks all subsequent accesses and stops data output from the SCE9

＜Changed description＞

Table 13.4 Event table (7 of 7)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x1C4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1C5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1C6		SPI0_SPII	✓	—	—	—	—	—
0x1C7		SPI0_SPEI	✓	—	—	—	—	—
0x1C8		SPI0_SPCEND	✓	—	—	—	—	—
0x1DA	QSPI	QSPI_INTR	✓	—	—	—	—	—
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*3	—	—
0x1E9	SCE9	SCE_TADI	✓	—	—	—	—	—

Note 1. Only the first edge detection is valid.
Note 2. Only interrupts after DTC transfer are supported.
Note 3. Using SELSR0.
Note 4. SCIX0_SCIXn (n = 0 to 3) links to extended serial interface of SCI1.
Note 5. SCIX1_SCIXn (n = 0 to 3) links to extended serial interface of SCI2.

Table 36.1 SCE9 specifications (1 of 2)

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE9 due to a tampered program or CPU runaway, this circuit blocks all subsequent accesses and stops data output from the SCE9. Interrupt SCE_TADI is generated in response.

4. The changes to the RA4W1 microcontroller group are as follows.

＜Current description＞ Page 228

Table 14.4 Event table (4 of 4)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC		
09Bh	GPT168	GPT8_CCMPA	✓	✓	✓		
09Ch		GPT8_CCMPB	✓	✓	✓		
09Dh		GPT8_CMPC	✓	✓	✓		
09Eh		GPT8_CMPD	✓	✓	✓		
09Fh		GPT8_CMPE	✓	✓	✓		
0A0h		GPT8_CMPF	✓	✓	✓		
0A1h		GPT8_OVF	✓	✓	✓		
0A2h		GPT8_UDF	✓	✓	✓		
0ABh	GPT	GPT_UVWEDGE	✓				
0ACh	SCI0	SCI0_RXI	✓	✓	✓		
0ADh		SCI0_TXI	✓	✓	✓		
0AEh		SCI0_TEI	✓				
0AFh		SCI0_ERI	✓				
0B0h		SCI0_AM	✓			✓*4	
0B1h		SCI0_RXI_OR_ERI				✓*4	
0B2h	SCI1	SCI1_RXI	✓	✓	✓		
0B3h		SCI1_TXI	✓	✓	✓		
0B4h		SCI1_TEI	✓				
0B5h		SCI1_ERI	✓				
0B6h		SCI1_AM	✓				
0C1h	SCI4	SCI4_RXI	✓	✓	✓		
0C2h		SCI4_TXI	✓	✓	✓		
0C3h		SCI4_TEI	✓				
0C4h		SCI4_ERI	✓				
0C5h		SCI4_AM	✓				
0C6h	SCI9	SCI9_RXI	✓	✓	✓		
0C7h		SCI9_TXI	✓	✓	✓		
0C8h		SCI9_TEI	✓				
0C9h		SCI9_ERI	✓				
0CAh		SCI9_AM	✓				
0CBh	SPI0	SPI0_SPRI	✓	✓	✓		
0CCh		SPI0_SPTI	✓	✓	✓		
0CDh		SPI0_SPII	✓				
0CEh		SPI0_SPEI	✓				
0CFh		SPI0_SPTEND	✓				
0D0h	SPI1	SPI1_SPRI	✓	✓	✓		
0D1h		SPI1_SPTI	✓	✓	✓		
0D2h		SPI1_SPII	✓				
0D3h		SPI1_SPEI	✓				
0D4h		SPI1_SPTEND	✓				

Note 1. Only supported when KRCTL.KRMD = 1.
Note 2. Only the first edge detection is valid.
Note 3. Only interrupts after DTC transfer are supported.
Note 4. Using SELSR0.
Note 5. The Bluetooth middleware executes processing in response to BLEIRQ. Do not use this source.

＜Current description＞ Page 1192

Table 45.1 SCE5 specifications

Item	Description
Access control	Access management circuit • In case of irregular access to the SCE5 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE5.

＜Changed description＞

Table 14.4 Event table (4 of 4)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC		
09Bh	GPT168	GPT8_CCMPA	✓	✓	✓		
09Ch		GPT8_CCMPB	✓	✓	✓		
09Dh		GPT8_CMPC	✓	✓	✓		
09Eh		GPT8_CMPD	✓	✓	✓		
09Fh		GPT8_CMPE	✓	✓	✓		
0A0h		GPT8_CMPF	✓	✓	✓		
0A1h		GPT8_OVF	✓	✓	✓		
0A2h		GPT8_UDF	✓	✓	✓		
0ABh	GPT	GPT_UVWEDGE	✓				
0ACh	SCI0	SCI0_RXI	✓	✓	✓		
0ADh		SCI0_TXI	✓	✓	✓		
0AEh		SCI0_TEI	✓				
0AFh		SCI0_ERI	✓				
0B0h		SCI0_AM	✓			✓*4	
0B1h		SCI0_RXI_OR_ERI				✓*4	
0B2h	SCI1	SCI1_RXI	✓	✓	✓		
0B3h		SCI1_TXI	✓	✓	✓		
0B4h		SCI1_TEI	✓				
0B5h		SCI1_ERI	✓				
0B6h		SCI1_AM	✓				
0B8h	SCE5	SCE_TADI	✓				
0C1h	SCI4	SCI4_RXI	✓	✓	✓		
0C2h		SCI4_TXI	✓	✓	✓		
0C3h		SCI4_TEI	✓				
0C4h		SCI4_ERI	✓				
0C5h		SCI4_AM	✓				
0C6h	SCI9	SCI9_RXI	✓	✓	✓		
0C7h		SCI9_TXI	✓	✓	✓		
0C8h		SCI9_TEI	✓				
0C9h		SCI9_ERI	✓				
0CAh		SCI9_AM	✓				
0CBh	SPI0	SPI0_SPRI	✓	✓	✓		
0CCh		SPI0_SPTI	✓	✓	✓		
0CDh		SPI0_SPII	✓				
0CEh		SPI0_SPEI	✓				
0CFh		SPI0_SPTEND	✓				
0D0h	SPI1	SPI1_SPRI	✓	✓	✓		
0D1h		SPI1_SPTI	✓	✓	✓		
0D2h		SPI1_SPII	✓				
0D3h		SPI1_SPEI	✓				
0D4h		SPI1_SPTEND	✓				

Note 1. Only supported when KRCTL.KRMD = 1.
Note 2. Only the first edge detection is valid.
Note 3. Only interrupts after DTC transfer are supported.
Note 4. Using SELSR0.
Note 5. The Bluetooth middleware executes processing in response to BLEIRQ. Do not use this source.

Table 45.1 SCE5 specifications

Item	Description
Access control	Access management circuit • In case of irregular access to the SCE5 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE5. Interrupt SCE_TADI is generated in response.

5. The changes to the RA6M1 microcontroller group are as follows.

＜Current description＞ Page 260

Table 14.4 Event table (7 of 7)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
18Ch	SCI4	SCI4_RXI	✓	✓	✓	-	-	-
18Dh		SCI4_TXI	✓	✓	✓	-	-	-
18Eh		SCI4_TEI	✓	-	-	-	-	-
18Fh		SCI4_ERI	✓	-	-	-	-	-
190h		SCI4_AM	✓	-	-	-	-	-
1A4h	SCI8	SCI8_RXI	✓	✓	✓	-	-	-
1A5h		SCI8_TXI	✓	✓	✓	-	-	-
1A6h		SCI8_TEI	✓	-	-	-	-	-
1A7h		SCI8_ERI	✓	-	-	-	-	-
1A8h		SCI8_AM	✓	-	-	-	-	-
1AAh	SCI9	SCI9_RXI	✓	✓	✓	-	-	-
1ABh		SCI9_TXI	✓	✓	✓	-	-	-
1ACh		SCI9_TEI	✓	-	-	-	-	-
1ADh		SCI9_ERI	✓	-	-	-	-	-
1AEh		SCI9_AM	✓	-	-	-	-	-
1BCh	SPI0	SPI0_SPRI	✓	✓	✓	-	-	-
1BDh		SPI0_SPTI	✓	✓	✓	-	-	-
1BEh		SPI0_SPII	✓	-	-	-	-	-
1BFh		SPI0_SPEI	✓	-	-	-	-	-
1C0h		SPI0_SPTEND	✓	-	-	-	-	-
1C1h	SPI1	SPI1_SPRI	✓	✓	✓	-	-	-
1C2h		SPI1_SPTI	✓	✓	✓	-	-	-
1C3h		SPI1_SPII	✓	-	-	-	-	-
1C4h		SPI1_SPEI	✓	-	-	-	-	-
1C5h		SPI1_SPTEND	✓	-	-	-	-	-
1C6h	QSPI	QSPI_INTR	✓	-	-	-	-	-
1C7h	SDHI0	SDHI_MMC0_ACCS	✓	-	-	-	-	-
1C8h		SDHI_MMC0_SDIO	✓	-	-	-	-	-
1C9h		SDHI_MMC0_CARD	✓	-	-	-	-	-
1CAh		SDHI_MMC0_ODMSDBREQ	-	✓	✓	-	-	-
1CBh	SDHI1	SDHI_MMC1_ACCS	✓	-	-	-	-	-
1CCh		SDHI_MMC1_SDIO	✓	-	-	-	-	-
1CDh		SDHI_MMC1_CARD	✓	-	-	-	-	-
1CEh		SDHI_MMC1_ODMSDBREQ	-	✓	✓	-	-	-

Note 1. Only supported when CMPCTL.CSTEN = 1.
Note 2. Only supported when KRCTL.KRMD = 1.
Note 3. Only the first edge detection is valid.
Note 4. Only interrupts after DTC transfer are supported.
Note 5. Using SELSR0.

＜Current description＞ Page 1282

Table 41.1 SCE7 specifications (1 of 2)

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE7 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE7.

＜Changed description＞

Table 14.4 Event table (7 of 7)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
18Ch	SCI4	SCI4_RXI	✓	✓	✓	-	-	-
18Dh		SCI4_TXI	✓	✓	✓	-	-	-
18Eh		SCI4_TEI	✓	-	-	-	-	-
18Fh		SCI4_ERI	✓	-	-	-	-	-
190h		SCI4_AM	✓	-	-	-	-	-
1A4h	SCI8	SCI8_RXI	✓	✓	✓	-	-	-
1A5h		SCI8_TXI	✓	✓	✓	-	-	-
1A6h		SCI8_TEI	✓	-	-	-	-	-
1A7h		SCI8_ERI	✓	-	-	-	-	-
1A8h		SCI8_AM	✓	-	-	-	-	-
1AAh	SCI9	SCI9_RXI	✓	✓	✓	-	-	-
1ABh		SCI9_TXI	✓	✓	✓	-	-	-
1ACh		SCI9_TEI	✓	-	-	-	-	-
1ADh		SCI9_ERI	✓	-	-	-	-	-
1AEh		SCI9_AM	✓	-	-	-	-	-
1BCh	SPI0	SPI0_SPRI	✓	✓	✓	-	-	-
1BDh		SPI0_SPTI	✓	✓	✓	-	-	-
1BEh		SPI0_SPII	✓	-	-	-	-	-
1BFh		SPI0_SPEI	✓	-	-	-	-	-
1C0h		SPI0_SPTEND	✓	-	-	-	-	-
1C1h	SPI1	SPI1_SPRI	✓	✓	✓	-	-	-
1C2h		SPI1_SPTI	✓	✓	✓	-	-	-
1C3h		SPI1_SPII	✓	-	-	-	-	-
1C4h		SPI1_SPEI	✓	-	-	-	-	-
1C5h		SPI1_SPTEND	✓	-	-	-	-	-
1C6h	QSPI	QSPI_INTR	✓	-	-	-	-	-
1C7h	SDHI0	SDHI_MMC0_ACCS	✓	-	-	-	-	-
1C8h		SDHI_MMC0_SDIO	✓	-	-	-	-	-
1C9h		SDHI_MMC0_CARD	✓	-	-	-	-	-
1CAh		SDHI_MMC0_ODMSDBREQ	-	✓	✓	-	-	-
1CBh	SDHI1	SDHI_MMC1_ACCS	✓	-	-	-	-	-
1CCh		SDHI_MMC1_SDIO	✓	-	-	-	-	-
1CDh		SDHI_MMC1_CARD	✓	-	-	-	-	-
1CEh		SDHI_MMC1_ODMSDBREQ	-	✓	✓	-	-	-
1E2h	SCE7	SCE_TADI	✓	-	-	-	-	-

Note 1. Only supported when CMPCTL.CSTEN = 1.
Note 2. Only supported when KRCTL.KRMD = 1.
Note 3. Only the first edge detection is valid.
Note 4. Only interrupts after DTC transfer are supported.
Note 5. Using SELSR0.

Table 41.1 SCE7 specifications (1 of 2)

Item	Description
Access control	Access management circuit • In case of irregular access to the SCE7 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE7. Interrupt SCE_TADI is generated in response.

6. The changes to the RA6M2 microcontroller group are as follows.

＜Current description＞ Page 203

Table 10.4 Event table (8 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
19Eh	SCI7	SCI7_RXI	✓	✓	✓	-	-	-
19Fh		SCI7_TXI	✓	✓	✓	-	-	-
1A0h		SCI7_TEI	✓	-	-	-	-	-
1A1h		SCI7_ERI	✓	-	-	-	-	-
1A2h		SCI7_AM	✓	-	-	-	-	-
1A4h	SCI8	SCI8_RXI	✓	✓	✓	-	-	-
1A5h		SCI8_TXI	✓	✓	✓	-	-	-
1A6h		SCI8_TEI	✓	-	-	-	-	-
1A7h		SCI8_ERI	✓	-	-	-	-	-
1A8h		SCI8_AM	✓	-	-	-	-	-
1AAh	SCI9	SCI9_RXI	✓	✓	✓	-	-	-
1ABh		SCI9_TXI	✓	✓	✓	-	-	-
1ACh		SCI9_TEI	✓	-	-	-	-	-
1ADh		SCI9_ERI	✓	-	-	-	-	-
1AEh		SCI9_AM	✓	-	-	-	-	-
1BCh	SPI0	SPI0_SPRI	✓	✓	✓	-	-	-
1BDh		SPI0_SPTI	✓	✓	✓	-	-	-
1BEh		SPI0_SPII	✓	-	-	-	-	-
1BFh		SPI0_SPEI	✓	-	-	-	-	-
1C0h		SPI0_SPTEND	✓	-	-	-	-	-
1C1h	SPI1	SPI1_SPRI	✓	✓	✓	-	-	-
1C2h		SPI1_SPTI	✓	✓	✓	-	-	-
1C3h		SPI1_SPII	✓	-	-	-	-	-
1C4h		SPI1_SPEI	✓	-	-	-	-	-
1C5h		SPI1_SPTEND	✓	-	-	-	-	-
1C6h	QSPI	QSPI_INTR	✓	-	-	-	-	-
1C7h	SDHI0	SDHI_MMC0_ACCS	✓	-	-	-	-	-
1C8h		SDHI_MMC0_SDIO	✓	-	-	-	-	-
1C9h		SDHI_MMC0_CARD	✓	-	-	-	-	-
1CAh		SDHI_MMC0_ODMSDBREQ	-	✓	✓	-	-	-
1CBh	SDHI1	SDHI_MMC1_ACCS	✓	-	-	-	-	-
1CCh		SDHI_MMC1_SDIO	✓	-	-	-	-	-
1CDh		SDHI_MMC1_CARD	✓	-	-	-	-	-
1CEh		SDHI_MMC1_ODMSDBREQ	-	✓	✓	-	-	-

Note 1. Only supported when CMPCTL.CSTEN = 1.
Note 2. Only supported when KRCTL.KRMD = 1.
Note 3. Only the first edge detection is valid.
Note 4. Only interrupts after DTC transfer are supported.
Note 5. Using SELSR0.

＜Current description＞ Page 1432

Table 44.1 SCE7 specifications (1 of 2)

Parameter	Description
Access control	Access management circuit • In case of irregular access to the SCE7 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE7.

＜Changed description＞

Table 10.4 Event table (8 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
19Eh	SCI7	SCI7_RXI	✓	✓	✓	-	-	-
19Fh		SCI7_TXI	✓	✓	✓	-	-	-
1A0h		SCI7_TEI	✓	-	-	-	-	-
1A1h		SCI7_ERI	✓	-	-	-	-	-
1A2h		SCI7_AM	✓	-	-	-	-	-
1A4h	SCI8	SCI8_RXI	✓	✓	✓	-	-	-
1A5h		SCI8_TXI	✓	✓	✓	-	-	-
1A6h		SCI8_TEI	✓	-	-	-	-	-
1A7h		SCI8_ERI	✓	-	-	-	-	-
1A8h		SCI8_AM	✓	-	-	-	-	-
1AAh	SCI9	SCI9_RXI	✓	✓	✓	-	-	-
1ABh		SCI9_TXI	✓	✓	✓	-	-	-
1ACh		SCI9_TEI	✓	-	-	-	-	-
1ADh		SCI9_ERI	✓	-	-	-	-	-
1AEh		SCI9_AM	✓	-	-	-	-	-
1BCh	SPI0	SPI0_SPRI	✓	✓	✓	-	-	-
1BDh		SPI0_SPTI	✓	✓	✓	-	-	-
1BEh		SPI0_SPII	✓	-	-	-	-	-
1BFh		SPI0_SPEI	✓	-	-	-	-	-
1C0h		SPI0_SPTEND	✓	-	-	-	-	-
1C1h	SPI1	SPI1_SPRI	✓	✓	✓	-	-	-
1C2h		SPI1_SPTI	✓	✓	✓	-	-	-
1C3h		SPI1_SPII	✓	-	-	-	-	-
1C4h		SPI1_SPEI	✓	-	-	-	-	-
1C5h		SPI1_SPTEND	✓	-	-	-	-	-
1C6h	QSPI	QSPI_INTR	✓	-	-	-	-	-
1C7h	SDHI0	SDHI_MMC0_ACCS	✓	-	-	-	-	-
1C8h		SDHI_MMC0_SDIO	✓	-	-	-	-	-
1C9h		SDHI_MMC0_CARD	✓	-	-	-	-	-
1CAh		SDHI_MMC0_ODMSDBREQ	-	✓	✓	-	-	-
1CBh	SDHI1	SDHI_MMC1_ACCS	✓	-	-	-	-	-
1CCh		SDHI_MMC1_SDIO	✓	-	-	-	-	-
1CDh		SDHI_MMC1_CARD	✓	-	-	-	-	-
1CEh		SDHI_MMC1_ODMSDBREQ	-	✓	✓	-	-	-
1E2h	SCE7	SCE_TADI	✓	-	-	-	-	-

Note 1. Only supported when CMPCTL.CSTEN = 1.
Note 2. Only supported when KRCTL.KRMD = 1.
Note 3. Only the first edge detection is valid.
Note 4. Only interrupts after DTC transfer are supported.
Note 5. Using SELSR0.

Table 44.1 SCE7 specifications (1 of 2)

Item	Description
Access control	Access management circuit • In case of irregular access to the SCE7 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE7. Interrupt SCE_TADI is generated in response.

7. The changes to the RA6M3 microcontroller group are as follows.

＜Current description＞ Page 286

Table 14.4 Event table (9 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
1CBh	SDHI1	SDHI_MMC1_ACCS	✓	-	-	-	-	-
1CCh		SDHI_MMC1_SDIO	✓	-	-	-	-	-
1CDh		SDHI_MMC1_CARD	✓	-	-	-	-	-
1CEh		SDHI_MMC1_ODMSDBREQ	-	✓	✓	-	-	-
1FAh	GLCDC	GLCDC_VPOS	✓	-	-	-	-	-
1FBh		GLCDC_L1UNDF	✓	-	-	-	-	-
1FCh		GLCDC_L2UNDF	✓	-	-	-	-	-
1FDh	DRW	DRW_IRQ	✓	-	-	-	-	-
1FEh	JPEG	JPEG_JEDI	✓	-	-	-	-	-
1FFh		JPEG_JDTI	✓	-	-	-	-	-

Note 1. Only supported when CMPCTL.CSTEN = 1.
Note 2. Only supported when KRCTL.KRMD = 1.
Note 3. Only the first edge detection is valid.
Note 4. Only interrupts after DTC transfer are supported.
Note 5. Using SELSR0.

＜Current description＞ Page 1678

Table 46.1 SCE7 specifications (1 of 2)

Parameter	Description
Access control	Access management circuit • In case of irregular access to the SCE7 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent access and stops the output of data from the SCE7.

<Changed description>

Table 14.4 Event table (9 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
1CBh	SDHI1	SDHI_MMC1_ACCS	✓	-	-	-	-	-
1CCh		SDHI_MMC1_SDIO	✓	-	-	-	-	-
1CDh		SDHI_MMC1_CARD	✓	-	-	-	-	-
1CEh		SDHI_MMC1_ODMSDBREQ	-	✓	✓	-	-	-
1E2h	SCE7	SCE_TADI	✓	-	-	-	-	-
1FAh	GLCDC	GLCDC_VPOS	✓	-	-	-	-	-
1FBh		GLCDC_L1UNDF	✓	-	-	-	-	-
1FCh		GLCDC_L2UNDF	✓	-	-	-	-	-
1FDh	DRW	DRW_IRQ	✓	-	-	-	-	-
1FEh	JPEG	JPEG_JEDI	✓	-	-	-	-	-
1FFh		JPEG_JDTI	✓	-	-	-	-	-

Note 1. Only supported when CMPCTL.CSTEN = 1.
Note 2. Only supported when KRCTL.KRMD = 1.
Note 3. Only the first edge detection is valid.
Note 4. Only interrupts after DTC transfer are supported.
Note 5. Using SELSR0.

Table 46.1 SCE7 specifications (1 of 2)

Item	Description
Access control	Access management circuit • In case of irregular access to the SCE7 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE7. Interrupt SCE_TADI is generated in response.

8. The changes to the RA6M4 microcontroller group are as follows.

＜Current description＞ Page 294

Table 13.4 Event table (8 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x1C0	SCIX1*5	SCIX1_SCIX0	✓	—	—	—	—	—
0x1C1		SCIX1_SCIX1	✓	—	—	—	—	—
0x1C2		SCIX1_SCIX2	✓	—	—	—	—	—
0x1C3		SCIX1_SCIX3	✓	—	—	—	—	—
0x1C4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1C5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1C6		SPI0_SPII	✓	—	—	—	—	—
0x1C7		SPI0_SPEI	✓	—	—	—	—	—
0x1C8		SPI0_SPCEND	✓	—	—	—	—	—
0x1C9	SPI1	SPI1_SPRI	✓	✓	✓	—	—	—
0x1CA		SPI1_SPTI	✓	✓	✓	—	—	—
0x1CB		SPI1_SPII	✓	—	—	—	—	—
0x1CC		SPI1_SPEI	✓	—	—	—	—	—
0x1CD		SPI1_SPCEND	✓	—	—	—	—	—
0x1D9	OSPI	OSPI_INTR	✓	—	—	—	—	—
0x1DA	QSPI	QSPI_INTR	✓	—	—	—	—	—
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*3	—	—

Note 1. Only the first edge detection is valid.
Note 2. Only interrupts after DTC transfer are supported.
Note 3. Using SELSR0.
Note 4. SCIX0_SCIXn (n = 0 to 3) links to extended serial interface of SCI1.
Note 5. SCIX1_SCIXn (n = 0 to 3) links to extended serial interface of SCI2.

＜Current description＞ Page 1544

Table 39.1 SCE9 specifications (1 of 2)

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE9 due to a tampered program or CPU runaway, this circuit blocks all subsequent accesses and stops data output from the SCE9

＜Changed description＞

Table 13.4 Event table (8 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x1C0	SCIX1*5	SCIX1_SCIX0	✓	—	—	—	—	—
0x1C1		SCIX1_SCIX1	✓	—	—	—	—	—
0x1C2		SCIX1_SCIX2	✓	—	—	—	—	—
0x1C3		SCIX1_SCIX3	✓	—	—	—	—	—
0x1C4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1C5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1C6		SPI0_SPII	✓	—	—	—	—	—
0x1C7		SPI0_SPEI	✓	—	—	—	—	—
0x1C8		SPI0_SPCEND	✓	—	—	—	—	—
0x1C9	SPI1	SPI1_SPRI	✓	✓	✓	—	—	—
0x1CA		SPI1_SPTI	✓	✓	✓	—	—	—
0x1CB		SPI1_SPII	✓	—	—	—	—	—
0x1CC		SPI1_SPEI	✓	—	—	—	—	—
0x1CD		SPI1_SPCEND	✓	—	—	—	—	—
0x1D9	OSPI	OSPI_INTR	✓	—	—	—	—	—
0x1DA	QSPI	QSPI_INTR	✓	—	—	—	—	—
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*3	—	—
0x1E9	SCE9	SCE_TADI	✓	—	—	—	—	—

Note 1. Only the first edge detection is valid.
Note 2. Only interrupts after DTC transfer are supported.
Note 3. Using SELSR0.
Note 4. SCIX0_SCIXn (n = 0 to 3) links to extended serial interface of SCI1.
Note 5. SCIX1_SCIXn (n = 0 to 3) links to extended serial interface of SCI2.

Table 39.1 SCE9 specifications (1 of 2)

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE9 due to a tampered program or CPU runaway, this circuit blocks all subsequent accesses and stops data output from the SCE9. Interrupt SCE_TADI is generated in response.

9. The changes to the RA6M5 microcontroller group are as follows.

＜Current description＞ Page 316

Table 13.4 Event table (9 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x1C0	SCIX1*5	SCIX1_SCIX0	✓	—	—	—	—	—
0x1C1		SCIX1_SCIX1	✓	—	—	—	—	—
0x1C2		SCIX1_SCIX2	✓	—	—	—	—	—
0x1C3		SCIX1_SCIX3	✓	—	—	—	—	—
0x1C4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1C5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1C6		SPI0_SPII	✓	—	—	—	—	—
0x1C7		SPI0_SPEI	✓	—	—	—	—	—
0x1C8		SPI0_SPCEND	✓	—	—	—	—	—
0x1C9	SPI1	SPI1_SPRI	✓	✓	✓	—	—	—
0x1CA		SPI1_SPTI	✓	✓	✓	—	—	—
0x1CB		SPI1_SPII	✓	—	—	—	—	—
0x1CC		SPI1_SPEI	✓	—	—	—	—	—
0x1CD		SPI1_SPCEND	✓	—	—	—	—	—
0x1CE	CANFD ECC	CAN_AFLRAM0_ERI	✓	—	—	—	—	—
0x1CF		CAN_AFLRAM1_ERI	✓	—	—	—	—	—
0x1D0		CAN_MRAM_ERI	✓	—	—	—	—	—
0x1D9	OSPI	OSPI_INTR	✓	—	—	—	—	—
0x1DA	QSPI	QSPI_INTR	✓	—	—	—	—	—
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*3	—	—

Note 1. Only the first edge detection is valid.
Note 2. Only interrupts after DTC transfer are supported.
Note 3. Using SELSR0.
Note 4. SCIX0_SCIXn (n = 0 to 3) links to extended serial interface of SCI1.
Note 5. SCIX1_SCIXn (n = 0 to 3) links to extended serial interface of SCI2.

＜Current description＞ Page 1915

Table 42.1 SCE9 specifications (1 of 2)

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE9 due to a tampered program or CPU runaway, this circuit blocks all subsequent accesses and stops data output from the SCE9

<Changed description>

Table 13.4 Event table (9 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x1C0	SCIX1*5	SCIX1_SCIX0	✓	—	—	—	—	—
0x1C1		SCIX1_SCIX1	✓	—	—	—	—	—
0x1C2		SCIX1_SCIX2	✓	—	—	—	—	—
0x1C3		SCIX1_SCIX3	✓	—	—	—	—	—
0x1C4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1C5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1C6		SPI0_SPII	✓	—	—	—	—	—
0x1C7		SPI0_SPEI	✓	—	—	—	—	—
0x1C8		SPI0_SPCEND	✓	—	—	—	—	—
0x1C9	SPI1	SPI1_SPRI	✓	✓	✓	—	—	—
0x1CA		SPI1_SPTI	✓	✓	✓	—	—	—
0x1CB		SPI1_SPII	✓	—	—	—	—	—
0x1CC		SPI1_SPEI	✓	—	—	—	—	—
0x1CD		SPI1_SPCEND	✓	—	—	—	—	—
0x1CE	CANFD ECC	CAN_AFLRAM0_ERI	✓	—	—	—	—	—
0x1CF		CAN_AFLRAM1_ERI	✓	—	—	—	—	—
0x1D0		CAN_MRAM_ERI	✓	—	—	—	—	—
0x1D9	OSPI	OSPI_INTR	✓	—	—	—	—	—
0x1DA	QSPI	QSPI_INTR	✓	—	—	—	—	—
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*3	—	—
0x1E9	SCE9	SCE_TADI	✓	—	—	—	—	—

Note 1. Only the first edge detection is valid.
Note 2. Only interrupts after DTC transfer are supported.
Note 3. Using SELSR0.
Note 4. SCIX0_SCIXn (n = 0 to 3) links to extended serial interface of SCI1.
Note 5. SCIX1_SCIXn (n = 0 to 3) links to extended serial interface of SCI2.

Table 42.1 SCE9 specifications (1 of 2)

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE9 due to a tampered program or CPU runaway, this circuit blocks all subsequent accesses and stops data output from the SCE9. Interrupt SCE_TADI is generated in response.

10. The changes to the RA6T1 microcontroller group are as follows.

＜Current description＞ Page 227

Table 13.4 Event table (6 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
174h	SCI0	SCI0_RXI	✓	✓	✓	-	-	-
175h		SCI0_TXI	✓	✓	✓	-	-	-
176h		SCI0_TEI	✓	-	-	-	-	-
177h		SCI0_ERI	✓	-	-	-	-	-
178h		SCI0_AM	✓	-	-	✓*5	-	-
179h		SCI0_RXI_OR_ERI	-	-	-	✓*5	-	-
17Ah	SCI1	SCI1_RXI	✓	✓	✓	-	-	-
17Bh		SCI1_TXI	✓	✓	✓	-	-	-
17Ch		SCI1_TEI	✓	-	-	-	-	-
17Dh		SCI1_ERI	✓	-	-	-	-	-
17Eh		SCI1_AM	✓	-	-	-	-	-
180h	SCI2	SCI2_RXI	✓	✓	✓	-	-	-
181h		SCI2_TXI	✓	✓	✓	-	-	-
182h		SCI2_TEI	✓	-	-	-	-	-
183h		SCI2_ERI	✓	-	-	-	-	-
184h		SCI2_AM	✓	-	-	-	-	-
186h	SCI3	SCI3_RXI	✓	✓	✓	-	-	-
187h		SCI3_TXI	✓	✓	✓	-	-	-
188h		SCI3_TEI	✓	-	-	-	-	-
189h		SCI3_ERI	✓	-	-	-	-	-
18Ah		SCI3_AM	✓	-	-	-	-	-
18Ch	SCI4	SCI4_RXI	✓	✓	✓	-	-	-
18Dh		SCI4_TXI	✓	✓	✓	-	-	-
18Eh		SCI4_TEI	✓	-	-	-	-	-
18Fh		SCI4_ERI	✓	-	-	-	-	-
190h		SCI4_AM	✓	-	-	-	-	-
1A4h	SCI8	SCI8_RXI	✓	✓	✓	-	-	-
1A5h		SCI8_TXI	✓	✓	✓	-	-	-
1A6h		SCI8_TEI	✓	-	-	-	-	-
1A7h		SCI8_ERI	✓	-	-	-	-	-
1A8h		SCI8_AM	✓	-	-	-	-	-
1AAh	SCI9	SCI9_RXI	✓	✓	✓	-	-	-
1ABh		SCI9_TXI	✓	✓	✓	-	-	-
1ACh		SCI9_TEI	✓	-	-	-	-	-
1ADh		SCI9_ERI	✓	-	-	-	-	-
1AEh		SCI9_AM	✓	-	-	-	-	-
1BCh	SPI0	SPI0_SPRI	✓	✓	✓	-	-	-
1BDh		SPI0_SPTI	✓	✓	✓	-	-	-
1BEh		SPI0_SPII	✓	-	-	-	-	-
1BFh		SPI0_SPEI	✓	-	-	-	-	-
1C0h		SPI0_SPTEND	✓	-	-	-	-	-
1C1h	SPI1	SPI1_SPRI	✓	✓	✓	-	-	-
1C2h		SPI1_SPTI	✓	✓	✓	-	-	-
1C3h		SPI1_SPII	✓	-	-	-	-	-
1C4h		SPI1_SPEI	✓	-	-	-	-	-
1C5h		SPI1_SPTEND	✓	-	-	-	-	-

<Current description> Page 923

Table 34.1 SCE7 specifications (1 of 2)

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE7 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE7.

<Changed description>

Table 13.4 Event table (6 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
174h	SCI0	SCI0_RXI	✓	✓	✓	-	-	-
175h		SCI0_TXI	✓	✓	✓	-	-	-
176h		SCI0_TEI	✓	-	-	-	-	-
177h		SCI0_ERI	✓	-	-	-	-	-
178h		SCI0_AM	✓	-	-	✓*5	-	-
179h		SCI0_RXI_OR_ERI	-	-	-	✓*5	-	-
17Ah	SCI1	SCI1_RXI	✓	✓	✓	-	-	-
17Bh		SCI1_TXI	✓	✓	✓	-	-	-
17Ch		SCI1_TEI	✓	-	-	-	-	-
17Dh		SCI1_ERI	✓	-	-	-	-	-
17Eh		SCI1_AM	✓	-	-	-	-	-
180h	SCI2	SCI2_RXI	✓	✓	✓	-	-	-
181h		SCI2_TXI	✓	✓	✓	-	-	-
182h		SCI2_TEI	✓	-	-	-	-	-
183h		SCI2_ERI	✓	-	-	-	-	-
184h		SCI2_AM	✓	-	-	-	-	-
186h	SCI3	SCI3_RXI	✓	✓	✓	-	-	-
187h		SCI3_TXI	✓	✓	✓	-	-	-
188h		SCI3_TEI	✓	-	-	-	-	-
189h		SCI3_ERI	✓	-	-	-	-	-
18Ah		SCI3_AM	✓	-	-	-	-	-
18Ch	SCI4	SCI4_RXI	✓	✓	✓	-	-	-
18Dh		SCI4_TXI	✓	✓	✓	-	-	-
18Eh		SCI4_TEI	✓	-	-	-	-	-
18Fh		SCI4_ERI	✓	-	-	-	-	-
190h		SCI4_AM	✓	-	-	-	-	-
1A4h	SCI8	SCI8_RXI	✓	✓	✓	-	-	-
1A5h		SCI8_TXI	✓	✓	✓	-	-	-
1A6h		SCI8_TEI	✓	-	-	-	-	-
1A7h		SCI8_ERI	✓	-	-	-	-	-
1A8h		SCI8_AM	✓	-	-	-	-	-
1AAh	SCI9	SCI9_RXI	✓	✓	✓	-	-	-
1ABh		SCI9_TXI	✓	✓	✓	-	-	-
1ACh		SCI9_TEI	✓	-	-	-	-	-
1ADh		SCI9_ERI	✓	-	-	-	-	-
1AEh		SCI9_AM	✓	-	-	-	-	-
1BCh	SPI0	SPI0_SPRI	✓	✓	✓	-	-	-
1BDh		SPI0_SPTI	✓	✓	✓	-	-	-
1BEh		SPI0_SPII	✓	-	-	-	-	-
1BFh		SPI0_SPEI	✓	-	-	-	-	-
1C0h		SPI0_SPTEND	✓	-	-	-	-	-
1C1h	SPI1	SPI1_SPRI	✓	✓	✓	-	-	-
1C2h		SPI1_SPTI	✓	✓	✓	-	-	-
1C3h		SPI1_SPII	✓	-	-	-	-	-
1C4h		SPI1_SPEI	✓	-	-	-	-	-
1C5h		SPI1_SPTEND	✓	-	-	-	-	-
1E2h	SCE7	SCE_TADI	✓	-	-	-	-	-

Table 34.1 SCE7 specifications (1 of 2)

Item	Description
Access control	Access management circuit • In case of irregular access to the SCE7 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE7. Interrupt SCE_TADI is generated in response.

11. The changes to the RA6T2 microcontroller group are as follows.

＜Current description＞ Page 262

Table 12.4 Event table (9 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*1	—	—

Note 1. Using SELSR0.
Note 2. Only supported when KRCTL.KRMD = 1.
Note 3. Only the first edge detection is valid.
Note 4. Only interrupts after DTC transfer are supported.

＜Current description＞ Page 1414

Table 35.1 SCE5 specifications

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE5 due to a tampered program or CPU runaway, this circuit blocks all subsequent accesses and stops data output from the SCE5

＜Changed description＞

Table 12.4 Event table (9 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*1	—	—
0x1E9	SCE5	SCE_TADI	✓	—	—	—	—	—

Note 1. Using SELSR0.
Note 2. Only supported when KRCTL.KRMD = 1.
Note 3. Only the first edge detection is valid.
Note 4. Only interrupts after DTC transfer are supported.

Table 35.1 SCE5 specifications

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE5 due to a tampered program or CPU runaway, this circuit blocks all subsequent accesses and stops data output from the SCE5. Interrupt SCE_TADI is generated in response.