

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0170A/E	Rev.	1.00
Title	Correction of the description		Information Category	Technical Notification		
Applicable Product	RA8P1 Group RA8D2 Group RA8M2 Group RA8T2 Group	Lot No.	Reference Document	Refer the table at the end of this document		
		All				

This document describes a correction to the RA8P1 Group, RA8D2 Group, RA8M2 Group and RA8T2 Group User's Manual Hardware Rev1.20. Each chapter lists the product-specific number and page number for the corrections.

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1. Correction of Table 1.15 Function Comparison (1 of 2)

The LOCO in CPUs clock sources will be deleted.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/Figure No	Page	Chapter/Table/Figure No	Page	Chapter/Table/Figure No	Page	Chapter/Table/Figure No	Page
Overview	Table 1.15	83	Table 1.14	83	Table 1.14	74	Table 1.13	72

Before Correction

Parts number	R7KA8P1AxxCAC to R7JA81KxxSAJ	
System	CPUs clock sources	MOSC, SOSC, HOCO, MOCO, LOCO , PLL1P

After Correction

Parts number	R7KA8P1AxxCAC to R7JA81KxxSAJ	
System	CPUs clock sources	MOSC, SOSC, HOCO, MOCO, PLL1P

2. Correction of Figure 5.2 1MB MRAM product for Standard Product in 5.1 Address Space

The CPU0/1 will be corrected.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/Figure No	Page	Chapter/Table/Figure No	Page	Chapter/Table/Figure No	Page	Chapter/Table/Figure No	Page
Address Space	Figure 5.2	242	Figure 5.2	242	Figure 5.2	230	Figure 5.2	227

Before Correction

- Note 2. CPU0-ITCM for Secure has different addresses for CPU0 and other bus masters.
- Note 3. CPU0-DTCM for Secure has different addresses for CPU0 and other bus masters.
- Note 4. CPU1-CTCM for Secure has different addresses for CPU1 and other bus masters.
- Note 5. CPU1-STCM for Secure has different addresses for CPU1 and other bus masters.
- Note 6. CPU0-ITCM for Non-Secure has different addresses for CPU0 and other bus masters.
- Note 7. CPU0-DTCM for Non-Secure has different addresses for CPU0 and other bus masters.
- Note 8. CPU1-CTCM for Non-Secure has different addresses for CPU1 and other bus masters.
- Note 9. CPU1-STCM for Non-Secure has different addresses for CPU1 and other bus masters.

After Correction

- Note 2. CPU0-ITCM for Secure has different addresses for **CPU1** and other bus masters.
- Note 3. CPU0-DTCM for Secure has different addresses for **CPU1** and other bus masters.
- Note 4. CPU1-CTCM for Secure has different addresses for **CPU0** and other bus masters.
- Note 5. CPU1-STCM for Secure has different addresses for **CPU0** and other bus masters.
- Note 6. CPU0-ITCM for Non-Secure has different addresses for **CPU1** and other bus masters.
- Note 7. CPU0-DTCM for Non-Secure has different addresses for **CPU1** and other bus masters.
- Note 8. CPU1-CTCM for Non-Secure has different addresses for **CPU0** and other bus masters.
- Note 9. CPU1-STCM for Non-Secure has different addresses for **CPU0** and other bus masters.

3. Correction of 7.2.18 HOEMRTRKn : Hash of OEM_ROOT_PKn (n= 0 to 3)

The address will be corrected.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Option-Setting Memory	7.2.18	297	7.2.18	296	7.2.18	284	7.2.18	281

Before Correction

Address:

HOEMRTPK0: 0x02E0_7400 +0x4 × i (i = 0 to 12)

HOEMRTPK1: 0x02E0_7430 +0x4 × i (i = 0 to 12)

HOEMRTPK1: 0x02E0_7460 +0x4 × i (i = 0 to 12)

HOEMRTPK3: 0x02E0_7490 +0x4 × i (i = 0 to 12)

After Correction

Address:

HOEMRTPK0: 0x02E0_7400 +0x4 × i (i = 0 to 11)

HOEMRTPK1: 0x02E0_7430 +0x4 × i (i = 0 to 11)

HOEMRTPK2: 0x02E0_7460 +0x4 × i (i = 0 to 11)

HOEMRTPK3: 0x02E0_7490 +0x4 × i (i = 0 to 11)

4. Correction of Table 9.6 Example of the initial system clock setting procedure after reset release/after Deep Software Standby cancellation (1 of 2)

The voltage scaling setting will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Clock Generation Circuit	Table 9.6	409	Table 9.6	408	Table 9.6	394	Table 9.6	393

Before Correction

No.	Step	Description
6	Set internal clock division ratio	Set the internal clock division ratio with SCKDIVCR and SCKDIVCR2 registers.
.	.	.
.	.	.
11	End	System clock setting is completed.

When the PLL1 is selected as the system clock source, additional procedure is required for procedure No.8. This additional procedure is shown in Figure 9.14. It is recommended to use software to measure the wait time. Be sure to consider the worst-case conditions to ensure that the required wait time elapses. If an interrupt is unavoidably generated during the wait time, retry the measurement after return from the interrupt.

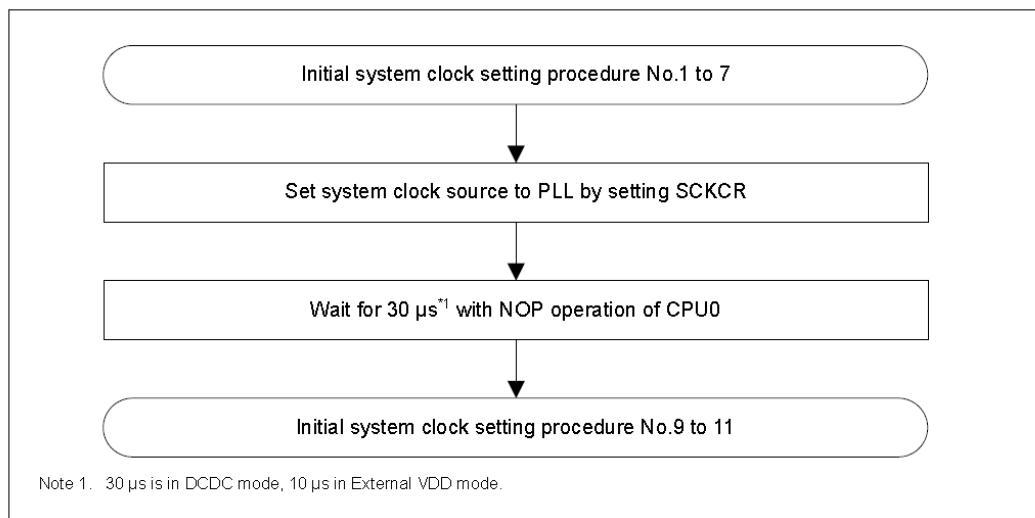


Figure 9.14 Additional flow of initial system clock setting when PLL is used for the system clock source (assuming all module stop bits are initial value)

After Correction

No.	Step	Description
6	Set voltage scaling	Set an appropriate target voltage of VDD according to the frequency of each clocks after switching the system clock. For details, see section 11, Low Power Mode.
7	Set internal clock division ratio	Set the internal clock division ratio with SCKDIVCR and SCKDIVCR2 registers.
.	.	.
.	.	.
12	End	System clock setting is completed.

When the PLL1 is selected as the system clock source, additional procedure is required for procedure No.9. This additional procedure is shown in Figure 9.14. It is recommended to use software to measure the wait time. Be sure to consider the worst-case conditions to ensure that the required wait time elapses. If an interrupt is unavoidably generated during the wait time, retry the measurement after return from the interrupt.

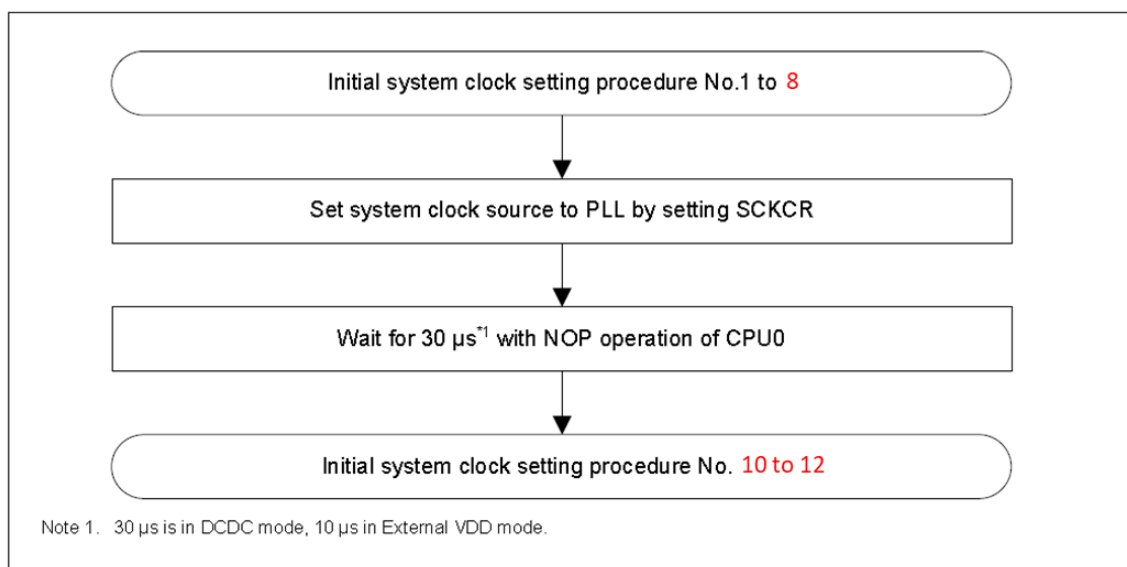


Figure 9.14 Additional flow of initial system clock setting when PLL is used for the system clock source (assuming all module stop bits are initial value)

5. Correction of Table 9.7 Example of setting procedure when changing the current system clock frequency to a faster Frequency.

The voltage scaling setting will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Clock Generation Circuit	Table 9.7	410	Table 9.7	409	Table 9.7	395	Table 9.7	394

Before Correction

No.	Step	Description
6	Set internal clock division ratio	Set the internal clock division ratio with SCKDIVCR and SCKDIVCR2 registers.
7	Switch the System Clock source*3 ·	Switch the system clock source with SCKCR register. Before switching the system clock source, confirm that the clock source oscillation is stable.
8	Change Operating Power Control Mode	Change the Operating Power Control Mode with OPCCR register. *2
10	Apply Register Write Protection	Set 0 to PRC0 bit and PRC1*1*2 bit in PRCR register
11	End	System clock is changed to a Faster frequency.

When the PLL1 is selected as the system clock source, additional procedure is required for procedure No.7. This additional procedure is shown in Figure 9.15. It is recommended to use software to measure the wait time. Be sure to consider the worst-case conditions to ensure that the required wait time elapses. If an interrupt is unavoidably generated during the wait time, retry the measurement after return from the interrupt.

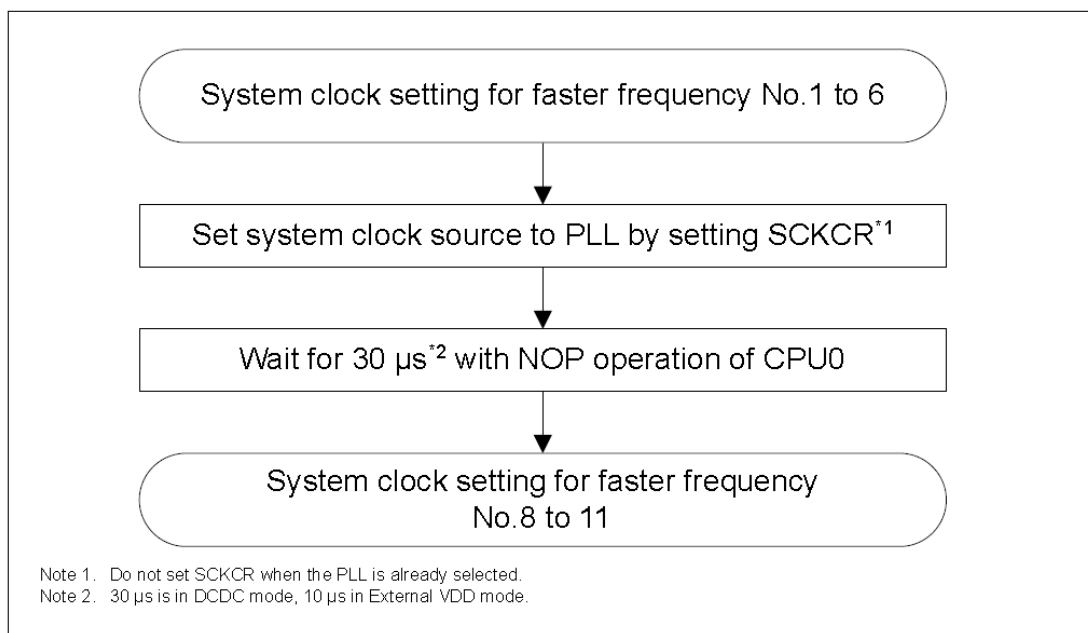


Figure 9.15 Additional flow of system clock setting when PLL is used for the system clock source and CPUCLK0 to be faster frequency

After Correction

No.	Step	Description
6	Set voltage scaling	Set an appropriate target voltage of VDD according to the frequency of each clocks after switching the system clock. For details, see section 11, Low Power Mode.
7	Set internal clock division ratio	Set the internal clock division ratio with SCKDIVCR and SCKDIVCR2 registers.
8	Switch the System Clock source*3	Switch the system clock source with SCKCR register. Before switching the system clock source, confirm that the clock source oscillation is stable.
9	Change Operating Power Control Mode	Change the Operating Power Control Mode with OPCCR register. *2
10	Apply Register Write Protection	Set 0 to PRC0 bit and PRC1*1*2 bit in PRCR register
11	End	System clock is changed to a Faster frequency.

When the PLL1 is selected as the system clock source, additional procedure is required for procedure No.8. This additional procedure is shown in Figure 9.15. It is recommended to use software to measure the wait time. Be sure to consider the worst-case conditions to ensure that the required wait time elapses. If an interrupt is unavoidably generated during the wait time, retry the measurement after return from the interrupt.

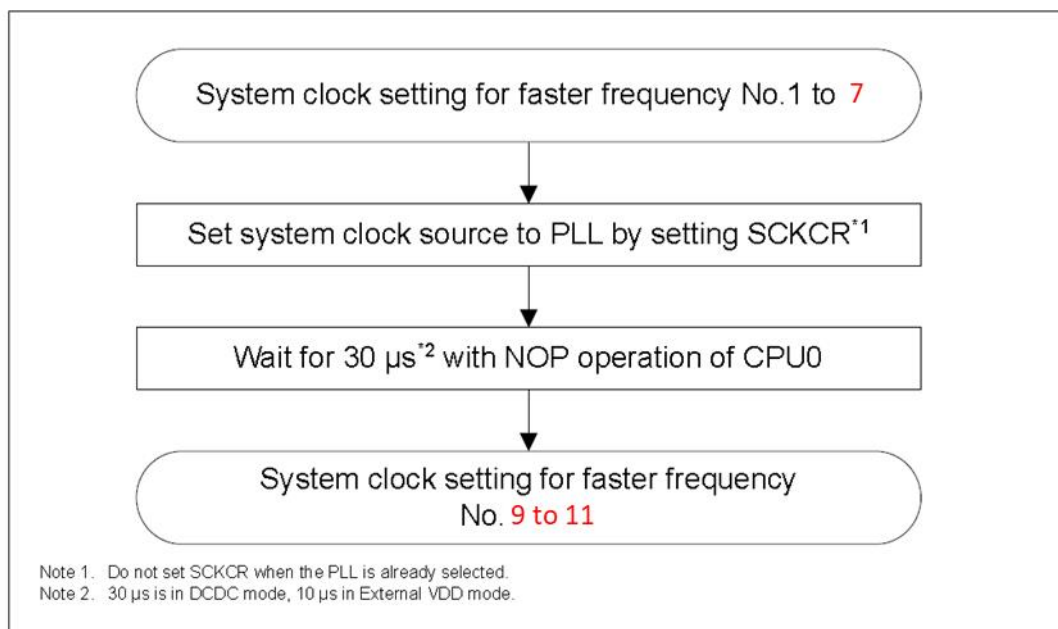


Figure 9.15 Additional flow of system clock setting when PLL is used for the system clock source and CPUCLK0 to be faster frequency

6. Correction of Table 9.8 Example of setting procedure when changing the current system clock frequency to a slower frequency (1 of 2)

The voltage scaling setting will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Clock Generation Circuit	Table 9.8	412	Table 9.8	410	Table 9.8	396	Table 9.8	395

Before Correction

No.	Step	Description
8	Set MRAM and SRAM Wait Cycle	Set an appropriate access wait count for the MRAM and SRAM according to the frequency at which it operates after the system clock (ICLK), MRICLK and MRPCLK are set. For details, see section 60, MRAM and section 59, SRAM.
.	.	.
.	.	.
11	End	System clock is changed to a Slower frequency.

When the PLL1 is selected as the system clock source, additional procedure is required before procedure No.5. This additional procedure is shown in Figure 9.16. It is recommended to use software to measure the wait time. Be sure to consider the worst-case conditions to ensure that the required wait time elapses. If an interrupt is unavoidably generated during the wait time, retry the measurement after return from the interrupt.

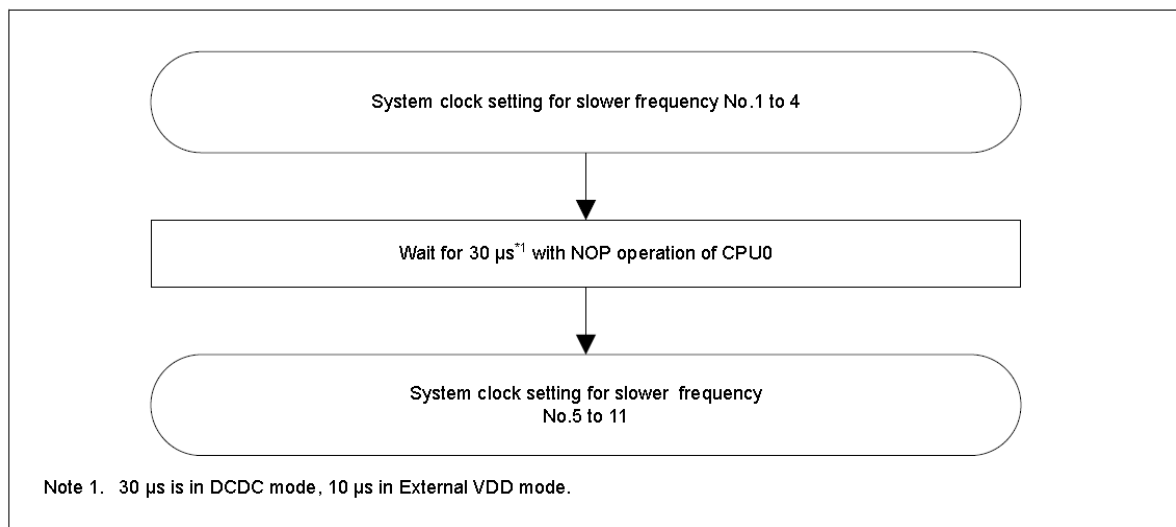


Figure 9.16 Additional flow of system clock setting when PLL is used for the system clock source and CPUCLK0 to be slower frequency

After Correction

No.	Step	Description
8	Set voltage scaling	Set an appropriate target voltage of VDD according to the frequency of each clocks after switching the system clock. For details, see section 11, Low Power Mode.
9	Set MRAM and SRAM Wait Cycle	Set an appropriate access wait count for the MRAM and SRAM according to the frequency at which it operates after the system clock (ICLK), MRICK and MRPCLK are set. For details, see section 60, MRAM and section 59, SRAM.
.	.	.
.	.	.
12	End	System clock is changed to a Slower frequency.

When the PLL1 is selected as the system clock source before switching the system clock source, additional procedure is required before procedure No.5. This additional procedure is shown in Figure 9.16. It is recommended to use software to measure the wait time. Be sure to consider the worst-case conditions to ensure that the required wait time elapses. If an interrupt is unavoidably generated during the wait time, retry the measurement after return from the interrupt.

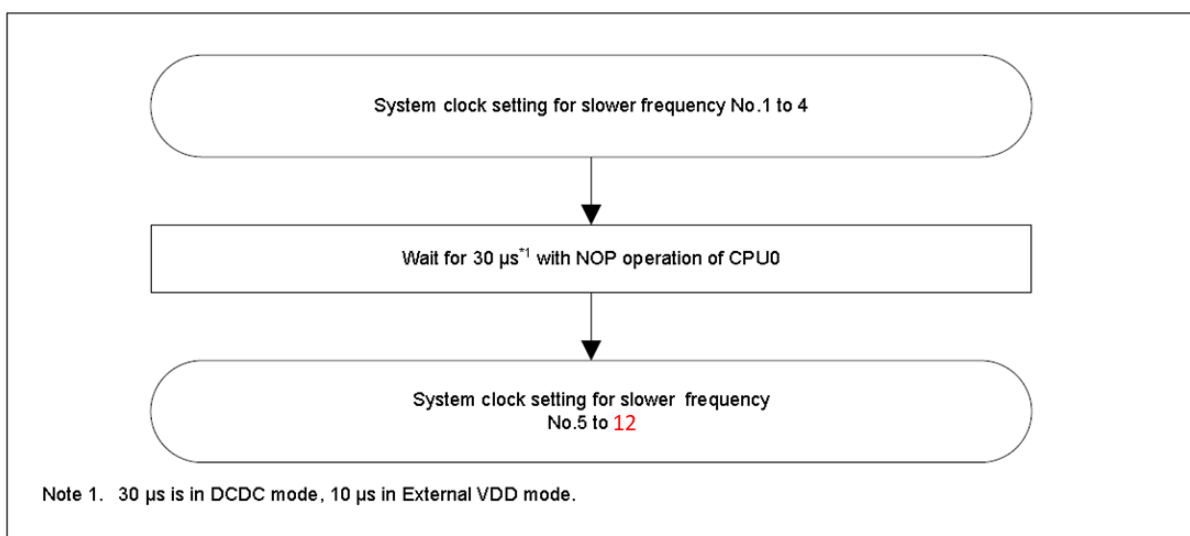


Figure 9.16 Additional flow of system clock setting when PLL is used for the system clock source and CPUCLK0 to be slower frequency

7. Correction of 11.6.2.2 Canceling Software Standby Mode

The following sentence will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Low Power Mode	11.6.2.2	485	11.6.2.2	482	11.6.2.2	467	11.6.2.2	466

7. Canceling by a temperature monitor reset

Software Standby mode is canceled by a temperature monitor reset and the MCU starts the reset exception handling.

8. Correction of 11.6.3.2 Canceling Deep Software Standby Mode

The following sentence will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Low Power Mode	11.6.3.2	487	11.6.3.2	484	11.6.3.2	469	11.6.3.2	468

7. Canceling by a temperature monitor reset

Deep Software Standby mode is canceled by a temperature monitor reset and the MCU starts the reset exception handling.

9. Correction of Table 14.5 Event List (9 of 14) (Excluding RA8T2)

The CPU Deep Sleep in table 14.5 Event List (9 of 14) will be changed.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Interrupt Controller Unit (ICU)	Table 14.5	570	Table 14.5	564	Table 14.5	549	—	—

Before Correction

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling CPU Deep Sleep	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x2C1	USBHS	USBHS_D0FIFO	✓	✓	✓	—	—	—
0x2C2		USBHS_D1FIFO	✓	✓	✓	—	—	—

After Correction

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling CPU Deep Sleep	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x2C1	USBHS	USBHS_D0FIFO	✓	✓	✓	✓	—	—
0x2C2		USBHS_D1FIFO	✓	✓	✓	✓	—	—

10. Correction of Table 15.3 Addresses assigned for each slave (2 of 2)

The typo of Table 15.3 Addresses assigned to each slave (2/2) will be revised.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Buses	Table 15.3	589	Table 15.3	584	Table 15.3	569	Table 15.3	569

Before Correction

Region	Address	Bus Interface	Area
External RAM	0x7000_0000 to 0x7FFF_FFFF	OSPI1BI*1	OSPI for SIP-Flash

Note 1. Products without SIP-FLASH can be accessed, but products with SIP-FLASH cannot.

After Correction

Region	Address	Bus Interface	Area
External RAM	0x7000_0000 to 0x7FFF_FFFF	OSPI1BI*1	OSPI (via DOTF)

Note 1. Products without SIP-FLASH can be accessed, but products with SIP-FLASH cannot.

11. Correction of 16.3.1.17 MMPUEMIPICn : MPU End Address Register for MIPI-CSI via VIN (n = 0 to 2) (RA8P1/RA8D2)

The value after reset will be revised.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Memory Protection Unit (MPU)	16.3.1.17	705	16.3.1.16	699	—	—	—	—

Before Correction

Value after reset: 0 0 0 0 0 0 0 0 0 0 0 (bit 11 to 0)

After Correction

Value after reset: 1 1 1 1 1 1 1 1 1 1 1 (bit 11 to 0)

12. Correction of 16.3.1.18 MMPUENPUn : MMPU End Address Register for NPU (n = 0 to 4) (RA8P1 only)

The value after reset will be revised.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Memory Protection Unit (MPU)	16.3.1.18	705	—	—	—	—	—	—

Before Correction

Value after reset: 0 0 0 0 0 0 0 0 0 0 0 (bit 11 to 0)

After Correction

Value after reset: 1 1 1 1 1 1 1 1 1 1 1 (bit 11 to 0)

13. Correction of Table 20.3 Association between event signal names set in ELSRn.ELS[9:0] bits and signal numbers (6 of 9)

The RSW2 will be revised to ESWM.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Event Link Controller (ELC)	Table 20.3	831	Table 19.3	824	Table 19.3	790	Table 19.3	786

Before Correction

RWS2

After Correction

ESWM

14. Correction of Table 21.9 Register settings for input/output pin function (PORT2)

The following document in Table 21.9 Register settings for input/output pin function (PORT2) will be revised.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
I/O Ports	Table 21.9	866	Table 20.9	855	Table 20.9	821	Table 20.9	817

Before Correction

PSEL[4:0] setting	Function	Pin
		P201
DSCR[1:0] bit	Drive capability control	L ^{*3}

Note 3. The driver strength of this port can not be controlled by PmnPFS.DSCR[1:0] bits.

After Correction

PSEL[4:0] setting	Function	Pin
		P201
DSCR[1:0] bit	Drive capability control	L ^{*3}

Note 3. **The driver strength of this port is controlled by PmnPFS.DSCR[1:0] bits. Set the PmnPFS.DSCR[1:0] bits to Low Drive (00b).**

15. Correction of Table 20.19 Register settings for input/output pin function (PORTC) (RA8T2 only)

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
I/O Ports	—	—	—	—	—	—	Table 20.19	826

The CRX1 will be added in PC15.

PSEL[4:0] setting	Function	Pin
10000b	CANFD	PC15 CRX1

16. Correction of 30.4.2 Precautions

The following description in 30.4.2 Precautions are corrected.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Layer 3 Ethernet Switch Module (ESWM)	30.4.2	1324	29.4.2	1312	29.4.2	1277	29.4.2	1273

Before Correction

Selection			Definition	
Local RAM size*1	Clk*1	Internal band width	Ethernet & CPU total band width	Throughput (Ether2Ether)
512 KB	320 MHz	40.9 Gbps	MAX 1G bps (Exp 100M Ether 3 port + 100M CPU 2 port) × TX/RX	800 to 1000 ns
512 KB	320 MHz	40.9 Gbps	MAX 10G bps (Exp 1G Ether 3 port + 1G CPU 2 port) × TX/RX	400 to 500 ns
512 KB	320 MHz	40.9 Gbps	MAX 25G bps (Exp 2.5G Ether 3 port + 2.5G CPU 2 port) × TX/RX	300 to 500 ns
512 KB	400 MHz	51.2 Gbps	MAX 25G bps (Exp 2.5G Ether 3 port + 2.5G CPU 2 port) × TX/RX	300 to 500 ns

Note: At the frame end (forwarding source port) - frame start (forwarding destination port). When measuring, there is no dependency on the payload length of the frame.

Note: The frame start (forwarding destination port) is up to the point where the preamble starts to output.

Note 1. Specifications less than these are prohibited.

Throughput measurement conditions:

- From frame end (forwarding source port) to frame start (forwarding destination port)
- The forwarding (destination port) is not busy
- L2 forwarding unicast (1:1 forwarding).

After Correction

Selection			Definition	
Local RAM size*1	Clk*1	Internal band width	Ethernet & CPU total band width	Throughput (Ether2Ether)
64 KB	250 MHz	32 Gbps	MAX 1G bps (Exp 100M Ether 2 port + 100M CPU 1 port) × TX/RX	800 to 2000 ns
64 KB	50 MHz	6.4 Gbps	MAX 1G bps (Exp 100M Ether 2 port + 100M CPU 1 port) × TX/RX	2000 to 6000 ns
64 KB	250 MHz	32 Gbps	MAX 3G bps (Exp 1G Ether 2 port + 1G CPU 1 port) × TX/RX	400 to 600 ns
64 KB	150 MHz	19.2 Gbps	MAX 3G bps (Exp 1G Ether 2 port + 1G CPU 1 port) × TX/RX	500 to 800 ns

Note: At the frame end (forwarding source port) - frame start (forwarding destination port). When measuring, there is no

dependency on the payload length of the frame.

Note: The frame start (forwarding destination port) is up to the point where the preamble starts to output.

Note 1. Specifications less than these are prohibited.

Throughput measurement conditions:

- From frame end (forwarding source port) to frame start (forwarding destination port)
- The forwarding (destination port) is not busy
- L2 forwarding unicast (1:1 forwarding).

17. Correction of 36.3.2.3 PTPTIVCt : Timer t Increment Value Configuration Register (t = 0, 1)

The following examples 36.3.2.3 PTPTIVCt : Timer t Increment Value Configuration Register (t = 0, 1) are corrected.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Ethernet Generic PTP Timer (GTP)	36.3.2.3	1937	35.3.2.3	1925	35.3.2.3	1890	35.3.2.3	1886

Before Correction

[Examples]

- If clk clock frequency is 50 MHz, 100 MHz, 200 MHz, 320 MHz or 400 MHz, PTPTIVCt.TIV should be respectively set to a value around 0xA000_0000, 0x5000_0000, 0x2800_0000, 0x1900_0000 or 0x1400_0000.

After Correction

[Examples]

- If clk clock frequency is 50 MHz, 100 MHz, 200 MHz or 250 MHz, PTPTIVCt.TIV should be respectively set to a value around 0xA000_0000, 0x5000_0000, 0x2800_0000 or 0x2000_0000.

18. Correction of 45.2.1.4 CMCFG0CSn : OSPI Command Map Configuration Register 0 CSn (n = 0, 1)

The explanation of ADDSIZE dependency to the ADDRPEN bit description will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Octal Serial Peripheral Interface (OSPI)	45.2.1.4	2998	44.2.1.4	2986	44.2.1.4	2952	44.2.1.4	2899

Before Correction

Bit	Symbol	Function	R/W
23:16	ADDRPEN[7:0]	Address Replace Enable These bits select the bits to replace the MSByte of system bus address in memory-mapping mode. 0: No replacement (xSPI frame address field is the same as system bus address) 1: Replacement	R/W

After Correction

Bit	Symbol	Function	R/W										
23:16	ADDRPEN[7:0]	Address Replace Enable These bits select the bits to replace the MSByte of system bus address in memory-mapping mode. 0: No replacement (xSPI frame address field is the same as system bus address) 1: Replacement	R/W										
		<table border="1"> <thead> <tr> <th>ADDSize[1:0]</th> <th>Replace target bits of system bus address</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>bit 7 to bit 0</td> </tr> <tr> <td>01</td> <td>bit 15 to bit 8</td> </tr> <tr> <td>10</td> <td>bit 23 to bit 16</td> </tr> <tr> <td>11</td> <td>bit 31 to bit 24</td> </tr> </tbody> </table>	ADDSize[1:0]	Replace target bits of system bus address	00	bit 7 to bit 0	01	bit 15 to bit 8	10	bit 23 to bit 16	11	bit 31 to bit 24	
ADDSize[1:0]	Replace target bits of system bus address												
00	bit 7 to bit 0												
01	bit 15 to bit 8												
10	bit 23 to bit 16												
11	bit 31 to bit 24												

19. Correction of 45.2.1.7 LIOCFGCSn : OSPI Link I/O Configuration Register CSn (n = 0, 1)

The description about t_{CKHDSH} will be added to DDRSMPEX bit.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Octal Serial Peripheral Interface (OSPI)	45.2.1.7	3000	44.2.1.7	2990	44.2.1.7	2955	44.2.1.7	2902

Before Correction

Bit	Symbol	Function	R/W
31:28	DDRSMPLEX[3:0]	DDR Sampling Window Extend These bits configure the cycle of extending the sampling window in DDR. In DDR, the input data is sampled during the expected cycle soon after the latency cycle. The input data out of range is ignored. It can be configured depending on the OM_DQS propagation delay. 0x0: Expand no cycle 0x1: Expand 1 cycle ⋮ 0x6: Expand 6 cycles 0x7: Expand 7 cycles Others: Setting prohibited	R/W

After Correction

Bit	Symbol	Function	R/W
31:28	DDRSMPLEX[3:0]	DDR Sampling Window Extend These bits configure the cycle of extending the sampling window in DDR. In DDR, the input data is sampled during the expected cycle soon after the latency cycle. The input data out of range is ignored. It can be configured depending on the OM_DQS propagation delay. These bits setting should be set to satisfy t_{CKHDSH} in section 70.3.11 OSPI Timing. t_{CKHDSH} means the output delay time of the external memory. For example, the DDRSMPEX[3:0] bits are set to 0x1 in the following conditions. <ul style="list-style-type: none"> • VCC is 2.7 V or above • OM_n_SCLK is 133 MHz • Memory output delay time (t_{CKHDSH}) is 6 ns The maximum allowable t_{CKHDSH} value is: t_{PERIOD} × (1 + DDRSMPEX[3:0]) - 8.5 = 7.5 × (1 + 1) - 8.5 = 6.5[ns] The memory output delay time should be less than this value. 0x0: Expand no cycle 0x1: Expand 1 cycle ⋮ 0x6: Expand 6 cycles 0x7: Expand 7 cycles Others: Setting prohibited	R/W

20. Addition of 45.2.2.22 RACTL : OSPI Register Access Control Register

The register which allows access to MER register will be added for SiP products.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Octal Serial Peripheral Interface (OSPI)	45.2.2.22	—	44.2.2.22	—	44.2.2.22	—	44.2.2.22	—

Base address: $OSPI_n_B = 0x4026_8000 + 0x0400 \times n$ ($n = 0, 1$)
 $OSPI_n_B_NS = 0x5026_8000 + 0x0400 \times n$ ($n = 0, 1$)
 Offset address: 0x208

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15
Bit field	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	2	3	2	1	0
Bit field	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RAEN
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RAEN	Register Access Enable 0: Disable MER register access 1: Enable MER register access	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: S-TYPE-3, P-TYPE-3

21. Addition of 45.2.2.23 MER : OSPI Map End Replace Register

The following register will be added for setting of SiP product configuration.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Octal Serial Peripheral Interface (OSPI)	45.2.2.23	—	44.2.2.23	—	44.2.2.23	—	44.2.2.23	—

Base address: $OSPI_n_B = 0x4026_8000 + 0x0400 \times n$ ($n = 0, 1$)
 $OSPI_n_B_NS = 0x5026_8000 + 0x0400 \times n$ ($n = 0, 1$)
 Offset address: 0x228

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field	—	—	—	—	MECS1								—	—	—	MERCS1
Value after reset	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
11:4	—	These bits are read as 1. The write value should be 1.	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
16	MERCS1	Map End Replace CS1 Enable 0: No replacement 1: Replacement	R/W
19:17	–	These bits are read as 0. The write value should be 0.	R/W
27:20	MECS1	Map End CS1 Replace Address The bit27 to bit20 of system bus address is replaced with this value when MERCS1 is set to 1.	R/W
31:28	–	These bits are read as 0. The write value should be 0.	R/W

Note: S-TYPE-3, P-TYPE-3

For SiP product, the MER register should be set as described in section 45.4, SiP Product Configuration. For standard product, do not change the value after reset.

22. Correction of 45.4 SiP Product Configuration

Some steps for setting the SiP memory area will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Octal Serial Peripheral Interface (OSPI)	45.4	3051	44.4	3039	44.4	3004	44.4	2950

Before Correction

The following settings should be set before accessing the SiP Flash memory.

- The OM_1_DQS, OM_1_SIO7 to OM_1_SIO0 and OM_1_ECSINT1 pins are pull-up by PmnPFS.PCR bit before PmnPFS.PMR bit is set to 1.
- The LVOCR.LVO1E bit is set to 1.

After Correction

The following settings should be set before accessing the SiP Flash memory.

- Set OSPI (11100b) to the PmnPFS.PSEL[4:0] bits of P603 to P607 and PC00 to PC07
- Set the LVOCR.LVO1E bit to 1
- Set the PSARB.PSARB17 bit to 0 unless whole SiP Flash area is marked as Non-secure
- Set the end address of CS1
 - Set the RACTL.RAEN bit to 1
 - Set the MER register to 0x0871_0FF0 for 8 MB SiP-Flash product
 - Set the MER register to 0x0831_0FF0 for 4 MB SiP-Flash product
 - Set the RACTL.RAEN bit to 0
- Set the LIOCFGCS1.DDRSMPEX[3:0] bits

The t_{CKHDSH} value of SiP Flash memory is t_{PERIOD}/2 + 6[ns]. When OM1_SCLK is 133 MHz, the DDRSMPEX[3:0] bits should be 0x2.

23. Correction of 45.5.4 Memory Write Combination Mode

Memory Write Combination Mode is restricted to CPU0 only (CPU1 is not included).

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Octal Serial Peripheral Interface (OSPI)	45.5.4	3053	44.5.4	3041	44.5.4	3005	44.5.4	2952

Before Correction

When BMCFGCHn.MWRCOMB = 1, the memory write combination mode is enabled. However, the combination does not work if the bus master is CPU and OSPI data is under 32 bits. Table 45.11 shows the possibility of a data write for each bus master.

Table 45.11 Data write possibility for each bus master

Bus master	Combination enable	Combination disable
CPU under 32-bit access	Not possible	Possible
CPU 64-bit access	Possible	Possible
DMAC/DTC	Possible	Possible
EDMAC	Possible	Possible
CEU	Possible	Possible
DRW	Possible	Possible

After Correction

45.5.4 Memory Write Combination Mode

When BMCFGCHn.MWRCOMB = 1, the memory write combination mode is enabled. However, the combination does not work if the bus master is **CPU0** and OSPI data is under 32 bits. Table 45.11 shows the possibility of a data write for each bus master.

Table 45.11 Data write possibility for each bus master

Bus master	Combination enable	Combination disable
CPU0 under 32-bit access	Not possible	Possible
CPU0 64-bit access	Possible	Possible
Other bus masters	Possible	Possible

24. Correction of 47.2.1 SSICR : Control Register (Excluding RA8T2)

The following description will be revised.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Serial Sound Interface Enhanced (SSIE)	47.2.1	3063	46.2.1	3052	46.2.1	3015	—	—

Before Correction

Communication format (SSIOFR.OMOD[1:0])			
FRM[1:0]	I ² S (00b)	Monaural (10b)	TDM (01b)
00b	2	1	Setting prohibited
01b	Setting prohibited	Setting prohibited	4
10b			5
11b			6

After Correction

Communication format (SSIOFR.OMOD[1:0])			
FRM[1:0]	I ² S (00b)	Monaural (10b)	TDM (01b)
00b	2	1	Setting prohibited
01b	Setting prohibited	Setting prohibited	4
10b			6
11b			8

25. Correction of Table 50.5 Guaranteed clock frequency and clock mode (Excluding RA8T2)

The max frequency for PCLK will be revised.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Pulse Density Modulation Interface (PDM-IF)	Table 50.5	3236	Table 49.5	3224	Table 49.5	3187	—	—

Before Correction

PDMIFCLK	PCLK	PDM_CLKn		
Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Supported core clock Division ratio	Setting value (PDSFCR.CKDIV[3:0])
8	1 to 100 ^{*1}	4	2	0x0
		2	4	0x1
		.	.	.
		.	.	.
		0.25	32	0xF

Note 1. PDM-IF is possible to operate at PCLK below 1 MHz but the guaranteed frequency operation range is 1 to 100 MHz.

After Correction

PDMIFCLK	PCLK	PDM_CLKn		
Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Supported core clock Division ratio	Setting value (PDSFCR.CKDIV[3:0])
8	1 to 62.5 ^{*1}	4	2	0x0
		2	4	0x1
		.	.	.
		.	.	.
		0.25	32	0xF

Note 1. PDM-IF is possible to operate at PCLK below 1 MHz but the guaranteed frequency operation range is 1 to 62.5 MHz.

26. Addition of 50.3.1.1 Output Sampling Frequency (Excluding RA8T2)

The following sections are added to the 50.3.1 Clock Specifications section.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Pulse Density Modulation Interface (PDM-IF)	Table 50.5	3236	Table 49.5	3224	Table 49.5	3187	—	—

50.3.1.1 Output Sampling Frequency

PDM-IF output sampling frequency is shown by the following formula:

$$F_{out} = F_{clk} / (M \times 2)$$

- F_{out} : PDM-IF output sampling frequency
- F_{clk} : PDM_CLKn frequency (See Table 50.5)
- M : Sinc filter decimation ratio (PDSFCRCHn.SINCDEC[7:0] + 1)

27. Correction of Table 50.7 Sinc filter output clip (Excluding RA8T2)

PDM-IF output sampling frequency (kHz) will be added to Table 50.7.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Pulse Density Modulation Interface (PDM-IF)	Table 50.7	3239	Table 50.7	3227	Table 50.7	3190	—	—

Before Correction

Table 50.7 Sinc filter output clip (1 of 2)

PDMIFCLK (MHz)	Sinc filter order	PDMDSRCHn.SFMD[2:0]	PDM_CLK dividend ratio	PDSFCRCHn.CKDIV[3:0]	Sinc filter decimation ratio	PDSFCRCHn.SINCDEC[7:0]	Sinc filter output effective bits	Sinc filter output clipping (20 bits)	PDSFCRCHn. SINC RNG[4:0]	Resolution	PDM_CLKn frequency (MHz)	SINC filter output sampling frequency (kHz)
8	4	0x0	2	0x0	125	0x7C	b28 to b0	b28 to b9	00101	20	4.0	32
			4	0x1	62	0x3D	b24 to b0	b24 to b5	01001	20	2.0	32.26
			6	0x2	42	0x29	b22 to b0	b22 to b3	01011	20	1.33	31.75
			8	0x3	31	0x1E	b20 to b0	b20 to b1	01101	20	1.0	32.26
			10	0x4	25	0x18	b19 to b0	b19 to b0	01110	20	0.8	32
			12	0x5	21	0x14	b18 to b0	b18 to b0, 0	01111	19	0.67	31.75
			14	0x6	18	0x11	b17 to b0	b17 to b0, 00	10000	18	0.57	31.75
			16	0x7	16	0x0F	b17 to b0	b17 to b0, 00	10000	18	0.50	31.25
			18	0x8	14	0x0D	b16 to b0	b16 to b0, 000	10001	17	0.44	31.75
			20	0x9	12	0x0B	b15 to b0	b15 to b0, 0000	10010	16	0.40	33.33
			22	0xA	11	0x0A	b14 to b0	b14 to b0, 00000	10011	15	0.36	33.06
			24	0xB	10	0x09	b14 to b0	b14 to b0, 00000	10011	15	0.33	33.33
			26	0xC	9	0x08	b13 to b0	b13 to b0, 000000	10100	14	0.31	34.19

PDMIFCLK (MHz)	Sinc filter order	PDMDSRCHn.SFMD[2:0]	PDM_CLK dividend ratio	PDSFCRCHn.CKDIV[3:0]	Sinc filter decimation ratio	PDSFCRCHn.SINCDEC[7:0]	Sinc filter output effective bits	Sinc filter output clipping (20 bits)	PDSFCRCHn. SINC RNG[4:0]	Resolution	PDM_CLKn frequency (MHz)	SINC filter output sampling frequency (kHz)
8	3	0x3	28	0xD	9	0x08	b13 to b0	b13 to b0, 000000	10100	14	0.29	31.75
			30	0xE	8	0x07	b13 to b0	b13 to b0, 000000	10100	14	0.27	33.33
			32	0xF	8	0x07	b13 to b0	b13 to b0, 000000	10100	14	0.25	31.25
			2	0x0	125	0x7C	b21 to b0	b21 to b2	01100	20	4.0	32
			4	0x1	62	0x3D	b18 to b0	b18 to b0, 0	01111	19	2.0	32.26
			6	0x2	42	0x29	b17 to b0	b17 to b0, 00	10000	18	1.33	31.75
			8	0x3	31	0x1E	b15 to b0	b15 to b0, 0000	10010	16	1.0	32.26
			10	0x4	25	0x18	b14 to b0	b14 to b0, 00000	10011	15	0.8	32
			12	0x5	21	0x14	b14 to b0	b14 to b0, 00000	10011	15	0.67	31.75
			14	0x6	18	0x11	b13 to b0	b13 to b0, 000000	10100	14	0.57	31.75
			16	0x7	16	0x0F	b13 to b0	b13 to b0, 000000	10100	14	0.50	31.25
			18	0x8	14	0x0D	b12 to b0	b12 to b0, 0000000	10101	13	0.44	31.75
			20	0x9	12	0x0B	b11 to b0	b11 to b0, 00000000	10110	12	0.40	33.33
			22	0xA	11	0x0A	b11 to b0	b11 to b0, 00000000	10110	12	0.36	33.06
			24	0xB	10	0x09	b10 to b0	b10 to b0, 000000000	10111	11	0.33	33.33
26	0xC	9	0x08	b10 to b0	b10 to b0, 000000000	10111	11	0.31	34.19			
28	0xD	9	0x08	b10 to b0	b10 to b0, 000000000	10111	11	0.29	31.75			
30	0xE	8	0x07	b10 to b0	b10 to b0, 000000000	10111	11	0.27	33.33			
32	0xF	8	0x07	b10 to b0	b10 to b0, 000000000	10111	11	0.25	31.25			

Table 50.7 Sinc filter output clip (2 of 2)

PDMIFCLK (MHz)	Sinc filter order	PDMDSRCHn.SFMD[2:0]	PDM_CLK dividend ratio	PDSFCRCHn.CKDIV[3:0]	Sinc filter decimation ratio	PDSFCRCHn.SINCDEC[7:0]	Sinc filter output effective bits	Sinc filter output clipping (20 bits)	PDSFCRCHn. SINC RNG[4:0]	Resolution	PDM_CLKn frequency (MHz)	SINC filter output sampling frequency (kHz)
8	2	0x2	2	0x0	125	0x7C	b14 to b0	b14 to b0, 00000	10011	15	4.0	32
			4	0x1	62	0x3D	b12 to b0	b12 to b0, 0000000	10101	13	2.0	32.26
			6	0x2	42	0x29	b11 to b0	b11 to b0, 00000000	10110	12	1.33	31.75
			8	0x3	31	0x1E	b10 to b0	b10 to b0, 000000000	10111	11	1.0	32.26
			10	0x4	25	0x18	b10 to b0	b10 to b0, 000000000	10111	11	0.8	32
			12	0x5	21	0x14	b9 to b0	b9 to b0, 0000000000	11000	10	0.67	31.75
			14	0x6	18	0x11	b9 to b0	b9 to b0, 0000000000	11000	10	0.57	31.75
			16	0x7	16	0x0F	b9 to b0	b9 to b0, 0000000000	11000	10	0.50	31.25

PDMIFCLK (MHz)	Sinc filter order	PDMDSRCHn.SFMD[2:0]	PDM_CLK dividend ratio	PDSFCRCHn.CKDIV[3:0]	Sinc filter decimation ratio	PDSFCRCHn.SINCDEC[7:0]	Sinc filter output effective bits	Sinc filter output clipping (20 bits)	PDSFCRCHn.SINCRNG[4:0]	Resolution	PDM_CLKn frequency (MHz)	SINC filter output sampling frequency (kHz)
			18	0x8	14	0x0D	b8 to b0	b8 to b0, 000000000000	11001	9	0.44	31.75
			20	0x9	12	0x0B	b8 to b0	b8 to b0, 000000000000	11001	9	0.40	33.33
			22	0xA	11	0x0A	b7 to b0	b7 to b0, 000000000000	11010	8	0.36	33.06
			24	0xB	10	0x09	b7 to b0	b7 to b0, 000000000000	11010	8	0.33	33.33
			26	0xC	9	0x08	b7 to b0	b7 to b0, 000000000000	11010	8	0.31	34.19
			28	0xD	9	0x08	b7 to b0	b7 to b0, 000000000000	11010	8	0.29	31.75
			30	0xE	8	0x07	b7 to b0	b7 to b0, 000000000000	11010	8	0.27	33.33
			32	0xF	8	0x07	b7 to b0	b7 to b0, 000000000000	11010	8	0.25	31.25
8	1	0x1	2	0x0	125	0x7C	b7 to b0	b7 to b0, 000000000000	11010	8	4.0	32
			4	0x1	62	0x3D	b6 to b0	b6 to b0, 000000000000	11011	7	2.0	32.26
			6	0x2	42	0x29	b6 to b0	b6 to b0, 000000000000	11011	7	1.33	31.75
			8	0x3	31	0x1E	b5 to b0	b5 to b0, 000000000000	11100	6	1.0	32.26
			10	0x4	25	0x18	b5 to b0	b5 to b0, 000000000000	11100	6	0.8	32
			12	0x5	21	0x14	b5 to b0	b5 to b0, 000000000000	11100	6	0.67	31.75
			14	0x6	18	0x11	b5 to b0	b5 to b0, 000000000000	11100	6	0.57	31.75
			16	0x7	16	0x0F	b5 to b0	b5 to b0, 000000000000	11100	6	0.50	31.25
			18	0x8	14	0x0D	b4 to b0	b4 to b0, 000000000000	11101	5	0.44	31.75
			20	0x9	12	0x0B	b4 to b0	b4 to b0, 000000000000	11101	5	0.40	33.33
			22	0xA	11	0x0A	b4 to b0	b4 to b0, 000000000000	11101	5	0.36	33.06
			24	0xB	10	0x09	b4 to b0	b4 to b0, 000000000000	11101	5	0.33	33.33
			26	0xC	9	0x08	b4 to b0	b4 to b0, 000000000000	11101	5	0.31	34.19
			28	0xD	9	0x08	b4 to b0	b4 to b0, 000000000000	11101	5	0.29	31.75
			30	0xE	8	0x07	b4 to b0	b4 to b0, 000000000000	11101	5	0.27	33.33
			32	0xF	8	0x07	b4 to b0	b4 to b0, 000000000000	11101	5	0.25	31.25

After Correction

Table 50.7 Sinc filter output clip (1 of 3)

PDMIFCLK (MHz)	Sinc filter order	PDMDSRCHn.SFMD[2:0]	PDM_CLK dividend ratio	PDSFRCRChn.CKDIV[3:0]	Sinc filter decimation ratio	PDSFRCRChn.SINCDEC[7:0]	Sinc filter output effective bits	Sinc filter output clipping (20 bits)	PDSFRCRChn.SINCRNG[4:0]	Resolution	PDM_CLKn frequency (MHz)	SINC filter output sampling frequency (kHz)	PDM-IF output sampling frequency (kHz)
8	4	0x0	2	0x0	125	0x7C	b28 to b0	b28 to b9	00101	20	4.0	32	16
			4	0x1	62	0x3D	b24 to b0	b24 to b5	01001	20	2.0	32.26	16.13
			6	0x2	42	0x29	b22 to b0	b22 to b3	01011	20	1.33	31.75	15.87
			8	0x3	31	0x1E	b20 to b0	b20 to b1	01101	20	1.0	32.26	16.13
			10	0x4	25	0x18	b19 to b0	b19 to b0	01110	20	0.8	32	16
			12	0x5	21	0x14	b18 to b0	b18 to b0, 0	01111	19	0.67	31.75	15.87
			14	0x6	18	0x11	b17 to b0	b17 to b0, 00	10000	18	0.57	31.75	15.87
			16	0x7	16	0x0F	b17 to b0	b17 to b0, 00	10000	18	0.50	31.25	15.63
			18	0x8	14	0x0D	b16 to b0	b16 to b0, 000	10001	17	0.44	31.75	15.87
			20	0x9	12	0x0B	b15 to b0	b15 to b0, 0000	10010	16	0.40	33.33	16.67
			22	0xA	11	0x0A	b14 to b0	b14 to b0, 00000	10011	15	0.36	33.06	16.53
			24	0xB	10	0x09	b14 to b0	b14 to b0, 00000	10011	15	0.33	33.33	16.67
			26	0xC	9	0x08	b13 to b0	b13 to b0, 000000	10100	14	0.31	34.19	17.09
			28	0xD	9	0x08	b13 to b0	b13 to b0, 000000	10100	14	0.29	31.75	15.87
30	0xE	8	0x07	b13 to b0	b13 to b0, 000000	10100	14	0.27	33.33	16.67			
32	0xF	8	0x07	b13 to b0	b13 to b0, 000000	10100	14	0.25	31.25	15.63			
8	3	0x3	2	0x0	125	0x7C	b21 to b0	b21 to b2	01100	20	4.0	32	16
			4	0x1	62	0x3D	b18 to b0	b18 to b0, 0	01111	19	2.0	32.26	16.13
			6	0x2	42	0x29	b17 to b0	b17 to b0, 00	10000	18	1.33	31.75	15.87
			8	0x3	31	0x1E	b15 to b0	b15 to b0, 0000	10010	16	1.0	32.26	16.13
			10	0x4	25	0x18	b14 to b0	b14 to b0, 00000	10011	15	0.8	32	16
			12	0x5	21	0x14	b14 to b0	b14 to b0, 00000	10011	15	0.67	31.75	15.87
			14	0x6	18	0x11	b13 to b0	b13 to b0, 000000	10100	14	0.57	31.75	15.87
			16	0x7	16	0x0F	b13 to b0	b13 to b0, 000000	10100	14	0.50	31.25	15.63
			18	0x8	14	0x0D	b12 to b0	b12 to b0, 0000000	10101	13	0.44	31.75	15.87
			20	0x9	12	0x0B	b11 to b0	b11 to b0, 00000000	10110	12	0.40	33.33	16.67
			22	0xA	11	0x0A	b11 to b0	b11 to b0, 00000000	10110	12	0.36	33.06	16.53
			24	0xB	10	0x09	b10 to b0	b10 to b0, 000000000	10111	11	0.33	33.33	16.67
			26	0xC	9	0x08	b10 to b0	b10 to b0, 000000000	10111	11	0.31	34.19	17.09
			28	0xD	9	0x08	b10 to b0	b10 to b0, 000000000	10111	11	0.29	31.75	15.87
30	0xE	8	0x07	b10 to b0	b10 to b0, 000000000	10111	11	0.27	33.33	16.67			
32	0xF	8	0x07	b10 to b0	b10 to b0, 000000000	10111	11	0.25	31.25	15.63			

Table 50.7 Sinc filter output clip (2 of 3)

PDMIFCLK (MHz)	Sinc filter order	PDMSRCHn.SFMD[2:0]	PDM_CLK dividend ratio	PDSFRCRChn.CKDIV[3:0]	Sinc filter decimation ratio	PDSFRCRChn.SINCDEC[7:0]	Sinc filter output effective bits	Sinc filter output clipping (20 bits)	PDSFRCRChn.SINCRNG[4:0]	Resolution	PDM_CLKn frequency (MHz)	SINC filter output sampling frequency (kHz)	PDM-IF output sampling frequency (kHz)
8	2	0x2	2	0x0	125	0x7C	b14 to b0	b14 to b0, 00000	10011	15	4.0	32	16
			4	0x1	62	0x3D	b12 to b0	b12 to b0, 0000000	10101	13	2.0	32.26	16.13
			6	0x2	42	0x29	b11 to b0	b11 to b0, 00000000	10110	12	1.33	31.75	15.87
			8	0x3	31	0x1E	b10 to b0	b10 to b0, 000000000	10111	11	1.0	32.26	16.13
			10	0x4	25	0x18	b10 to b0	b10 to b0, 000000000	10111	11	0.8	32	16
			12	0x5	21	0x14	b9 to b0	b9 to b0, 0000000000	11000	10	0.67	31.75	15.87
			14	0x6	18	0x11	b9 to b0	b9 to b0, 0000000000	11000	10	0.57	31.75	15.87
			16	0x7	16	0x0F	b9 to b0	b9 to b0, 0000000000	11000	10	0.50	31.25	15.63
			18	0x8	14	0x0D	b8 to b0	b8 to b0, 00000000000	11001	9	0.44	31.75	15.87
			20	0x9	12	0x0B	b8 to b0	b8 to b0, 00000000000	11001	9	0.40	33.33	16.67
			22	0xA	11	0x0A	b7 to b0	b7 to b0, 000000000000	11010	8	0.36	33.06	16.53
			24	0xB	10	0x09	b7 to b0	b7 to b0, 000000000000	11010	8	0.33	33.33	16.67
			26	0xC	9	0x08	b7 to b0	b7 to b0, 000000000000	11010	8	0.31	34.19	17.09
			28	0xD	9	0x08	b7 to b0	b7 to b0, 000000000000	11010	8	0.29	31.75	15.87
30	0xE	8	0x07	b7 to b0	b7 to b0, 000000000000	11010	8	0.27	33.33	16.67			
32	0xF	8	0x07	b7 to b0	b7 to b0, 000000000000	11010	8	0.25	31.25	15.63			

Table 50.7 Sinc filter output clip (3 of 3)

PDMIFCLK (MHz)	Sinc filter order	PDMSRCHn.SFMD[2:0]	PDM_CLK dividend ratio	PDSFRCRChn.CKDIV[3:0]	Sinc filter decimation ratio	PDSFRCRChn.SINCDEC[7:0]	Sinc filter output effective bits	Sinc filter output clipping (20 bits)	PDSFRCRChn.SINCRNG[4:0]	Resolution	PDM_CLKn frequency (MHz)	SINC filter output sampling frequency (kHz)	PDM-IF output sampling frequency (kHz)
8	1	0x1	2	0x0	125	0x7C	b7 to b0	b7 to b0, 000000000000	11010	8	4.0	32	16
			4	0x1	62	0x3D	b6 to b0	b6 to b0, 000000000000	11011	7	2.0	32.26	16.13
			6	0x2	42	0x29	b6 to b0	b6 to b0, 000000000000	11011	7	1.33	31.75	15.87
			8	0x3	31	0x1E	b5 to b0	b5 to b0, 000000000000	11100	6	1.0	32.26	16.13
			10	0x4	25	0x18	b5 to b0	b5 to b0, 000000000000	11100	6	0.8	32	16
			12	0x5	21	0x14	b5 to b0	b5 to b0, 000000000000	11100	6	0.67	31.75	15.87
			14	0x6	18	0x11	b5 to b0	b5 to b0, 000000000000	11100	6	0.57	31.75	15.87
			16	0x7	16	0x0F	b5 to b0	b5 to b0, 000000000000	11100	6	0.50	31.25	15.63

PDMIFCLK (MHz)	Sinc filter order	PDMSRCHn.SFMD[2:0]	PDM_CLK dividend ratio	PDSFCRCHn.CKDIV[3:0]	Sinc filter decimation ratio	PDSFCRCHn.SINCDEC[7:0]	Sinc filter output effective bits	Sinc filter output clipping (20 bits)	PDSFCRCHn.SINCRNG[4:0]	Resolution	PDM_CLKn frequency (MHz)	SINC filter output sampling frequency (kHz)	PDM-IF output sampling frequency (kHz)
			18	0x8	14	0x0D	b4 to b0	b4 to b0, 0000000000000000	11101	5	0.44	31.75	15.87
			20	0x9	12	0x0B	b4 to b0	b4 to b0, 0000000000000000	11101	5	0.40	33.33	16.67
			22	0xA	11	0x0A	b4 to b0	b4 to b0, 0000000000000000	11101	5	0.36	33.06	16.53
			24	0xB	10	0x09	b4 to b0	b4 to b0, 0000000000000000	11101	5	0.33	33.33	16.67
			26	0xC	9	0x08	b4 to b0	b4 to b0, 0000000000000000	11101	5	0.31	34.19	17.09
			28	0xD	9	0x08	b4 to b0	b4 to b0, 0000000000000000	11101	5	0.29	31.75	15.87
			30	0xE	8	0x07	b4 to b0	b4 to b0, 0000000000000000	11101	5	0.27	33.33	16.67
			32	0xF	8	0x07	b4 to b0	b4 to b0, 0000000000000000	11101	5	0.25	31.25	15.63

28. Correction of Table 60.1 Specifications of MRAM (1 of 2)

The Units of programming for Code MRAM will be revised.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
MRAM	Table 60.1	3548	Table 59.1	3536	Table 59.1	3498	Table 58.1	3364

Before Correction

Item	Code MRAM	Option-setting memory in extra MRAM
Units of programming	Program data buffer: 1/2/4/8 bytes Code MRAM: 32 bytes	16 bytes

After Correction

Item	Code MRAM	Option-setting memory in extra MRAM
Units of programming	1 to 32 bytes	16 bytes

29. Correction of 60.5.2 MRCFREQ : Code MRAM Frequency Notifications Register

The following description will be revised.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
MRAM	60.5.2	3557	59.5.2	3545	59.5.2	3507	58.5.2	3373

Before Correction

MRCMHZ[9:0] ≤ 0x064: 1 wait
 0x064 < MRCMHZ[9:0] ≤ 0x0C8: 2 waits
 0x0C8 < MRCMHZ[9:0] ≤ 0x0FA: 3 waits
 Other setting is reserved.

After Correction

MRCMHZ[9:0] ≤ 0x064 (100MHz): non wait access
 0x064 (100MHz) < MRCMHZ[9:0] ≤ 0x0C8 (200MHz): 1 wait access
 0x0C8 (200MHz) < MRCMHZ[9:0] ≤ 0x0FA (250MHz): 2 wait access
 Other setting is reserved.

30. Correction of 60.5.3 MREFREQ : Extra MRAM Frequency Notifications Register.

The following description will be revised.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
MRAM	60.5.3	3558	59.5.3	3546	59.5.3	3508	58.5.3	3374

Before Correction

MREMHZ[7:0] ≤ 0x64: 1 wait
 0x64 < MREMHZ[7:0] ≤ 0x7D: 2 waits
 Other setting is reserved.

After Correction

MREMHZ[7:0] ≤ 0x64 (100MHz): non wait access
 0x64 (100MHz) < MREMHZ[7:0] ≤ 0x7D (125MHz): 1 wait access
 Other setting is reserved.

31. Correction of Table 60.16 Address used by the Configuration Set command

The following description will be deleted.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
MRAM	Table 60.16	3602	Table 59.16	3590	Table 59.16	3552	Table 58.16	3418

Before Correction

Address	MSADDR register value	Setting data
BASE_MC + 0x00C9_F060	BASE_MCS + 0x00C9_F060	OCD/Serial Programmer ID Setting (OSIS)

After Correction

Deleted BASE_MC + 0x00C9_F060

32. Correction of 60.7.4.9 Increment Counter Command

The third item in the description of conditions under which the anti-rollback counter value does not increase will be revised.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
MRAM	60.7.4.9	3603	59.7.4.9	3591	59.7.4.9	3553	58.7.4.9	3419

Before Correction

- The update value of ARC_OEMBL is the unmatched register setting of the SHIP wrapper. For details of register of the SHIP wrapper, see the User’s Manual: Section xx.

After Correction

- The update value of ARC_OEMBL is equal to or higher than the OEM boot loader version (OEM BL Ver.) output from the security engine.

33. Correction of Table 60.36 Error protection type.

The following description will be revised.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
MRAM	Table 60.36	3618	Table 59.36	3606	Table 59.36	3568	Table 58.36	3434

Before Correction

Error type	Description
Illegal command error	Increment Counter command against ARC_OEMBL is issued when the SHIP wrapper register setting is the same or smaller than the ARC_OEMBL value (see section 60.8.5. Anti-Rollback Counter)

After Correction

Error type	Description
Illegal command error	Increment Counter command against ARC_OEMBL is issued when the OEM boot loader version (OEM BL Ver.) output from the security engine is the same or smaller than the ARC_OEMBL value (see section 60.8.5. Anti-Rollback Counter)

34. Correction of 60.13.2 Parallel Accessibility.

The following description will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
MRAM	60.13.2	3629	59.13.2	3617	59.13.2	3580	58.13.2	3445

Programming the code MRAM and the Extra MRAM cannot be executed at the same time, so they are arbitrated. The program executed later is forced to wait until the program executed first is completed. If the program for the code MRAM is started while MSTATR.MRDY = 0, the program will start after MSTATR.MRDY = 1. And if the program for the extra MRAM (issue the Program, Configuration set, or Increment Counter command) is started while MRCPS.PRGBSYC = 1, the program will start after MRCPS.PRGBSYC = 0. Therefore, in this case, the program time is the sum of the code and the extra MRAM program time.

There is also arbitration between read and program operations for the same MRAM macro, and they cannot be executed simultaneously. The values listed in the MRAM characteristics are for independent operation time without arbitration.

35. Correction of Table 70.2 Recommended operating condition

The ESWM description will be deleted, and SDRAM will be changed.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.2	4043	Table 69.2	4031	Table 62.2	3644	Table 60.2	3453

Before Correction

Parameter	Symbol			Min	Typ	Max	Unit
Power supply voltages	VCC2	Standard Product	Other than the following	1.62	—	3.63	V
			When ESWM is used	2.30	—	3.63	V
			When SDRAM is used	3.00	—	3.63	V

After Correction

Parameter	Symbol			Min	Typ	Max	Unit
Power supply voltages	VCC2	Standard Product	Other than the following	1.62	—	3.63	V
			When 32bit SDRAM is used	3.00	—	3.63	V

36. Correction of Table 70.35 Coremark and normal mode current, CPU0 Deep Sleep, CPU1 active. (DCDC mode and External VDD mode) (RA8P1 only)

The supply current value on CPU1 will be corrected.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.35	4077	—	—	—	—	—	—

Before Correction

Parameter			Sym bol	Typ	Max		Unit	Test conditions	
					95°C	105°C			
Supply current*1*2	CPUCLK1 = 250 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	I _{DD}	54	—	—	μ A/ MHz	CPU0 = Deep Sleep NPU and Graphics and ESWM power domain off CPUCLK0 = 1 GHz, NPUCLK = 500 MHz, MRICKL = 250 MHz, MRPCLK = 15.6 MHz, ICLK = 250 MHz, PCLKA = 15.6 MHz, PCLKB = 15.6 MHz, PCLKC = 15.6 MHz, PCLKD = 15.6 MHz, PCLKE = 15.6 MHz, BCLK = 15.6 MHz
			Cache off, executing from ITCM		49	—	—		
			Cache off, executing from SRAM		49	—	—		
			Cache off, executing from MRAM		67	—	—		
		Normal mode	All peripheral disabled, Cache on, while (1) code		50	—	—		
			All peripheral disabled, Cache off, while (1) code executing from MRAM		66	—	—		
	CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	47	—	—			
			Cache off, executing from ITCM	44	—	—			
			Cache off, executing from SRAM	43	—	—			
			Cache off, executing from MRAM	60	—	—			
		Normal mode	All peripheral disabled, Cache on, while (1) code	44	—	—			
			All peripheral disabled, Cache off, while (1) code executing from MRAM	59	—	—			
CPUCLK1 = 150 MHz VSCR_2 VCL = voltage range 2	Coremark	Cache on	40	—	—				
		Cache off, executing from ITCM	37	—	—				
		Cache off, executing from SRAM	37	—	—				
		Cache off, executing from MRAM	49	—	—				
	Normal mode	All peripheral disabled, Cache on, while (1) code	38	—	—				
		All peripheral disabled, Cache off, while (1) code executing from MRAM	49	—	—				

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

After Correction

Parameter			Sym bol	Typ	Max		Unit	Test conditions	
					95°C	105°C			
Supply current*1*2	CPUCLK1 = 250 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	IDD	215	—	—	$\mu A / MHz$	CPU0 = Deep Sleep NPU and Graphics and ESWM power domain off CPUCLK0 = 1 GHz, NPUCLK = 500 MHz, MRICKL = 250 MHz, MRPCLK = 15.6 MHz, ICLK = 250 MHz, PCLKA = 15.6 MHz, PCLKB = 15.6 MHz, PCLKC = 15.6 MHz, PCLKD = 15.6 MHz, PCLKE = 15.6 MHz, BCLK = 15.6 MHz
			Cache off, executing from ITCM		197	—	—		
			Cache off, executing from SRAM		194	—	—		
			Cache off, executing from MRAM		268	—	—		
		Normal mode	All peripheral disabled, Cache on, while (1) code		201	—	—		
			All peripheral disabled, Cache off, while (1) code executing from MRAM		264	—	—		
	CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	236	—	—			
			Cache off, executing from ITCM	218	—	—			
			Cache off, executing from SRAM	215	—	—			
			Cache off, executing from MRAM	299	—	—			
		Normal mode	All peripheral disabled, Cache on, while (1) code	222	—	—			
			All peripheral disabled, Cache off, while (1) code executing from MRAM	297	—	—			
CPUCLK1 = 150 MHz VSCR_2 VCL = voltage range 2	Coremark	Cache on	265	—	—				
		Cache off, executing from ITCM	247	—	—				
		Cache off, executing from SRAM	244	—	—				
		Cache off, executing from MRAM	326	—	—				
	Normal mode	All peripheral disabled, Cache on, while (1) code	252	—	—				
		All peripheral disabled, Cache off, while (1) code executing from MRAM	324	—	—				

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

37. Correction of Table 69.35 Coremark and normal mode current, CPU0 Deep Sleep, CPU1 active. (DCDC mode and External VDD mode) (RA8D2 only)

The supply current value on CPU1 will be corrected.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	—	—	Table 69.35	4065	—	—	—	—

Before Correction

Table 69.35 Coremark and normal mode current, CPU0 Deep Sleep, CPU1 active. (DCDC mode and External VDD mode)

Parameter			Sym bol	Typ	Max		Unit	Test conditions		
					95°C	105°C				
Supply current*1*2	CPUCLK1 = 250 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	IDD	54	—	—	μ A/ MHz	CPU0 = Deep Sleep Graphics and ESWM power domain off CPUCLK0 = 1 GHz, MRICKL = 250 MHz, MRPCLK = 15.6 MHz, ICLK = 250 MHz, PCLKA = 15.6 MHz, PCLKB = 15.6 MHz, PCLKC = 15.6 MHz, PCLKD = 15.6 MHz, PCLKE = 15.6 MHz, BCLK = 15.6 MHz	
			Cache off, executing from ITCM		49	—	—			
			Cache off, executing from SRAM		49	—	—			
			Cache off, executing from MRAM		67	—	—			
		Normal mode	All peripheral disabled, Cache on, while (1) code		50	—	—			
			All peripheral disabled, Cache off, while (1) code executing from MRAM		66	—	—			
		CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark		Cache on	47	—			—
					Cache off, executing from ITCM	44	—			—
	Cache off, executing from SRAM			43	—	—				
	Cache off, executing from MRAM			60	—	—				
Normal mode	All peripheral disabled, Cache on, while (1) code		44	—	—					
	All peripheral disabled, Cache off, while (1) code executing from MRAM		59	—	—					
CPUCLK1 = 150 MHz VSCR_2 VCL = voltage range 2	Coremark	Cache on	40	—	—					
		Cache off, executing from ITCM	37	—	—					
		Cache off, executing from SRAM	37	—	—					
		Cache off, executing from MRAM	49	—	—					
	Normal mode	All peripheral disabled, Cache on, while (1) code	38	—	—					
		All peripheral disabled, Cache off, while (1) code executing from MRAM	49	—	—					

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

After Correction

Parameter			Sym bol	Typ	Max		Unit	Test conditions		
					95°C	105°C				
Supply current*1*2	CPUCLK1 = 250 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	IDD	215	—	—	$\mu A / MHz$	CPU0 = Deep Sleep Graphics and ESWM power domain off CPUCLK0 = 1 GHz, MRICKL = 250 MHz, MRPCLK = 15.6 MHz, ICLK = 250 MHz, PCLKA = 15.6 MHz, PCLKB = 15.6 MHz, PCLKC = 15.6 MHz, PCLKD = 15.6 MHz, PCLKE = 15.6 MHz, BCLK = 15.6 MHz	
			Cache off, executing from ITCM		197	—	—			
			Cache off, executing from SRAM		194	—	—			
			Cache off, executing from MRAM		268	—	—			
		Normal mode	All peripheral disabled, Cache on, while (1) code		201	—	—			
			All peripheral disabled, Cache off, while (1) code executing from MRAM		264	—	—			
	CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	236	—	—	$\mu A / MHz$			CPU0 = Deep Sleep Graphics and ESWM power domain off CPUCLK0 = 800MHz, MRICKL = 200 MHz, MRPCLK = 12.5 MHz, ICLK = 200 MHz, PCLKA = 12.5 MHz, PCLKB = 12.5 MHz, PCLKC = 12.5 MHz, PCLKD = 12.5 MHz, PCLKE = 12.5 MHz, BCLK = 12.5 MHz
			Cache off, executing from ITCM	218	—	—				
			Cache off, executing from SRAM	215	—	—				
			Cache off, executing from MRAM	299	—	—				
		Normal mode	All peripheral disabled, Cache on, while (1) code	222	—	—				
			All peripheral disabled, Cache off, while (1) code executing from MRAM	297	—	—				
CPUCLK1 = 150 MHz VSCR_2 VCL = voltage range 2	Coremark	Cache on	265	—	—	$\mu A / MHz$	CPU0 = Deep Sleep Graphics and ESWM power domain off CPUCLK0 = 600MHz, MRICKL = 150 MHz, MRPCLK = 9.4 MHz, ICLK = 150 MHz, PCLKA = 9.4 MHz, PCLKB = 9.4 MHz, PCLKC = 9.4 MHz, PCLKD = 9.4 MHz, PCLKE = 9.4 MHz, BCLK = 9.4 MHz			
		Cache off, executing from ITCM	247	—	—					
		Cache off, executing from SRAM	244	—	—					
		Cache off, executing from MRAM	326	—	—					
	Normal mode	All peripheral disabled, Cache on, while (1) code	252	—	—					
		All peripheral disabled, Cache off, while (1) code executing from MRAM	324	—	—					

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

38. Correction of Table 62.35 Coremark and normal mode current, CPU0 Deep Sleep, CPU1 active. (DCDC mode and External VDD mode) (1 of 2) (RA8M2 only)

The supply current value on CPU1 will be corrected.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	—	—	—	—	Table 62.35	3684	—	—

Before Correction

Parameter			Sym bol	Typ	Max		Unit	Test conditions			
					95°C	105°C					
Supply current*1*2	CPUCLK1 = 250 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	I _{DD}	54	—	—	μA/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 1 GHz, MRCLK = 250 MHz, MRPCLK = 15.6 MHz, ICLK = 250 MHz, PCLKA = 15.6 MHz, PCLKB = 15.6 MHz, PCLKC = 15.6 MHz, PCLKD = 15.6 MHz, PCLKE = 15.6 MHz, BCLK = 15.6 MHz		
			Cache off, executing from ITCM		49	—	—				
			Cache off, executing from SRAM		49	—	—				
			Cache off, executing from MRAM		67	—	—				
		Normal mode	All peripheral disabled, Cache on, while (1) code		50	—	—				
			All peripheral disabled, Cache off, while (1) code executing from MRAM		66	—	—				
	CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on		47	—	—			μA/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 800 MHz, MRCLK = 200 MHz, MRPCLK = 12.5 MHz, ICLK = 200 MHz, PCLKA = 12.5 MHz, PCLKB = 12.5 MHz, PCLKC = 12.5 MHz, PCLKD = 12.5 MHz, PCLKE = 12.5 MHz, BCLK = 12.5 MHz
			Cache off, executing from ITCM		44	—	—				
			Cache off, executing from SRAM		43	—	—				
			Cache off, executing from MRAM		60	—	—				
Normal mode	All peripheral disabled, Cache on, while (1) code	44	—	—							
	All peripheral disabled, Cache off, while (1) code executing from MRAM	59	—	—							

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

After Correction

Parameter			Sym bol	Typ	Max		Unit	Test conditions			
					95°C	105°C					
Supply current*1*2	CPUCLK1 = 250 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	I _{DD}	215	—	—	μA/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 1 GHz, MRCLK = 250 MHz, MRPCLK = 15.6 MHz, ICLK = 250 MHz, PCLKA = 15.6 MHz, PCLKB = 15.6 MHz, PCLKC = 15.6 MHz, PCLKD = 15.6 MHz, PCLKE = 15.6 MHz, BCLK = 15.6 MHz		
			Cache off, executing from ITCM		197	—	—				
			Cache off, executing from SRAM		194	—	—				
			Cache off, executing from MRAM		268	—	—				
		Normal mode	All peripheral disabled, Cache on, while (1) code		201	—	—				
			All peripheral disabled, Cache off, while (1) code executing from MRAM		264	—	—				
	CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on		236	—	—			μA/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 800 MHz, MRCLK = 200 MHz, MRPCLK = 12.5 MHz, ICLK = 200 MHz, PCLKA = 12.5 MHz, PCLKB = 12.5 MHz, PCLKC = 12.5 MHz, PCLKD = 12.5 MHz, PCLKE = 12.5 MHz, BCLK = 12.5 MHz
			Cache off, executing from ITCM		218	—	—				
			Cache off, executing from SRAM		215	—	—				
			Cache off, executing from MRAM		299	—	—				
Normal mode	All peripheral disabled, Cache on, while (1) code	222	—	—							
	All peripheral disabled, Cache off, while (1) code executing from MRAM	297	—	—							

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

39. Correction of Table 62.35 Coremark and normal mode current, CPU0 Deep Sleep, CPU1 active. (DCDC mode and External VDD mode) (2 of 2) (RA8M2 only)

The supply current value on CPU1 will be corrected.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	—	—	—	—	Table 62.35	3685	—	—

Before Correction

Parameter			Sym bol	Typ	Max		Unit	Test conditions					
					95°C	105°C							
Supply current*1*2	CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	I _{DD}	45	—	—	μ A/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 600 MHz, MRICKL = 200 MHz, MRPCLK = 25 MHz, ICLK = 200 MHz, PCLKA = 25 MHz, PCLKB = 25 MHz, PCLKC = 25 MHz, PCLKD = 25 MHz, PCLKE = 25 MHz, BCLK = 25MHz				
			Cache off, executing from ITCM		42	—	—						
			Cache off, executing from SRAM		41	—	—						
			Cache off, executing from MRAM		58	—	—						
		Normal mode	All peripheral disabled, Cache on, while (1) code		43	—	—						
			All peripheral disabled, Cache off, while (1) code executing from MRAM		57	—	—						
			CPUCLK1 = 150 MHz VSCR_2 VCL = voltage range 2		Coremark	Cache on	40			—	—	μ A/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 600 MHz, MRICKL = 150 MHz, MRPCLK = 9.4 MHz, ICLK = 150 MHz, PCLKA = 9.4 MHz, PCLKB = 9.4 MHz, PCLKC = 9.4 MHz, PCLKD = 9.4 MHz, PCLKE = 9.4 MHz, BCLK = 9.4 MHz
						Cache off, executing from ITCM	37			—	—		
	Cache off, executing from SRAM	37				—	—						
	Cache off, executing from MRAM	49				—	—						
Normal mode	All peripheral disabled, Cache on, while (1) code	38	—	—									
	All peripheral disabled, Cache off, while (1) code executing from MRAM	49	—	—									

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

After Correction

Parameter			Sym bol	Typ	Max		Unit	Test conditions					
					95°C	105°C							
Supply current*1*2	CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	I _{DD}	226	—	—	μ A/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 600 MHz, MRICKL = 200 MHz, MRPCLK = 25 MHz, ICLK = 200 MHz, PCLKA = 25 MHz, PCLKB = 25 MHz, PCLKC = 25 MHz, PCLKD = 25 MHz, PCLKE = 25 MHz, BCLK = 25MHz				
			Cache off, executing from ITCM		208	—	—						
			Cache off, executing from SRAM		205	—	—						
			Cache off, executing from MRAM		289	—	—						
		Normal mode	All peripheral disabled, Cache on, while (1) code		213	—	—						
			All peripheral disabled, Cache off, while (1) code executing from MRAM		287	—	—						
			CPUCLK1 = 150 MHz VSCR_2 VCL = voltage range 2		Coremark	Cache on	265			—	—	μ A/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 600 MHz, MRICKL = 150 MHz, MRPCLK = 9.4 MHz, ICLK = 150 MHz, PCLKA = 9.4 MHz, PCLKB = 9.4 MHz, PCLKC = 9.4 MHz, PCLKD = 9.4 MHz, PCLKE = 9.4 MHz, BCLK = 9.4 MHz
						Cache off, executing from ITCM	247			—	—		
	Cache off, executing from SRAM	244				—	—						
	Cache off, executing from MRAM	326				—	—						
Normal mode	All peripheral disabled, Cache on, while (1) code	252		—	—								
	All peripheral disabled, Cache off, while (1) code executing from MRAM	324		—	—								

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

40. Correction of Table 60.35 Coremark and normal mode current, CPU0 Deep Sleep, CPU1 active. (DCDC mode and External VDD mode) (1 of 2) (RA8T2 only)

The supply current value on CPU1 will be corrected.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	—	—	—	—	—	—	Table 60.35	3492

Before Correction

Parameter			Sym bol	Typ	Max		Unit	Test conditions				
					95°C	105°C						
Supply current*1*2	CPUCLK1 = 250 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	I _{DD}	54	—	—	μ A/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 1 GHz, MRICK = 250 MHz, MRPCLK = 15.6 MHz, ICLK = 250 MHz, PCLKA = 15.6 MHz, PCLKB = 15.6 MHz, PCLKC = 15.6 MHz, PCLKD = 15.6 MHz, PCLKE = 15.6 MHz, BCLK = 15.6 MHz			
			Cache off, executing from ITCM		49	—	—					
			Cache off, executing from SRAM		49	—	—					
			Cache off, executing from MRAM		67	—	—					
	Normal mode	All peripheral disabled, Cache on, while (1) code	50	—	—							
		All peripheral disabled, Cache off, while (1) code executing from MRAM	66	—	—							
		CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on		47	—			—	μ A/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 800 MHz, MRICK = 200 MHz, MRPCLK = 12.5 MHz, ICLK = 200 MHz, PCLKA = 12.5 MHz, PCLKB = 12.5 MHz, PCLKC = 12.5 MHz, PCLKD = 12.5 MHz, PCLKE = 12.5 MHz, BCLK = 12.5 MHz
				Cache off, executing from ITCM		44	—			—		
Cache off, executing from SRAM	43			—		—						
Cache off, executing from MRAM	60			—		—						
Normal mode	All peripheral disabled, Cache on, while (1) code	44	—	—								
	All peripheral disabled, Cache off, while (1) code executing from MRAM	59	—	—								

After Correction

Parameter			Sym bol	Typ	Max		Unit	Test conditions				
					95°C	105°C						
Supply current*1*2	CPUCLK1 = 250 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	I _{DD}	215	—	—	μ A/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 1 GHz, MRICK = 250 MHz, MRPCLK = 15.6 MHz, ICLK = 250 MHz, PCLKA = 15.6 MHz, PCLKB = 15.6 MHz, PCLKC = 15.6 MHz, PCLKD = 15.6 MHz, PCLKE = 15.6 MHz, BCLK = 15.6 MHz			
			Cache off, executing from ITCM		197	—	—					
			Cache off, executing from SRAM		194	—	—					
			Cache off, executing from MRAM		268	—	—					
	Normal mode	All peripheral disabled, Cache on, while (1) code	201	—	—							
		All peripheral disabled, Cache off, while (1) code executing from MRAM	264	—	—							
		CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on		236	—			—	μ A/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 800 MHz, MRICK = 200 MHz, MRPCLK = 12.5 MHz, ICLK = 200 MHz, PCLKA = 12.5 MHz, PCLKB = 12.5 MHz, PCLKC = 12.5 MHz, PCLKD = 12.5 MHz, PCLKE = 12.5 MHz, BCLK = 12.5 MHz
				Cache off, executing from ITCM		218	—			—		
Cache off, executing from SRAM	215			—		—						
Cache off, executing from MRAM	299			—		—						
Normal mode	All peripheral disabled, Cache on, while (1) code	222	—	—								
	All peripheral disabled, Cache off, while (1) code executing from MRAM	297	—	—								

41. Correction of Table 60.35 Coremark and normal mode current, CPU0 Deep Sleep, CPU1 active. (DCDC mode and External VDD mode) (2 of 2) (RA8T2 only)

The supply current value on CPU1 will be corrected.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	—	—	—	—	—	—	Table 60.35	3493

Before Correction

Parameter			Sym bol	Typ	Max		Unit	Test conditions				
					95°C	105°C						
Supply current*1*2	CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	I _{DD}	45	—	—	μA/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 600 MHz, MRICKL = 200 MHz, MRPCLK = 25 MHz, ICLK = 200 MHz, PCLKA = 25 MHz, PCLKB = 25 MHz, PCLKC = 25 MHz, PCLKD = 25 MHz, PCLKE = 25 MHz, BCLK = 25MHz			
			Cache off, executing from ITCM		42	—	—					
			Cache off, executing from SRAM		41	—	—					
			Cache off, executing from MRAM		58	—	—					
	Normal mode	All peripheral disabled, Cache on, while (1) code	43		—	—						
		All peripheral disabled, Cache off, while (1) code executing from MRAM	57		—	—						
		CPUCLK1 = 150 MHz VSCR_2 VCL = voltage range 2	Coremark		Cache on	40	—			—	μA/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 600 MHz, MRICKL = 150 MHz, MRPCLK = 9.4 MHz, ICLK = 150 MHz, PCLKA = 9.4 MHz, PCLKB = 9.4 MHz, PCLKC = 9.4 MHz, PCLKD = 9.4 MHz, PCLKE = 9.4 MHz, BCLK = 9.4 MHz
					Cache off, executing from ITCM	37	—			—		
Cache off, executing from SRAM	37			—	—							
Cache off, executing from MRAM	49			—	—							
Normal mode	All peripheral disabled, Cache on, while (1) code	38	—	—								
	All peripheral disabled, Cache off, while (1) code executing from MRAM	49	—	—								

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

After Correction

Parameter			Sym bol	Typ	Max		Unit	Test conditions				
					95°C	105°C						
Supply current*1*2	CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	I _{DD}	226	—	—	μA/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 600 MHz, MRICKL = 200 MHz, MRPCLK = 25 MHz, ICLK = 200 MHz, PCLKA = 25 MHz, PCLKB = 25 MHz, PCLKC = 25 MHz, PCLKD = 25 MHz, PCLKE = 25 MHz, BCLK = 25MHz			
			Cache off, executing from ITCM		208	—	—					
			Cache off, executing from SRAM		205	—	—					
			Cache off, executing from MRAM		289	—	—					
	Normal mode	All peripheral disabled, Cache on, while (1) code	213		—	—						
		All peripheral disabled, Cache off, while (1) code executing from MRAM	287		—	—						
		CPUCLK1 = 150 MHz VSCR_2 VCL = voltage range 2	Coremark		Cache on	265	—			—	μA/ MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 600 MHz, MRICKL = 150 MHz, MRPCLK = 9.4 MHz, ICLK = 150 MHz, PCLKA = 9.4 MHz, PCLKB = 9.4 MHz, PCLKC = 9.4 MHz, PCLKD = 9.4 MHz, PCLKE = 9.4 MHz, BCLK = 9.4 MHz
					Cache off, executing from ITCM	247	—			—		
Cache off, executing from SRAM	244			—	—							
Cache off, executing from MRAM	326			—	—							
Normal mode	All peripheral disabled, Cache on, while (1) code	252	—	—								
	All peripheral disabled, Cache off, while (1) code executing from MRAM	324	—	—								

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

42. Correction of Table 70.47 Clock timing except for sub-clock oscillator (2 of 2) (RA8P1/RA8D2)

The HOCO accuracy and FLL stabilization time specifications for SiP Product will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.47	4113	Table 69.47	4098	—	—	—	—

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
HOCO clock oscillator oscillation frequency	Without FLL (SiP Product)	fHOCO16	15.744	16.000	16.256	MHz	-20 ≤ Tj ≤ 105°C
		fHOCO18	17.712	18.000	18.288		
		fHOCO20	19.680	20.000	20.320		
		fHOCO32	31.488	32.000	32.512		
		fHOCO48	47.232	48.000	48.768		
		fHOCO16	15.680	16.000	16.320		-40 ≤ Tj ≤ 105°C
		fHOCO18	17.640	18.000	18.360		
		fHOCO20	19.600	20.000	20.400		
		fHOCO32	31.360	32.000	32.640		
		fHOCO48	47.040	48.000	48.960		
FLL stabilization wait time (SiP Product)		tFLLWT	—	—	2.15	ms	—

43. Correction of Table 70.47 Clock timing except for sub-clock oscillator (2 of 2) (RA8M2/RA8T2)

The HOCO accuracy and FLL stabilization time specifications for SiP Product will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	—	—	—	—	Table 62.47	3720	Table 60.47	3529

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
HOCO clock oscillator oscillation frequency	Without FLL (SiP Product)	fHOCO16	15.744	16.000	16.256	MHz	-20 ≤ Tj ≤ 105°C
		fHOCO18	17.712	18.000	18.288		
		fHOCO20	19.680	20.000	20.320		
		fHOCO32	31.488	32.000	32.512		
		fHOCO48	47.232	48.000	48.768		
		fHOCO16	15.680	16.000	16.320		-40 ≤ Tj ≤ 125°C
		fHOCO18	17.640	18.000	18.360		
		fHOCO20	19.600	20.000	20.400		
		fHOCO32	31.360	32.000	32.640		
		fHOCO48	47.040	48.000	48.960		
FLL stabilization wait time (SiP Product)		tFLLWT	—	—	2.15	ms	—

44. Correction of Table 70.49 Reset timing

The following description of DPSBYCR.DCSSMODE=00 in RES pulse width will be deleted.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.49	4116	Table 69.49	4101	Table 62.49	3723	Table 60.49	3532

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
RES pulse width	Deep Software Standby Mode 1	DPSBYCR.DCSSMODE = 00	tRESWD	0.43	—	—	ms	Figure 70.33
	Deep Software Standby Mode 2	DPSBYCR.DCSSMODE = 00		0.43	—	—		
	Deep Software Standby Mode 3	DPSBYCR.DCSSMODE = 00		0.60	—	—		

45. Correction of Table 70.50 Timing of recovery from low power modes

The following description of DPSBYCR.DCSSMODE=00 in Recovery time from Deep Software Standby mode will be deleted.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.50	4118	Table 69.50	4103	Table 62.50	3726	Table 60.50	3535

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Recovery time from Deep Software Standby mode	Deep Software Standby Mode 1	DPSBYCR.DCSSMODE = 00	t _{DSBY}	–	216	266	us	Figure 70.35
	Deep Software Standby Mode 2	DPSBYCR.DCSSMODE = 00		–	216	266		
	Deep Software Standby Mode 3	DPSBYCR.DCSSMODE = 00		–	403	524		

46. Correction of Table 70.62 OSPI timing (7 of 8)

The error of voltage description will be corrected.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.62	4172	Table 69.62	4157	Table 62.62	3779	Table 60.62	3588

Before Correction

Item	Symbol		Min	Max	Unit	Note
Clock Low to CS Low	tCKLCSL	1.65 V to 2.00 V	VSCR_1, voltage range 1	6	–	ns
			VSCR_2, voltage range 2			

After Correction

Item	Symbol		Min	Max	Unit	Note
Clock Low to CS Low	tCKLCSL	1.62 V to 2.00 V	VSCR_1, voltage range 1	6	–	ns
			VSCR_2, voltage range 2			

47. Addition of Table 70.62 OSPI timing (9 of 9)

The t_{CKHDSH} item for OSPI AC Characteristics will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.62	4174	Table 69.62	4159	Table 62.62	3781	Table 60.62	3590

Table 70.62 OSPI timing (9 of 9)

Conditions:

High-speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_SCLK, OM_n_SCLKN, OM_n_SIO7-0, OM_n_DQS.

Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_CS0, OM_n_CS1. Load capacitance C = 15pF

Parameter	Symbol	VCC/VCC2	VDD	Min	Max	Unit	Note
Clock High to DQS input ⁴	t _{CKHDSH}	2.70 V or above	VSCR_1, voltage range 1	-	t _{PERIOD} × (1 + DDRSMPEX[3:0]) - 8.5	ns	Figure 70.85
			VSCR_2, voltage range 2				
		1.62 V to 2.00 V	VSCR_1, voltage range 1	-	t _{PERIOD} × (1 + DDRSMPEX[3:0]) - 12.5		
			VSCR_2, voltage range 2				

Note: n = 0, 1

Note 1. This restriction does not need to be met when using the JESD251 Profile 1.0 memory with an external pull-down attached to the OM_DQS pin.

Note 2. Condition: COMCFG.OEASTEX = 1

Note 3. Condition: LIOCFGCSx.CSASTEX = 1

Note 4. See the datasheet of memory and set DDRSMPEX[3:0] bits to satisfy this value.

48. Correction of Figure 70.85 DDR transmit/receive timing (4S-4D-4D, 8D-8D-8D)

The t_{CKHDSH} item for OSPI AC Characteristics will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Figure 70.85	4175	Figure 69.85	4160	Ta 62.85	3782	Table 60.86	3591

Before Correction

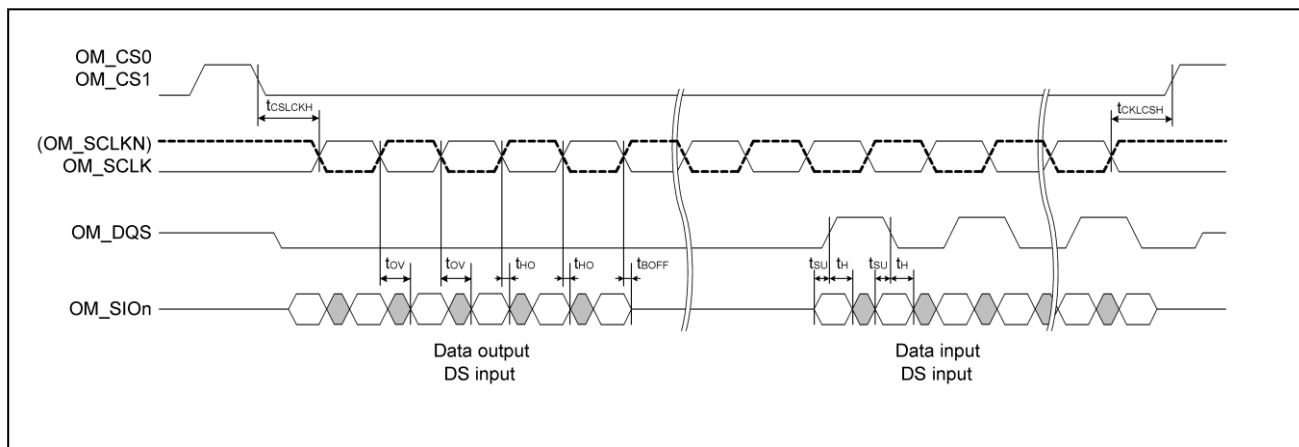


Figure 70.85 DDR transmit/receive timing (4S-4D-4D, 8D-8D-8D)

After Correction

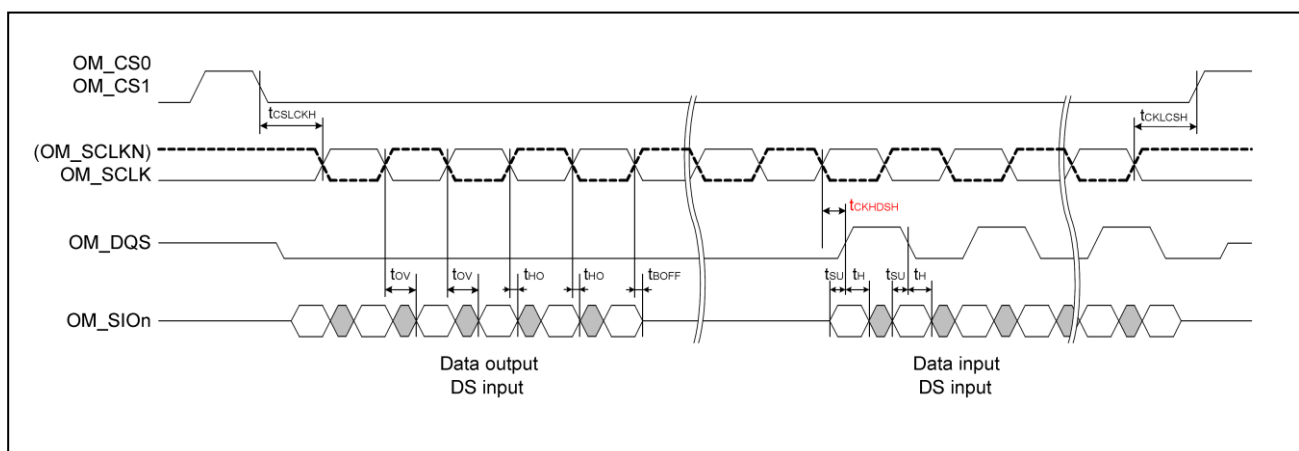


Figure 70.85 DDR transmit/receive timing (4S-4D-4D, 8D-8D-8D)

49. Correction of Table 70.77 PDG Timing

The error of test conditions will be corrected.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.77	4206	Table 69.77	4191	Table 62.76	3811	Table 60.74	3615

Before Correction

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	48.8	—	ps	GTDLYCR.FRANGE[1:0] = 00 and GPTCLK = 300 MHz

After Correction

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	48.8	—	ps	GTDLYCR.FRANGE[1:0] = 00 and GPTCLK = 160 MHz

50. Correction of Table 70.93 HS-RX Characteristics (RA8P1/RA8D2)

The Min/Typ/Max/Unit description of Table 70.93 HS-RX Characteristics for MIPI D-PHY will be revised.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.93	4221	Table 69.93	4206	—	—	—	—

Before Correction

Table 70.93 HS-RX Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Common-mode voltage HS receiver mode	V _{CMRX} (DC)	mV	70	—	330	
Differential input impedance	Z _{ID}	Ω	80	100	125	
Differential input impedance in unterminated mode	Z _{ID_OPEN}	kΩ	10k	—	—	
RX Data to Clock Setup Time Tolerance	T _{SETUP[RX]}	UIhs	-0.15	—	0.15	
	T _{HOLD[RX]}	UIhs	-0.15	—	0.15	
Common-mode interference beyond 450MHz	V _{CMRX} (HF)	mV	—	—	100	
Common-mode interference 50MHz – 450MHz	V _{CMRX} (LF)	mV	-50	—	50	
Differential input high threshold	V _{IDTH}	mV	—	—	70	
Differential input low threshold	V _{IDTL}	mV	-70	—	—	
Single-ended input high voltage	V _{IHHS}	mV	—	—	460	
Single-ended input low voltage	V _{ILHS}	mV	-40	—	—	
Single-ended threshold for HS termination enable	V _{TERM-EN}	mV	—	—	450	
Common-mode termination	C _{CM}	pF	—	—	60	
Datarate	D _{atarate}	Mbps	80	—	720	
Differential Return Loss	f _{hMIN}	S _{ddRX}	dB	—	—	-15
	f _{hMIN}		dB	—	—	-8.5
	f _{hMAX}		dB	—	—	-2.9
Common-mode Return Loss	1/4f _{INT MIN}	S _{ccRX}	dB	—	—	0
	f _{INT MIN}		dB	—	—	-6
	f _{hMAX}		dB	—	—	-6
Mode-Conversion Limits	S _{dcRX}	dB	—	—	-26	

After Correction

Parameter	Symbol	Min	Typ	Max	Unit	Note
Common-mode voltage HS receiver mode	V _{CMRX (DC)}	70	—	330	mV	
Differential input impedance	Z _{ID}	80	100	125	Ω	
Differential input impedance in unterminated mode	Z _{ID_OPEN}	10k	—	—	kΩ	
RX Data to Clock Setup Time Tolerance	T _{SETUP[RX]}	-0.15	—	0.15	UIhs	
	T _{HOLD[RX]}	-0.15	—	0.15	UIhs	
Common-mode interference beyond 450MHz	V _{CMRX (HF)}	—	—	100	mV	
Common-mode interference 50MHz – 450MHz	V _{CMRX (LF)}	-50	—	50	mV	
Differential input high threshold	V _{IDTH}	—	—	70	mV	
Differential input low threshold	V _{IDTL}	-70	—	—	mV	
Single-ended input high voltage	V _{IHHS}	—	—	460	mV	
Single-ended input low voltage	V _{ILHS}	-40	—	—	mV	
Single-ended threshold for HS termination enable	V _{TERM-EN}	—	—	450	mV	
Common-mode termination	C _{CM}	—	—	60	pF	
Datarate	D _{atarate}	80	—	720	Mbps	
Differential Return Loss	f _{hMIN}	S _{ddRX}	—	—	-15	dB
	f _{hMIN}		—	—	-8.5	dB
	f _{MAX}		—	—	-2.9	dB
Common-mode Return Loss	1/4f _{INT MIN}	S _{ccRX}	—	—	0	dB
	f _{INT MIN}		—	—	-6	dB
	f _{MAX}		—	—	-6	dB
Mode-Conversion Limits	S _{dcRX}	—	—	-26	dB	

51. Correction of Table 70.112 TSN characteristics

The output Voltage will be corrected.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.112	4253	Table 69.112	4238	Table 62.105	3855	Table 60.100	3658

Before Correction

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage (at 25 °C)	—	—	1.24	—	V	—

After Correction

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage (at 25 °C)	—	—	0.83	—	V	—

52. Correction of Table 70.114 Sub-clock oscillation stop detection circuit characteristics

The wait time for startup will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.114	4254	Table 69.114	4239	Table 62.107	3856	Table 60.102	3659

Before Correction

Table 70.114 Sub-clock oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	2	ms	Figure 70.140

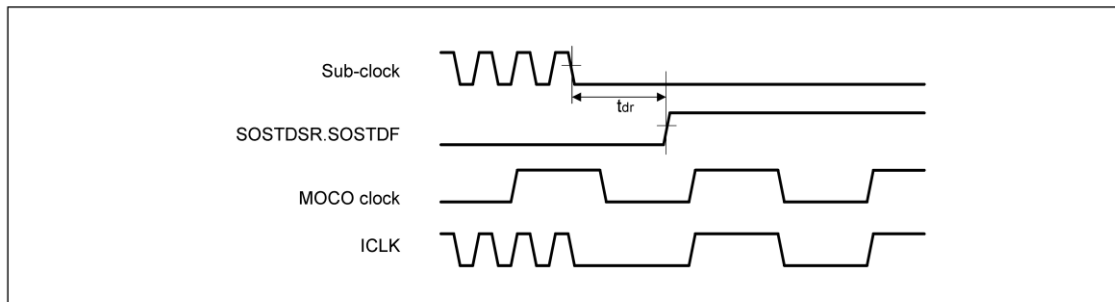


Figure 70.140 Sub-clock oscillation stop detection timing

After Correction

Table 70.117 Sub-clock oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Wait time for startup	t_{sodsup}	100	—	—	μ s	Figure 1.140
Detection time	t_{dr}	—	—	2	ms	Figure 1.141

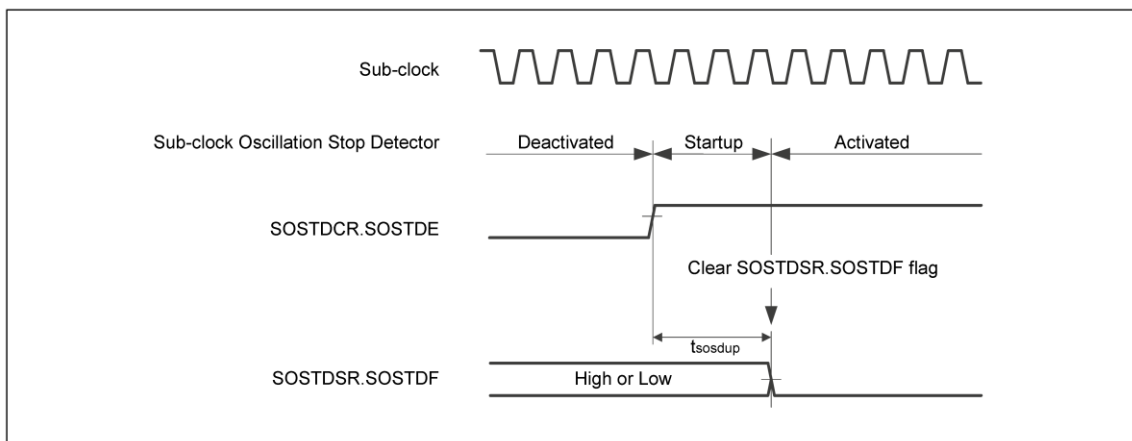


Figure 70.140 Sub-clock Oscillation Stop Detector start-up time

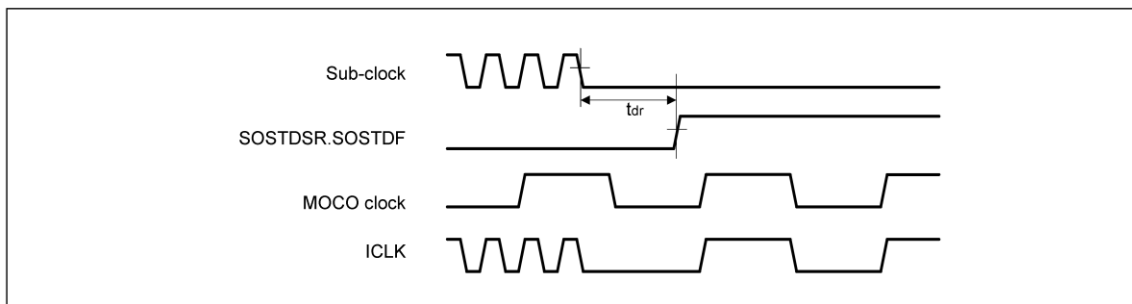


Figure 70.141 Sub-clock oscillation stop detection timing

53. Correction of Table 70.115 Power-on reset circuit and voltage detection circuit characteristics (1 of 2)

The following description will be deleted.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.115	4255	Table 69.115	4240	Table 62.108	3857	Table 60.103	3660

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Voltage detection circuit (PVDn) (n = 1, 2, 4, 5)	Vdetn_0 rise	4.23	4.39	4.54	V	Figure 70.143
		Vdetn_0 fall	4.13	4.29	4.44		
		Vdetn_1 rise	4.10	4.26	4.41		
		Vdetn_1 fall	4.00	4.16	4.31		
		Vdetn_2 rise	3.98	4.13	4.27		
		Vdetn_2 fall	3.88	4.03	4.17		

54. Correction of Figure 70.141 Power-on reset timing

The VD description will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Figure 70.141	4256	Figure 69.141	4241	Figure 62.138	3858	Figure 60.128	3661

Before Correction

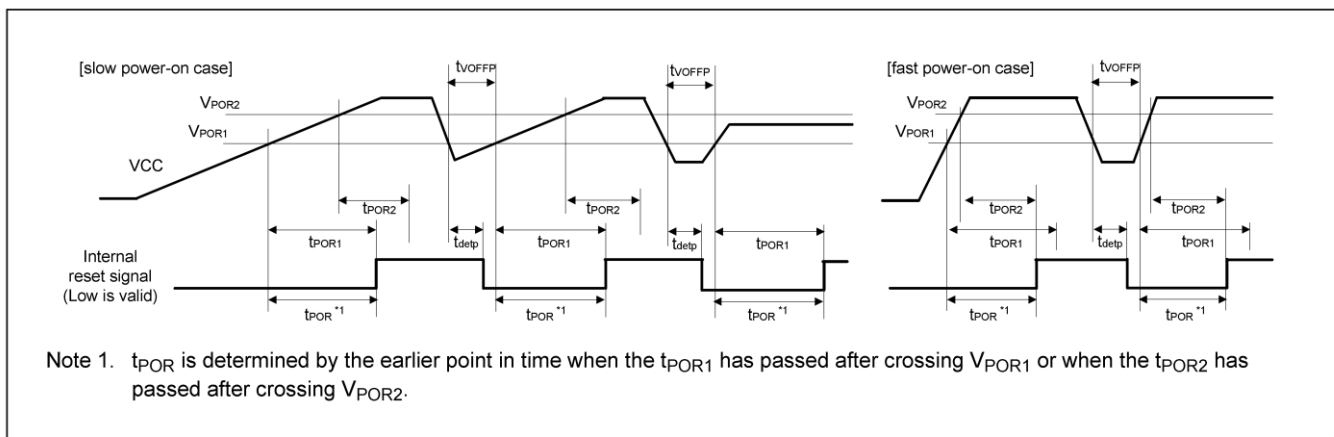


Figure 70.141 Power-on reset timing

After Correction

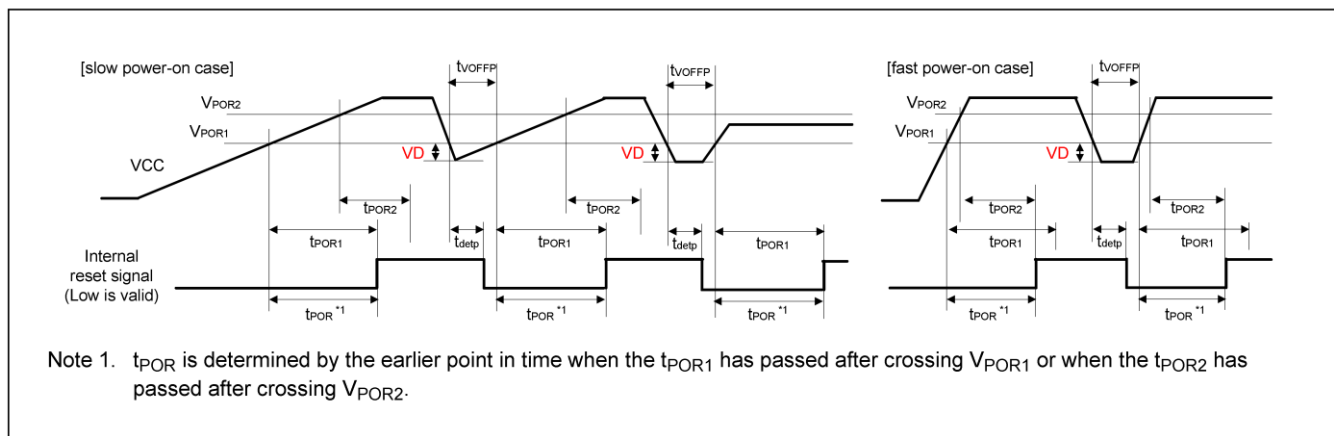


Figure 70.141 Power-on reset timing

55. Correction of Figure 70.142 Voltage detection circuit timing (V_{det0})

The VD description will be deleted.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Figure 70.142	4257	Figure 69.142	4242	Figure 62.139	3859	Figure 60.129	3662

Before Correction

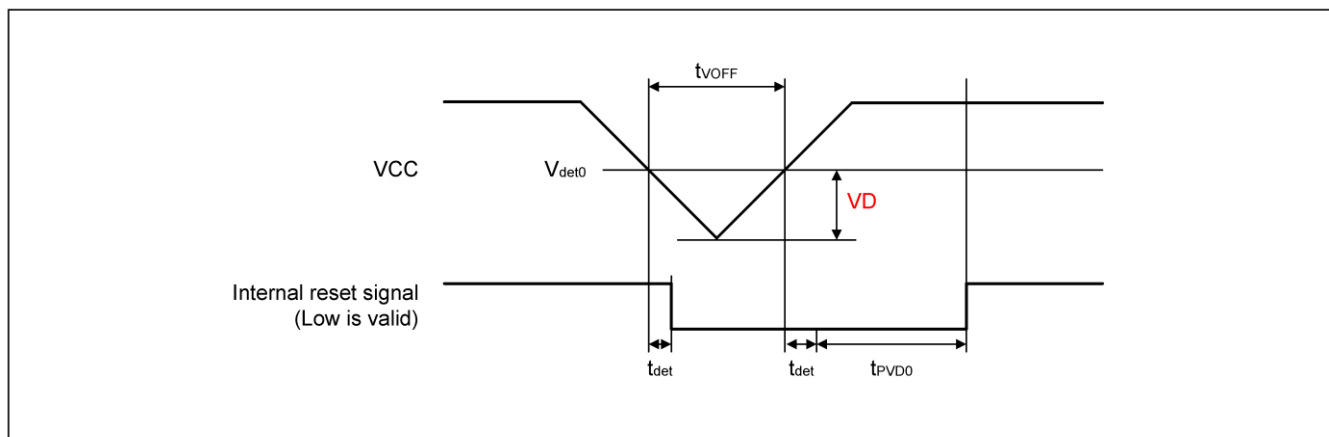


Figure 70.142 Voltage detection circuit timing (V_{det0})

After Correction

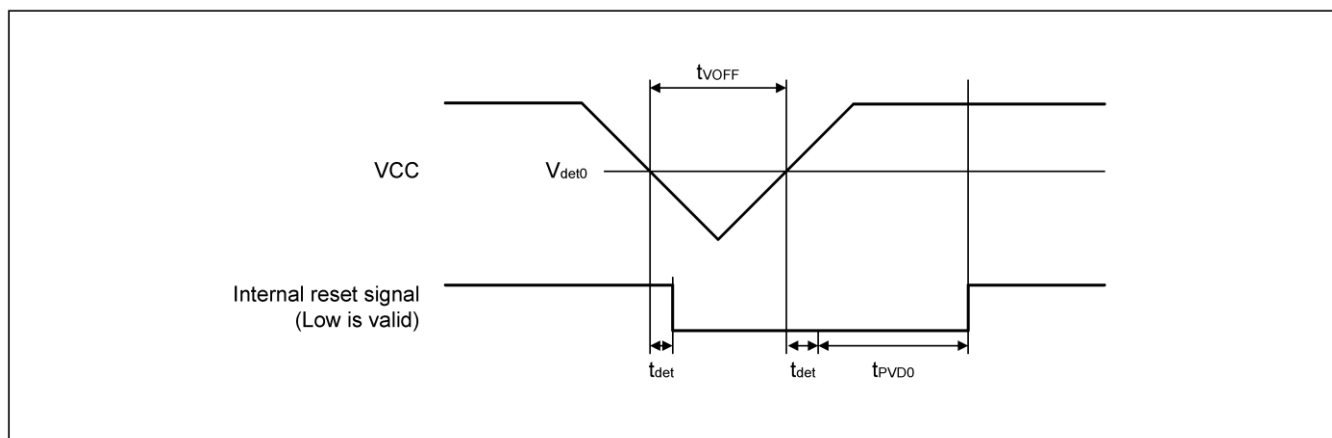


Figure 70.142 Voltage detection circuit timing (V_{det0})

56. Correction of Figure 70.143 Voltage detection circuit timing (V_{detn}) ($n = 1, 2, 4, 5$)

The VD description will be deleted.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Figure 70.143	4257	Figure 69.143	4242	Figure 62.140	3859	Figure 60.130	3663

Before Correction

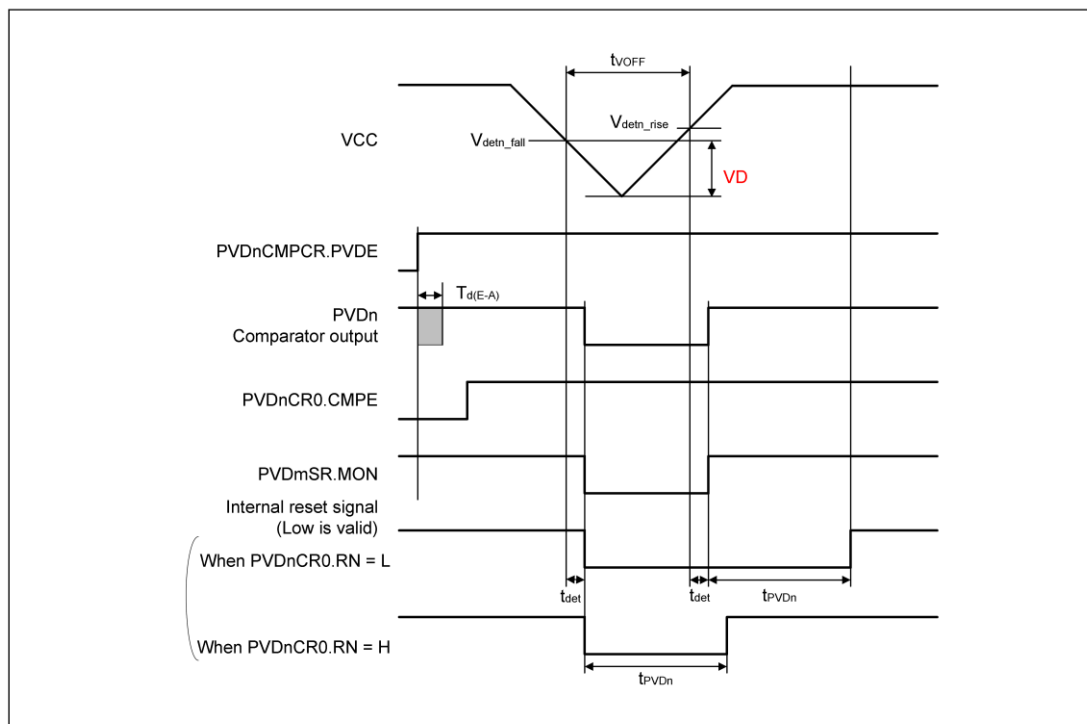


Figure 70.143 Voltage detection circuit timing (V_{detn}) ($n = 1, 2, 4, 5$)

After Correction

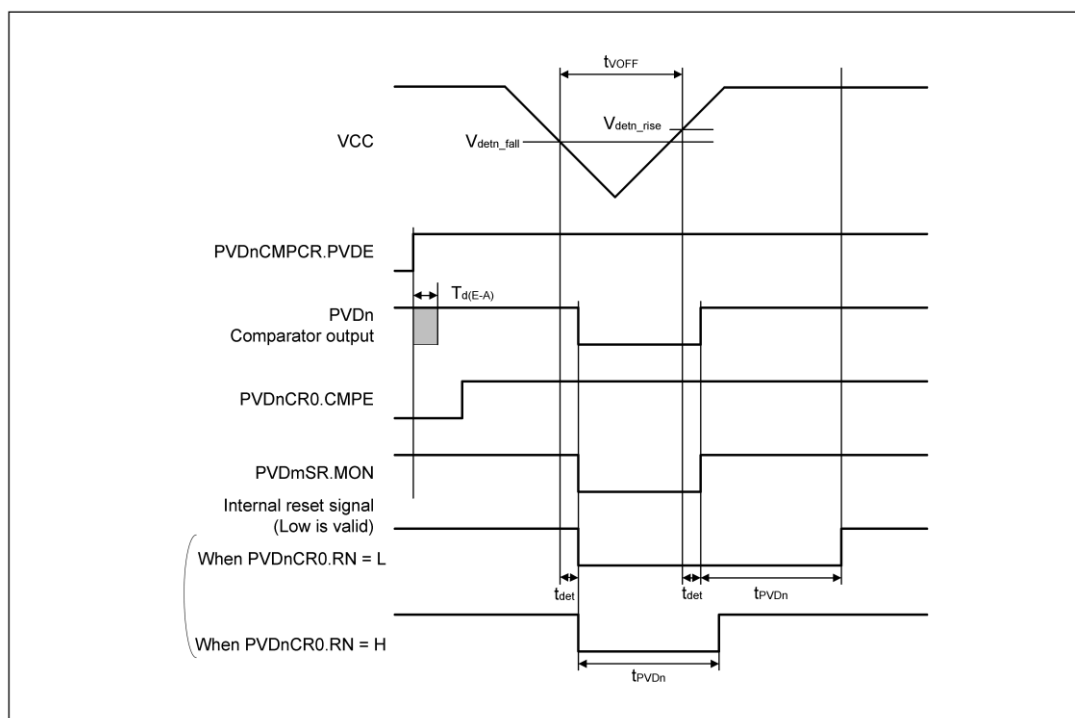


Figure 70.143 Voltage detection circuit timing (V_{detn}) ($n = 1, 2, 4, 5$)

57. Correction of Table 70.121 Code MRAM Characteristics (1 of 2)

The following explanation of MRAM rewrite count will be added.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.121	4262	Table 69.121	4247	Table 62.114	3864	Table 60.109	3667

Before Correction

Table 70.121 Code MRAM Characteristics (1 of 2)

Parameter	Symbol	MRICKL = 250 MHz			MRICKL = 250 MHz			MRICKL = 250 MHz			MRICKL = 250 MHz			Unit	Test conditions
		Min	Typ* 4	Max	Min	Typ* 4	Max	Min	Typ* 4	Max	Min	Typ* 4	Max		
Reprogramm ing cycle	N _{PC}	1000 00* ¹	—	—	100 000* 1	—	—	100 000* 1	—	—	100 000* 1	—	—	Tim es	—

After Correction

Parameter	Symbol	MRICKL = 250 MHz			MRICKL = 250 MHz			MRICKL = 250 MHz			MRICKL = 250 MHz			Unit	Test conditions
		Min	Typ* 4	Max	Min	Typ* 4	Max	Min	Typ* 4	Max	Min	Typ* 4	Max		
Reprogramm ing cycle* ⁹	N _{PC}	1000 00* ¹	—	—	100 000* 1	—	—	100 000* 1	—	—	100 000* 1	—	—	Tim es	—

Note 9. The reprogramming cycle is the number of programming per 32-byte code MRAM address space. Programming the same data to the same address also increases the reprogramming cycle count by one. For a reprogramming cycle of n times (n = 100,000), programming can be performed n times for every 32-byte code MRAM address space.

58. Correction of Table 70.122 Extra MRAM (MRAM area) characteristics

The data in this table was deleted due to it was values which included non-public areas, and will be changed to "Command time for Configuration set" which listed in 70.125 MACI command characteristics, this is for only the public areas.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.122	4263	Table 69.122	4248	Table 62.115	3865	Table 60.110	3668

Before correction

Table 70.122 Extra MRAM (MRAM area) characteristics

Parameter	Symbol	MRICKL = 125 MHz			MRICKL = 100 MHz			MRICKL = 75 MHz			MRICKL = 66 MHz			Unit	Test conditions	
		Min	Typ. ⁴	Max	Min	Typ. ⁴	Max	Min	Typ. ⁴	Max	Min	Typ. ⁴	Max			
Programming time of 16-byte ^{7,8}	Normal program mode (MRPSC. MHSPEN = 0)	t _{PM} _E	—	6.82 ⁵	75.8 ⁶	—	7.06 ⁵	76.6 ⁶	—	7.53 ⁵	80.7 ⁶	—	8.08 ⁵	85.2 ⁶	μs	—
	High speed program mode (MRPSC. MHSPEN = 1)	t _{PM} _E	—	4.82 ⁵	73.8 ⁶	—	5.06 ⁵	74.6 ⁶	—	5.53 ⁵	78.7 ⁶	—	6.08 ⁵	83.2 ⁶	μs	—
Reprogramming cycle	N _{PC}	1000	—	—	100	—	—	100	—	—	100	—	—	Times	—	
Data hold time ²	t _{DRP}	10 ⁻² ^{*3}	—	—	10 ⁻² ^{*3}	—	—	10 ⁻² ^{*3}	—	—	10 ⁻² ^{*3}	—	—	Years	Tj = +12 5°C	

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 3. This result is obtained from reliability testing.

Note 4. The reference value at VCC = 3.3 V and room temperature.

Note 5. Perform rewrite 50% of bits at Typ. condition.

Note 6. Timeout values of Figure x.x is about 1.1 times of the maximum value. (t_{PME} + t_{PMC} + Read time (MRPCLK 40cycle)).

Note 7. To calculate the updating time at other frequencies, using approximate formula below listed. (F_{MRPCLK}: frequency of MRPCLK[MHz])

$$t_{PMC} \text{ (Typ)} = 179.2/F_{MRPCLK} + 5.725 \text{ [}\mu\text{s]}, t_{PMC} \text{ (Max)} = 1988/F_{MRPCLK} + 61.9 \text{ [}\mu\text{s]} \text{ for normal program mode.}$$

$$t_{PMC} \text{ (Typ)} = 179.2/F_{MRPCLK} + 3.725 \text{ [}\mu\text{s]}, t_{PMC} \text{ (Max)} = 1988/F_{MRPCLK} + 59.9 \text{ [}\mu\text{s]} \text{ for high speed program mode.}$$

Note 8. Read and program operations for the extra MRAM cannot be executed simultaneously. This value is for independent program operation without arbitration between read and program.

After correction

Table 70.122 Option Setting Memory (configuration area) characteristics

Parameter		Symbol	MRICKL = 125 MHz			MRICKL = 100 MHz			MRICKL = 75 MHz			MRICKL = 66 MHz			Unit	Test conditions
			Min	Typ. ⁴	Max	Min	Typ. ⁴	Max	Min	Typ. ⁴	Max	Min	Typ. ⁴	Max		
Command time for configuration set ^{5,7}	Normal program mode (MRPSC, MHSPEN = 0)	t _{PCFG}	—	0.35	8.19 ⁶	—	0.35 ⁶	8.3 ⁶	—	0.37 ²	8.83 ⁶	—	0.39 ⁹	9.42 ⁶	ms	—
	High speed program mode (MRPSC, MHSPEN = 1)		—	0.06 ²⁵⁵	7.85 ⁶	—	0.07 ²⁵	7.96 ⁶	—	0.08 ⁸²	8.5 ⁶	—	0.09 ⁷⁸	9.06 ⁶	ms	—
Update cycle ⁸		N _{UPC}	1000 ⁰⁰ ¹	—	—	100 ⁰⁰⁰ ¹	—	—	100 ⁰⁰⁰ ¹	—	—	100 ⁰⁰⁰ ¹	—	—	Times	—
Data hold time ²		t _{DRP}	10 ² ^{*3}	—	—	10 ² ^{*3}	—	—	10 ² ^{*3}	—	—	10 ² ^{*3}	—	—	Years	Tj=+125°C

Note 1. This is the minimum number of times to guarantee all the characteristics after update. The guaranteed range is from 1 to the minimum value.

Note 2. This indicates the minimum value of the characteristic when update is performed within the specified range.

Note 3. This result is obtained from reliability testing.

Note 4. The reference value at VCC = 3.3 V and room temperature.

Note 5. To calculate the updating time at other frequencies, using approximate formula below listed. (F_{MRPCLK}: frequency of MRPCLK [MHz])

$$t_{PCFG} \text{ (Typ)} = 6.146/F_{MRPCLK} + 0.3133 \text{ [msec]}, t_{PCFG} \text{ (Max)} = 266.5/F_{MRPCLK} + 6.331 \text{ [msec]} \text{ for normal program mode.}$$

$$t_{PCFG} \text{ (Typ)} = 5.184/F_{MRPCLK} + 0.02754 \text{ [msec]}, t_{PCFG} \text{ (Max)} = 267.5/F_{MRPCLK} + 6.025 \text{ [msec]} \text{ for high speed program mode.}$$

Note 6. Values in this table are calculated based on the times of 5-times programming (16 bytes). Timeout values of Figure 60.16 Usage of the Configuration Set command is about 1.1 times of the maximum value (t_{PCFG} + t_{PMC} + Read time (MRPCLK 40cycle)).

Note 7. Read and program operations for the extra MRAM cannot be executed simultaneously. This value is for independent program operation without arbitration between read and program.

Note 8. The update cycle is the number of a configuration set command that can be issued configuration area. Programming the same data to the same address also increases the update cycle count by one.

59. Correction of Table 70.125 MACI command Characteristics

Command time for configuration set will be moved to 70.122, Option Setting Memory (Configuration Setting Area)

Characteristics.

Chapter	RA8P1		RA8D2		RA8M2		RA8T2	
	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page	Chapter/Table/ Figure No	Page
Electrical Characteristics	Table 70.125	4266	Table 69.125	4250	Table 62.118	3867	Table 60.113	3670

Before correction

Table 70.125 MACI command Characteristics

Parameter		Symbol	MRICKL = 125 MHz			MRICKL = 100 MHz			MRICKL = 75 MHz			MRICKL = 66 MHz			Unit	Test conditions
			Min	Typ. 4	Max	Min	Typ. 4	Max	Min	Typ. 4	Max	Min	Typ. 4	Max		
Command time for forced stop command ²		t_{FS}	—	—	3.35 ³	—	—	3.38 ³	—	—	3.47 ³	—	—	3.7 ³	μ s	—
Command time for configuration set ²	Normal program mode (MRPSC, MHSPEN = 0)	t_{PCFG}	—	0.35	8.19 ⁶	—	0.35	8.3 ⁶	—	0.37	8.83 ⁶	—	0.39	9.42 ⁶	ms	—
	High speed program mode (MRPSC, MHSPEN = 1)		—	0.06	7.85 ⁶	—	0.07	7.96 ⁶	—	0.08	8.5 ⁶	—	0.09	9.06 ⁶	ms	—
Command time for increment counter ²		t_{INCC}	—	0.25	1.61 ⁵	—	0.25	1.61 ⁵	—	0.25	1.61 ⁵	—	0.25	1.61 ⁵	ms	—
Command time for read counter ²		t_{RDC}	—	—	0.15	—	—	0.18	—	—	0.24	—	—	0.27	μ s	—

Note 1. The reference value at VCC = 3.3 V and room temperature.

Note 2. To calculate the updating time at other frequencies, using approximate formula below listed. (F_{MRPCLK} : frequency of MRPCLK[MHz])

$$t_{FS} (Max) = 38.62/F_{MRPCLK} + 3.155 [us]$$

$$t_{PCFG} (Typ) = 6.146/F_{MRPCLK} + 0.3133 [msec], t_{PCFG} (Max) = 266.5/F_{MRPCLK} + 6.331 [msec] \text{ for normal program mode.}$$

$$t_{PCFG} (Typ) = 5.184/F_{MRPCLK} + 0.02754 [msec], t_{PCFG} (Max) = 267.5/F_{MRPCLK} + 6.025 [msec] \text{ for high speed program mode.}$$

$$t_{INCC} (Typ) = 0.3348/F_{MRPCLK} + 0.2533 [msec], t_{INCC} (Max) = 0.8698/F_{MRPCLK} + 1.62 [msec]$$

$$t_{RDC} (Max) = 19.13/F_{MRPCLK} + 0.004099 [usec]$$

Note 3. Timeout values of Figure 60.16 Usage of the Configuration Set command is about 1.1 times of the maximum value. (t_{FS} + Read time (MRPCLK 40cycle)).

Note 4. Values in this table are calculated based on the times of 5-times programming (16 bytes). Timeout values of Figure x.x is about 1.1 times of the maximum value (t_{PCFG} + t_{PMC} + Read time (MRPCLK 40cycle)).

Note 5. Values in this table are calculated based on the times of 2-time programming (32 bytes). Timeout values of Figure x.x is about 1.1 times of the maximum value (t_{INCC} + t_{PMC} + Read time (MRPCLK 40cycle)).

Note 6. Counter read time is 100 cycles at MRPCLK. Timeout values of Figure x.x is about 1.1 times of the maximum value (t_{RDC} + Read time (MRPCLK 40cycle)).

After correction

Table 70.125 MACI command Characteristics

Parameter	Symbol	MRICKL = 125 MHz			MRICKL = 100 MHz			MRICKL = 75 MHz			MRICKL = 66 MHz			Unit	Test conditions
		Min	Typ. ⁴	Max	Min	Typ. ⁴	Max	Min	Typ. ⁴	Max	Min	Typ. ⁴	Max		
Command time for forced stop command ²	t_{FS}	—	—	3.35 ³	—	—	3.38 ³	—	—	3.47 ³	—	—	3.7 ³	μs	—
Command time for increment counter ²	t_{INCC}	—	0.25 ²	1.61 ⁴	—	0.25 ²	1.61 ⁴	—	0.25 ²	1.61 ⁴	—	0.25 ²	1.61 ⁴	ms	—
Command time for read counter ²	t_{RDC}	—	—	0.15 ⁶	—	—	0.18 ²	—	—	0.24 ³	—	—	0.27 ⁶	μs	—

Note 1. The reference value at VCC = 3.3 V and room temperature.

Note 2. To calculate the updating time at other frequencies, using approximate formula below listed. (F_{MRPCLK} : frequency of MRPCLK[MHz])

$$t_{FS} (Max) = 38.62/F_{MRPCLK} + 3.155 [us]$$

$$t_{INCC} (Typ) = 0.3348/F_{MRPCLK} + 0.2533 [msec], t_{INCC} (Max) = 0.8698/F_{MRPCLK} + 1.62 [msec]$$

$$t_{RDC} (Max) = 19.13/F_{MRPCLK} + 0.004099 [usec]$$

Note 3. Timeout values of Figure 60.15 Usage of the Forced Stop command is about 1.1 times of the maximum value. (t_{FS} + Read time (MRPCLK 40cycle)).

Note 4. Values in this table are calculated based on the times of 2-time programming (32 bytes). Timeout values of Figure 60.17 Usage of the Increment Counter command is about 1.1 times of the maximum value (t_{INCC} + t_{PMC} + Read time (MRPCLK 40cycle)).

Note 5. Counter read time is 100 cycles at MRPCLK. Timeout values of Figure 60.18 Usage of the Read Counter command is about 1.1 times of the maximum value (t_{RDC} + Read time (MRPCLK 40cycle)).

Reference document

Applicable Product	Manual Title	Document Number
RA8P1	RA8P1 Group User's Manual: Hardware Rev. 1.20	R01UH1064EJ0120
RA8D2	RA8D2 Group User's Manual: Hardware Rev. 1.20	R01UH1065EJ0120
RA8M2	RA8M2 Group User's Manual: Hardware Rev. 1.20	R01UH1066EJ0120
RA8T2	RA8T2 Group User's Manual: Hardware Rev. 1.20	R01UH1067EJ0120