To our customers,

# Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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# RENESAS TECHNICAL UPDATE

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RenesasTechnology Corp.

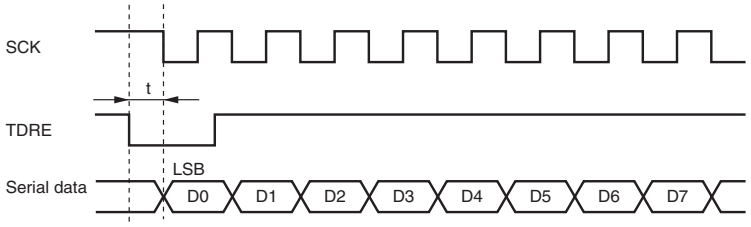
| Product Category | MPU&MCU | | Document No. | TN-H8*-A289A/E | Rev. | 1.0 |
|---|---|---|---|---|---|---|
| Title | Additional of SCI Usage Notes | | Information Category | Technical Notification | | |
| Applicable Product | H8S/2282 Group<br>H8S/2612 series<br>H8S/2628 series<br>H8S/2615 Group | Lot No.<br>All | Reference Document | H8S/2282 Group hardware manual (Rev.2.00 2004.3 REJ09B0148-0200Z)<br>H8S/2612 series, H8S/2612 F-ZTAT™ hardware manual (Rev.4.0 2003.3 ADE-602-220C)<br>H8S/2628 series hardware manual (Rev.2.00 2004.3 REJ09B0155-0200O)<br>H8S/2615 Group hardware manual (Rev.2.00 2004.3 REJ09B0072-0200O) | | |

The descriptions are dropped in the hardware manuals for the H8S Series is amended as shown below.

### 14.9.5 Restrictions on Using DTC

When the external clock source is used as a synchronization clock, update TDR by the DTC and wait for at least five φ clock cycles before allowing the transmit clock to be input. If the transmit clock is input within four clock cycles after TDR modification, the SCI may malfunction (figure 14.33).

When using the DTC to read RDR, be sure to set the receive end interrupt source (RXI) as a DTC activation source.




Note: When external clock is supplied, t must be more than four clock cycles.

**Figure 14.33 Sample Transmission using DTC in Clocked Synchronous Mode**

### 14.9.6 SCI Operations during Mode Transitions

**Transmission:** Before making the transition to module stop, software standby, watch, sub-active, or sub-sleep mode, stop all transmit operations (TE = TIE = TEIE = 0). TSR, TDR, and SSR are reset. The states of the output pins during each mode depend on the port settings, and the pins output a high-level signal after mode is cancelled and then the TE is set to 1 again. If the transition is made during data transmission, the data being transmitted will be undefined.

To transmit data in the same transmission mode after mode cancellation, set TE to 1, read SSR, write to TDR, clear TDRE in this order, and then start transmission. To transmit data in a different transmission mode, initialize the SCI first.

Figure 14.34 shows a sample flowchart for mode transition during transmission. Figures 14.35 and 14.36 show the pin states during transmission.

Before making the transition from the transmission mode using DTC transfer to module stop, software standby, watch, sub-active, or sub-sleep mode, stop all transmit operations (TE = TIE = TEIE = 0). Setting TE and TIE to 1 after mode

cancellation generates a TXI interrupt request to start transmission using the DTC.

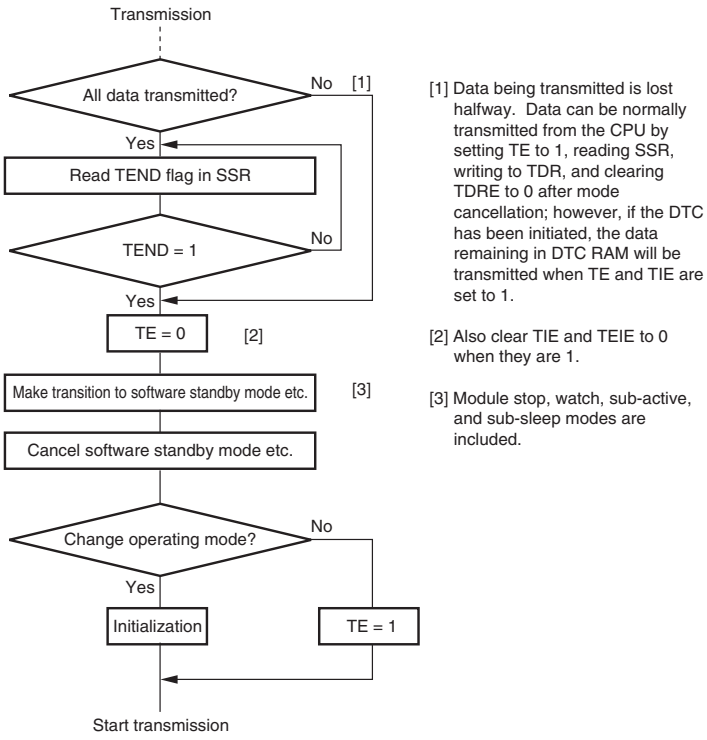



**Figure 14.34 Sample Flowchart for Mode Transition during Transmission**

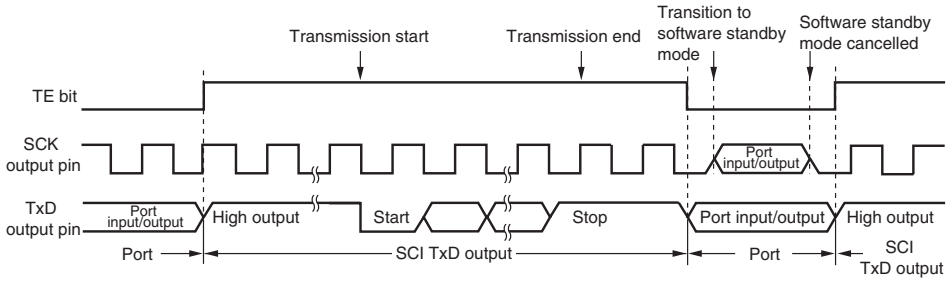



**Figure 14.35 Pin States during Transmission in Asynchronous Mode (Internal Clock)**

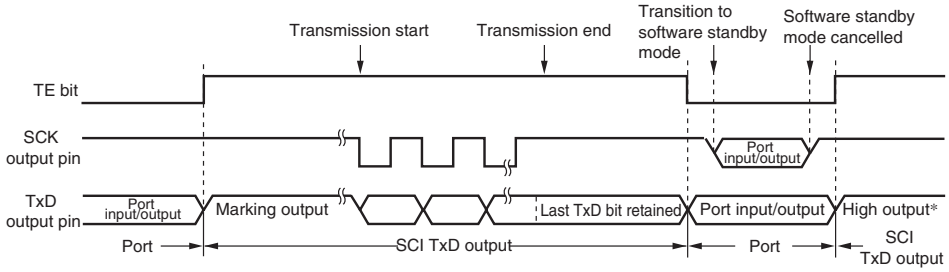



**Figure 14.36 Pin States during Transmission in Clocked Synchronous Mode (Internal Clock)**

**Reception:** Before making the transition to module stop, software standby, watch, sub-active, or sub-sleep mode, stop reception (RE = 0). RSR, RDR, and SSR are reset. If transition is made during data reception, the data being received will be invalid.

To receive data in the same reception mode after mode cancellation, set RE to 1, and then start reception. To receive data in a different reception mode, initialize the SCI first.

Figure 14.37 shows a sample flowchart for mode transition during reception.

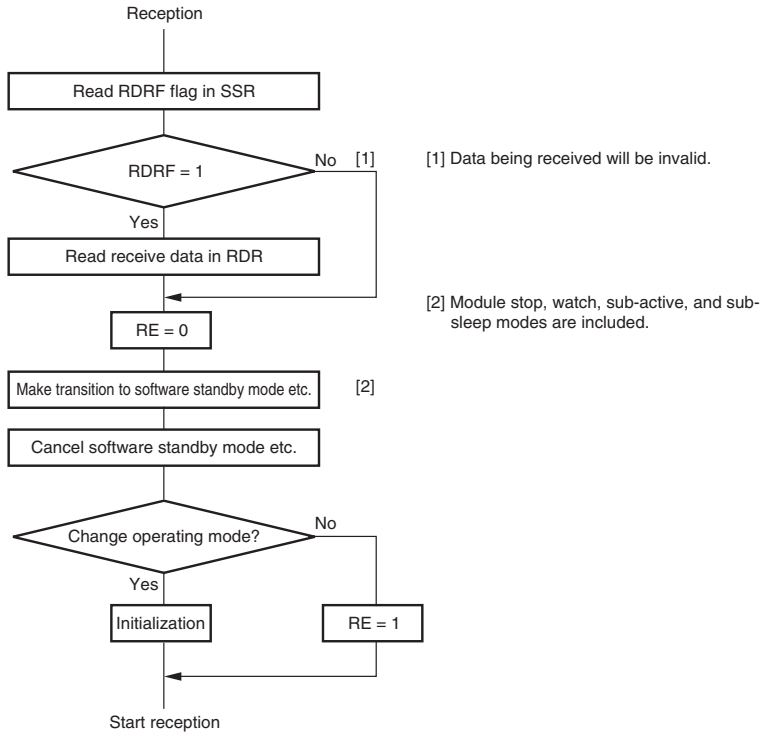



**Figure 14.37 Sample Flowchart for Mode Transition during Reception**

### 14.9.7 Notes when Switching from SCK Pin to Port Pin

- Problem in Operation: When DDR and DR are set to 1, SCI clock output is used in clocked synchronous mode, and the SCK pin is changed to the port pin while transmission is ended, port output is enabled after low-level output occurs for one half-cycle.

  When switching the SCK pin to the port pin by making the following settings while DDR = 1, DR = 1, C/A = 1, CKE1 = 0, CKE0 = 0, and TE = 1, low-level output occurs for one half-cycle.

1. End of serial data transmission
2. TE bit = 0
3. C/A bit = 0 ... switchover to port output
4. Occurrence of low-level output (see figure 14.38)

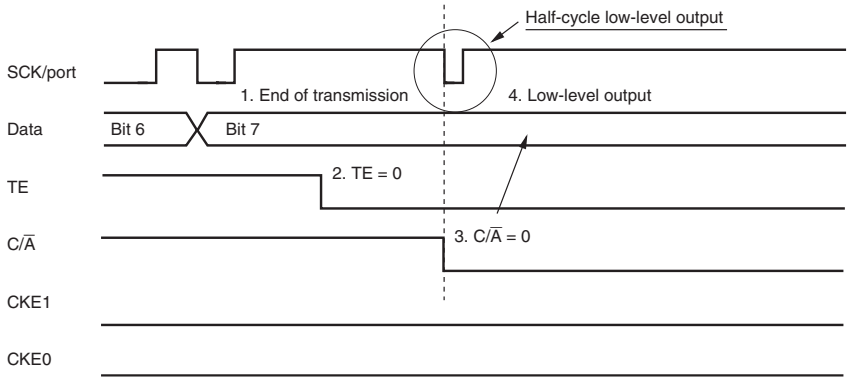



**Figure 14.38 Operation when Switching from SCK Pin to Port Pin**

- Usage Note: To prevent low-level output occurred when switching the SCK pin to port pin, follow the procedure described below.

  As this sample procedure temporarily places the SCK pin in the input state, the SCK/port pin should be pulled up beforehand with an external circuit.

  With DDR = 1, DR = 1, C/A = 1, CKE1 = 0, CKE0 = 0, and TE = 1, make the following settings in the order shown.

1. End of serial data transmission
2. TE bit = 0
3. CKE1 bit = 1
4. C/A bit = 0 ... switchover to port output
5. CKE1 bit = 0

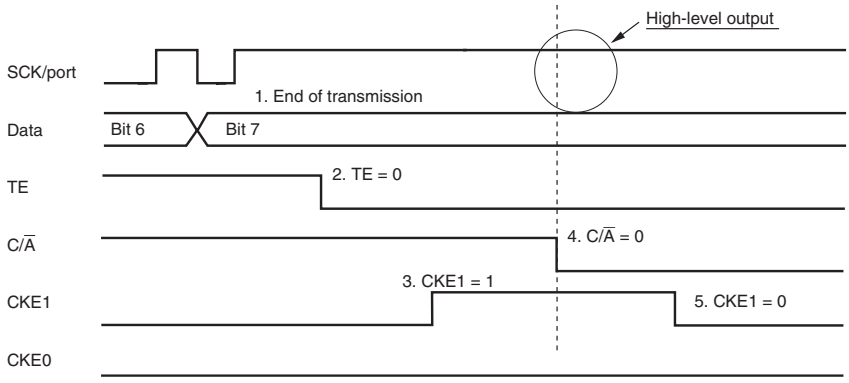



**Figure 14.39 Operation when Switching from SCK Pin to Port Pin (Example of Preventing Low-Level Output)**