Date: Dec. 19, 2023

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0130A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G16 Descriptions in the User's Manual: Hardware Rev. 1.10 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G16 Group	Lot No. All lots	Reference Document	RL78/G16 User's Manual: Hardware Rev. 1.10 R01UH0980EJ0110 (Aug. 2023)		

This document describes misstatements found in the RL78/G16 User's Manual: Hardware Rev. 1.10 (R01UH0980EJ0110).

Corrections

Applicable Item	Applicable Page	Contents
1.2 List of Part Numbers	Page 25, Page 26	Incorrect descriptions revised
4.5.3 Register setting examples for used port and alternate functions	Page 158, Page 160	Incorrect descriptions revised
17.3.2 STOP mode	Page 796 to Page 798	Incorrect descriptions revised
18.1 Timing of Reset Operation	Page 803	Incorrect descriptions revised
19.3 Operation of Selectable Power-on-reset Circuit	Page 813	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0980EJ 0110	
1	1.2 List of Part Numbers		Page 25, Page 26	Page 3
2	4.5.3 Register setting examples for used port and alternate functions		Page 158, Page 160	Page 4
3	17.3.2 STOP mode		Page 796 to Page 798	Page 5, Page 6
4	18.1 Timing of Reset Operation		Page 803	Page 7
5	19.3 Operation of Selectable Power-on-reset Circuit		Page 813	Page 8

Incorrect: Bold with underline; Correct: Gray hatched

Revision History No,

RL78/G16 Correction for incorrect description notice

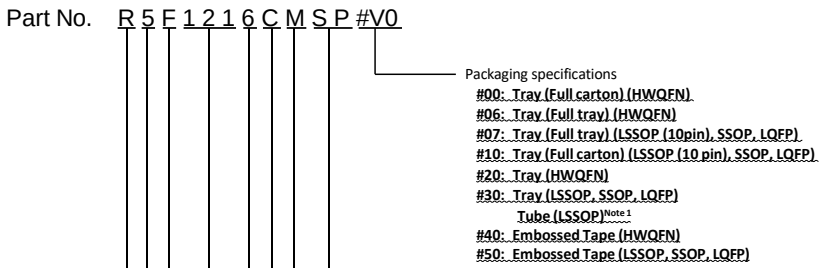
Document Number	Issue Date	Description
TN-RL*-A0130A/E	Dec. 19, 2023	First edition issued Corrections No.1 to No.5 revised (this document)

1. 1.2 List of Part Numbers (page 25, page 26)

Incorrect:

(page 25)

Figure 1-1. Part Number, Memory Size, and Package of RL78/G16



(omitted)

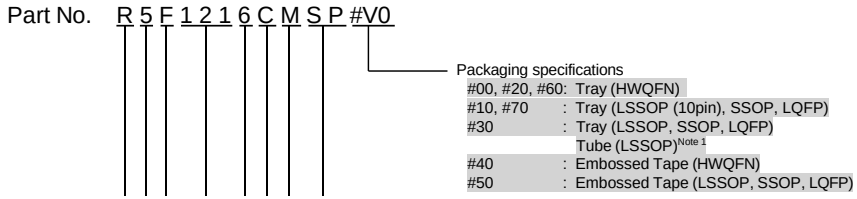
(page 26)

Table 1-1. List of Ordering Part Numbers

Pin count	Package	Fields of Application Note 1	Ordering Part Number		RENESAS Code
			Product Name	Packaging Specifications	
10 pins	10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65-mm pitch)	A	R5F1211CASP, R5F1211AASP	#07, #10, #30, #50	PLSP0010JA-A
		G	R5F1211CGSP, R5F1211AGSP		
		M	R5F1211CMSP, R5F1211AMSP		
16 pins	16-pin plastic SSOP (4.4 × 5.0 mm, 0.65-mm pitch)	A	R5F1214CASP, R5F1214AASP	#07, #10, #30, #50	PRSP0016JC-B
		G	R5F1214CGSP, R5F1214AGSP		
		M	R5F1214CMSP, R5F1214AMSP		
16 pins	16-pin plastic HWQFN (3 × 3 mm, 0.5-mm pitch)	A	R5F1214CANA, R5F1214AANA	#00, #06, #20, #40	PWQN0016KD-A
		G	R5F1214CGNA, R5F1214AGNA		
		M	R5F1214CMNA, R5F1214AMNA		
20 pins	20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch)	A	R5F1216CASP, R5F1216AASP	#30, #50	PLSP0020JB-A
		G	R5F1216CGSP, R5F1216AGSP		
		M	R5F1216CMSP, R5F1216AMSP		
24 pins	24-pin plastic HWQFN (4.0 × 4.0 mm, 0.5-mm pitch)	A	R5F1217CANA, R5F1217AANA	#00, #06, #20, #40	PWQN0024KF-A
		G	R5F1217CGNA, R5F1217AGNA		
		M	R5F1217CMNA, R5F1217AMNA		
32 pins	32-pin plastic HWQFN (5.0 × 5.0 mm, 0.5-mm pitch)	A	R5F121BCANA, R5F121BAANA	#00, #06, #20, #40	PWQN0032KE-A
		G	R5F121BCGNA, R5F121BAGNA		
		M	R5F121BCMNA, R5F121BAMNA		
32 pins	32-pin plastic LQFP (7.0 × 7.0 mm, 0.8-mm pitch)	A	R5F121BCAFP, R5F121BAAFP	#07, #10, #30, #50	PLQP0032GB-A
		G	R5F121BCGFP, R5F121BAGFP		
		M	R5F121BCMFP, R5F121BAMFP		

Correct:

Figure 1-1. Part Number, Memory Size, and Package of RL78/G16



(omitted)

Table 1-1. List of Ordering Part Numbers

Pin count	Package	Fields of Application Note 1	Ordering Part Number		RENESAS Code
			Product Name	Packaging Specifications	
10 pins	10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65-mm pitch)	A	R5F1211CASP, R5F1211AASP	#70, #10, #30, #50	PLSP0010JA-A
		G	R5F1211CGSP, R5F1211AGSP		
		M	R5F1211CMSP, R5F1211AMSP		
16 pins	16-pin plastic SSOP (4.4 × 5.0 mm, 0.65-mm pitch)	A	R5F1214CASP, R5F1214AASP	#70, #10, #30, #50	PRSP0016JC-B
		G	R5F1214CGSP, R5F1214AGSP		
		M	R5F1214CMSP, R5F1214AMSP		
16 pins	16-pin plastic HWQFN (3 × 3 mm, 0.5-mm pitch)	A	R5F1214CANA, R5F1214AANA	#00, #60, #20, #40	PWQN0016KD-A
		G	R5F1214CGNA, R5F1214AGNA		
		M	R5F1214CMNA, R5F1214AMNA		
20 pins	20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch)	A	R5F1216CASP, R5F1216AASP	#30, #50	PLSP0020JB-A
		G	R5F1216CGSP, R5F1216AGSP		
		M	R5F1216CMSP, R5F1216AMSP		
24 pins	24-pin plastic HWQFN (4.0 × 4.0 mm, 0.5-mm pitch)	A	R5F1217CANA, R5F1217AANA	#00, #60, #20, #40	PWQN0024KF-A
		G	R5F1217CGNA, R5F1217AGNA		
		M	R5F1217CMNA, R5F1217AMNA		
32 pins	32-pin plastic HWQFN (5.0 × 5.0 mm, 0.5-mm pitch)	A	R5F121BCANA, R5F121BAANA	#00, #60, #20, #40	PWQN0032KE-A
		G	R5F121BCGNA, R5F121BAGNA		
		M	R5F121BCMNA, R5F121BAMNA		
32 pins	32-pin plastic LQFP (7.0 × 7.0 mm, 0.8-mm pitch)	A	R5F121BCAFP, R5F121BAAFP	#70, #10, #30, #50	PLQP0032GB-A
		G	R5F121BCGFP, R5F121BAGFP		
		M	R5F121BCMFP, R5F121BAMFP		

2. 4.5.3 Register setting examples for used port and alternate functions (page 158, page 160)

Incorrect:

(page 158)

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (4/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	Function Name	I/O							SAU Output Function	Other than SAU					
P03	P03	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	✓
		Output	—	×	0	0	0/1	0	(SO00/TxD0) = 1 Note 1	TO00 = 0 (TO05) = 0 Note 1 SCLA0 = 0 Note 5					
		N-ch open	—	1	0	0	0/1	0							
	(SO00)	Output	PIOR21 = 1 PIOR20 = 0	0/1	0	0	1	0	×	TO00 = 0 TO05 = 0 Note 1 SCLA0 = 0 Note 5	✓	✓	✓	✓	—
	(TxD0)	Output		0/1	0	0	1	0	×		✓	✓	✓	✓	—
	RxD1	Input	PIOR31 = 0 PIOR30 = 0	×	0	1	1	0	×	×	✓	✓	✓	✓	—
	SCLA0	I/O	PIOR32 = 0	1	0	0	0	0	×	TO00 = 0 (TO05) = 0 Note 1	—	—	—	—	✓

(page 160)

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (6/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	Function Name	I/O							SAU Output Function	Other than SAU					
P07	P07	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output	—	0	0	0	0/1	0	SCK11/SCL11 = 1	VCOUT1 = 0 (TO03) = 0 TO04 = 0 SDAA0 = 0 Note 6 (SDAA0) = 0 Note 3					
		N-ch open drain output	—	1	0	0	0/1	0							
P10	P10	Input	—	—	—	1	×	—	×	×	✓	✓	—	—	—
		Output	—	—	—	0	0/1	—	(SCK11/SCL11) = 1	(TO03) = 0 (PCLBUZ0) = 0					
	INTP8	Input	PIOR56 = 0	—	—	1	×	—	×	×	✓	✓	—	—	—
	(TI03)	Input	PIOR12 = 1 PIOR11 = 0 PIOR10 = 0	—	—	1	×	—	—	×	✓	✓	—	—	—
	(TO03)	Output		—	—	0	0	—	×	(PCLBUZ0) = 0	✓	✓	—	—	—
	(RxD1)	Input	PIOR31 = 1 PIOR30 = 0	—	—	0	1	—	×	×	✓	✓	—	—	—
	(PCLBUZ0)	Output	PIOR62 = 0 PIOR61 = 1 PIOR60 = 1	—	—	0	0	—	×	(TO03) = 0	✓	✓	—	—	—
	(SCK11)	Input	PIOR24 = 1 PIOR23 = 0 PIOR22 = 0	—	—	1	×	—	×	×	✓	✓	—	—	—
		Output		—	—	0	1	—	×	(TO03) = 0 (PCLBUZ0) = 0					
	(SCL11)	Output		—	—	0	1	—			✓	✓	—	—	—

Correct:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (4/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	Function Name	I/O							SAU Output Function	Other than SAU					
P03	P03	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	✓
		Output	—	×	0	0	0/1	0	(SO00/TxD0) = 1 Note 1	TO00 = 0 (TO05) = 0 Note 1 SCLA0 = 0 Note 5					
		N-ch open	—	1	0	0	0/1	0							
	(SO00)	Output	PIOR21 = 1 PIOR20 = 0	0/1	0	0	1	0	×	TO00 = 0 TO05 = 0 Note 1 SCLA0 = 0 Note 5	✓	✓	✓	✓	—
	(TxD0)	Output		0/1	0	0	1	0	×		✓	✓	✓	✓	—
	RxD1	Input	PIOR31 = 0 PIOR30 = 0	×	0	1	×	0	×	×	✓	✓	✓	✓	—
	SCLA0	I/O	PIOR32 = 0	1	0	0	0	0	×	TO00 = 0 (TO05) = 0 Note 1	—	—	—	—	✓

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (6/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	Function Name	I/O							SAU Output Function	Other than SAU					
P07	P07	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output	—	0	0	0	0/1	0	SCK11/SCL11 = 1	VCOUT1 = 0 (TO03) = 0 TO04 = 0 SDAA0 = 0 Note 6 (SDAA0) = 0 Note 3					
		N-ch open drain output	—	1	0	0	0/1	0							
P10	P10	Input	—	—	—	1	×	—	×	×	✓	✓	—	—	—
		Output	—	—	—	0	0/1	—	(SCK11/SCL11) = 1	(TO03) = 0 (PCLBUZ0) = 0					
	INTP8	Input	PIOR56 = 0	—	—	1	×	—	×	×	✓	✓	—	—	—
	(TI03)	Input	PIOR12 = 1 PIOR11 = 0 PIOR10 = 0	—	—	1	×	—	—	×	✓	✓	—	—	—
	(TO03)	Output		—	—	0	0	—	×	(PCLBUZ0) = 0	✓	✓	—	—	—
	(RxD1)	Input	PIOR31 = 1 PIOR30 = 0	—	—	1	×	—	×	×	✓	✓	—	—	—
	(PCLBUZ0)	Output	PIOR62 = 0 PIOR61 = 1 PIOR60 = 1	—	—	0	0	—	×	(TO03) = 0	✓	✓	—	—	—
	(SCK11)	Input	PIOR24 = 1 PIOR23 = 0 PIOR22 = 0	—	—	1	×	—	×	×	✓	✓	—	—	—
		Output		—	—	0	1	—	×	(TO03) = 0 (PCLBUZ0) = 0					
	(SCL11)	Output		—	—	0	1	—			✓	✓	—	—	—

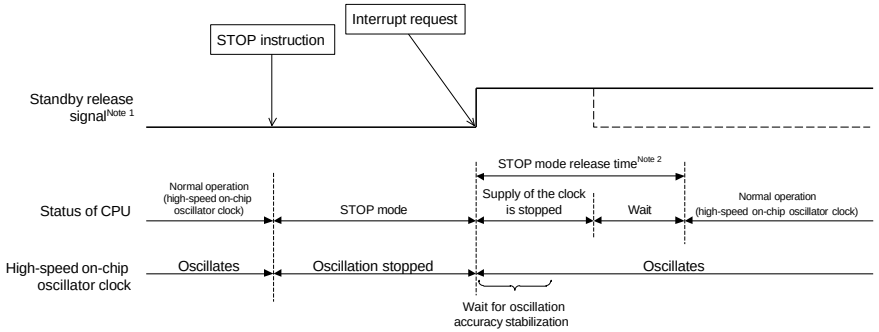
3. 17.3.2 STOP mode (page 796 to page 798)

Incorrect:

(page 796)

Figure 17-3. STOP Mode Release by Interrupt Request Generation (1/3)

(1) When high-speed on-chip oscillator clock is used as CPU clock



Note 1. For details of the standby release signal, see **Figure 16-1 Basic Configuration of Interrupt Function**.

Note 2. STOP mode release time: Supply of the clock is stopped: **TBD** µs (TYP.)

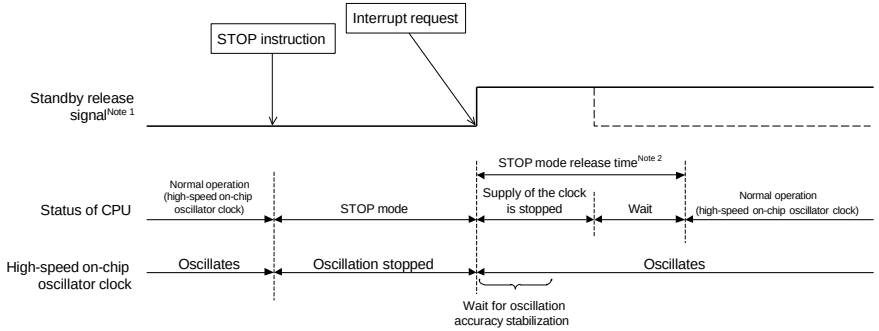
[Wait]

- When vectored interrupt servicing is carried out: 8 clocks
- When vectored interrupt servicing is not carried out: 2 clocks

Correct:

Figure 17-3. STOP Mode Release by Interrupt Request Generation (1/3)

(1) When high-speed on-chip oscillator clock is used as CPU clock



Note 1. For details of the standby release signal, see **Figure 16-1 Basic Configuration of Interrupt Function**.

Note 2. STOP mode release time: Supply of the clock is stopped: 27 µs (TYP.)

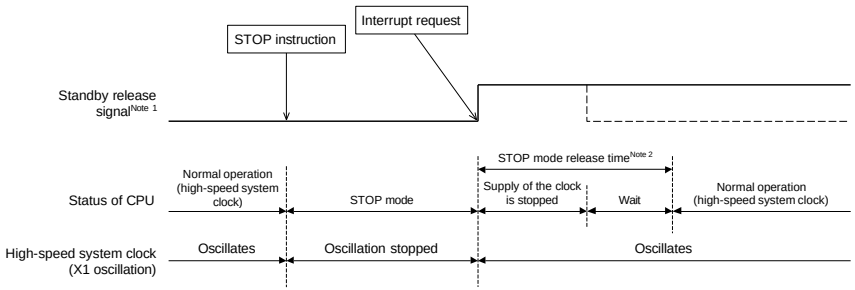
[Wait]

- When vectored interrupt servicing is carried out: 8 clocks
- When vectored interrupt servicing is not carried out: 2 clocks

(page 797)

Figure 17-3. STOP Mode Release by Interrupt Request Generation (2/3)

(2) When high-speed system clock (X1 oscillation) is used as CPU clock (Other than 10-pin products)



Note 1. For details of the standby release signal, see **Figure 16-1 Basic Configuration of Interrupt Function**.

Note 2. STOP mode release time: Whichever is longer, **TBD** µs (TYP.) or the oscillation stabilization time (set by OSTS)

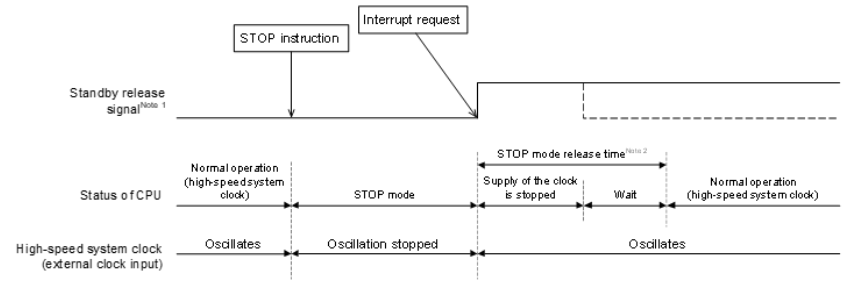
[Wait]

- When vectored interrupt servicing is carried out: 10 or 11 clocks
- When vectored interrupt servicing is not carried out: 4 or 5 clocks

(page 798)

Figure 17-3. STOP Mode Release by Interrupt Request Generation (3/3)

(3) When high-speed system clock (external clock input) is used as CPU clock (Other than 10-pin products)



Note 1. For details of the standby release signal, see **Figure 16-1 Basic Configuration of Interrupt Function**.

Note 2. STOP mode release time

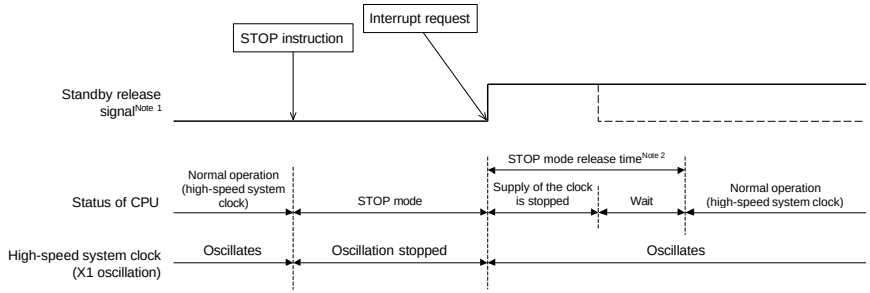
Supply of the clock is stopped: **To be determined (µs)**

[Wait]

- When vectored interrupt servicing is carried out: 8 clocks
- When vectored interrupt servicing is not carried out: 2 clocks

Figure 17-3. STOP Mode Release by Interrupt Request Generation (2/3)

(2) When high-speed system clock (X1 oscillation) is used as CPU clock (Other than 10-pin products)



Note 1. For details of the standby release signal, see **Figure 16-1 Basic Configuration of Interrupt Function**.

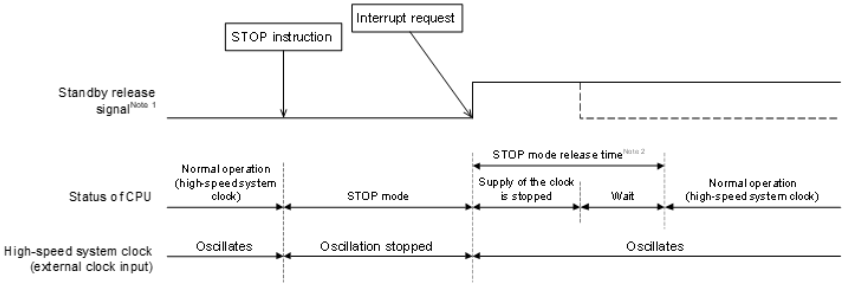
Note 2. STOP mode release time: Whichever is longer, 27 µs (TYP.) or the oscillation stabilization time (set by OSTS)

[Wait]

- When vectored interrupt servicing is carried out: 10 or 11 clocks
- When vectored interrupt servicing is not carried out: 4 or 5 clocks

Figure 17-3. STOP Mode Release by Interrupt Request Generation (3/3)

(3) When high-speed system clock (external clock input) is used as CPU clock (Other than 10-pin products)



Note 1. For details of the standby release signal, see **Figure 16-1 Basic Configuration of Interrupt Function**.

Note 2. STOP mode release time

Supply of the clock is stopped: 27 µs

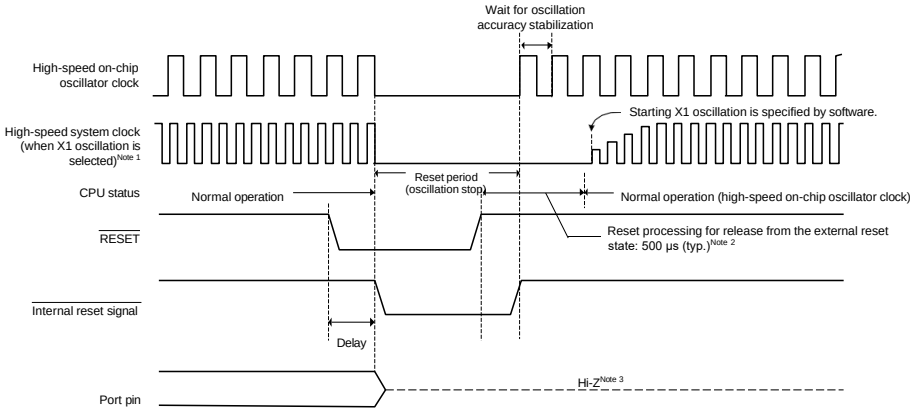
[Wait]

- When vectored interrupt servicing is carried out: 8 clocks
- When vectored interrupt servicing is not carried out: 2 clocks

4. 18.1 Timing of Reset Operation (page 803)

Incorrect:

Figure 18-2. Timing of Reset by $\overline{\text{RESET}}$ Input



Note 1. Other than 10-pin products.

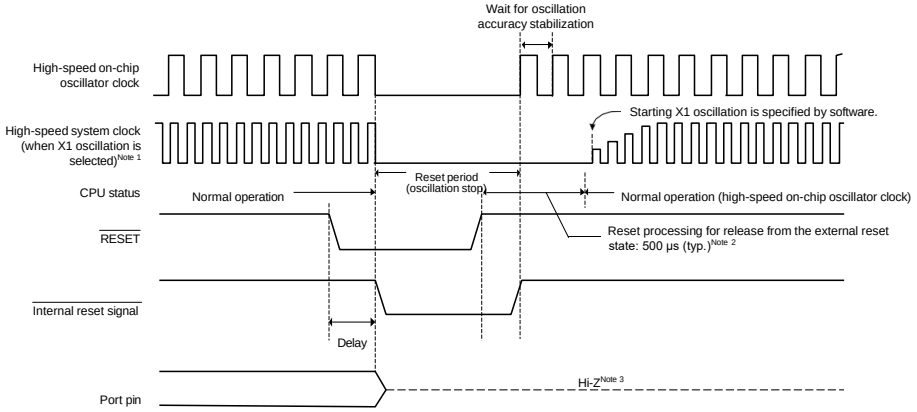
Note 2. After power is supplied, an SPOR reset processing time of **TBD** (MAX.) is required before reset processing starts after release of the external reset.

Note 3. Status of port pin P40 is as follows.

- High-impedance during external reset period or reset period by the data retention power supply voltage
- High level after receiving a reset (connected to the internal pull-up resistor)

Correct:

Figure 18-2. Timing of Reset by $\overline{\text{RESET}}$ Input



Note 1. Other than 10-pin products.

Note 2. After power is supplied, an SPOR reset processing time of 3.01ms (MAX.) is required before reset processing starts after release of the external reset.

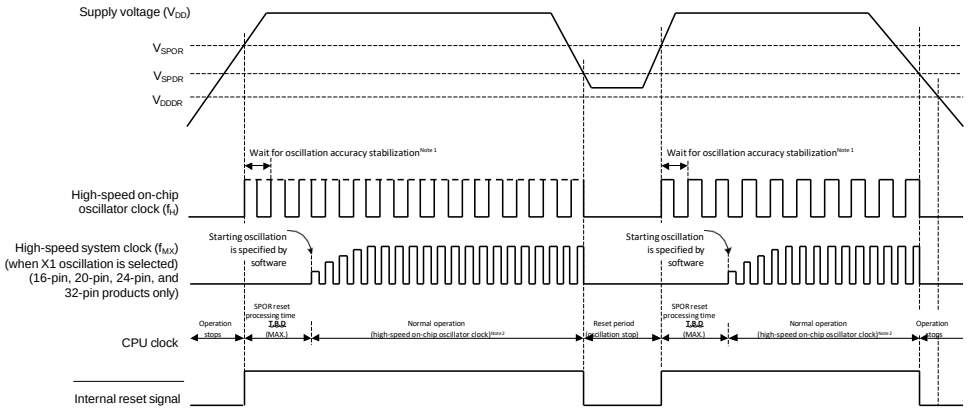
Note 3. Status of port pin P40 is as follows.

- High-impedance during external reset period or reset period by the data retention power supply voltage
- High level after receiving a reset (connected to the internal pull-up resistor)

5. 19.3 Operation of Selectable Power-on-reset Circuit (page 813)

Incorrect:

Figure 19-2. Timing of Internal Reset Signal Generation



Correct:

Figure 19-2. Timing of Internal Reset Signal Generation