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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0149A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/L23 Descriptions in the User's Manual: Hardware Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/L23 Group	Lot No. All lots	Reference Document	RL78/L23 User's Manual: Hardware Rev. 1.00 R01UH1082EJ0100 (May 2025)		

This document describes misstatements found in the RL78/L23 User's Manual: Hardware Rev. 1.00 (R01UH1082EJ0100).

Corrections

Applicable Item	Applicable Page	Contents
Table 3 - 6 List of 2nd Special Function Registers	Page 179	Correction of errors
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6.3.1 Clock operation mode control register (CMC)	Page 312, Page 313	Correction of errors
6.3.2 Main oscillator oscillation mode select register (MODRV)	Page 314	Correction of errors
35.2.4 CTSU control registers BL and BH (CTSUCRBL, CTSUCRBH)	Page 1533	Correction of errors
35.4.2 TSCAP pin	Page 1566	Addition of descriptions
42.3.2 Supply current characteristics	Page 1705, Page 1708 to Page 1710	Correction of errors

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH1082EJ0100	
1	Table 3 - 6 List of 2nd Special Function Registers		Page 179	Page 3
2	Table 4 - 6 Examples of Register and Output Latch Settings for Alternate Functions		Page 255	Page 4
3	6.3.1 Clock operation mode control register (CMC)		Page 312, Page 313	Page 5, Page 6
4	6.3.2 Main oscillator oscillation mode select register (MODRV)		Page 314	Page 7
5	35.2.4 CTSU control registers BL and BH (CTSUCRBL, CTSUCRBH)		Page 1533	Page 8
6	35.4.2 TSCAP pin		Page 1566	Page 9
7	42.3.2 Supply current characteristics		Page 1705, Page 1708 to Page 1710	Page 10 to Page 13

Incorrect: Bold with wavy underline; Correct: Gray shaded

Revision History

RL78/L23 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0149A/E	Oct. 7, 2025	First edition issued Corrections of errors stated in No.1 to No.7 (of this document)

1. Table 3 - 6 List of 2nd Special Function Registers (Page 179)

Incorrect:

Table 3 - 6 List of 2nd Special Function Registers (14/19)

Address	Extended Special Function Register (2nd SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F050AH	CTSU measurement channel register H	CTSUMFAF	CTSUMCHH	R/W	✓	✓	✓	0000H
F050BH		—			—	—		
F050CH	CTSU channel enable control register AL	CTSUCHAC0	CTSUCHACAL	R/W	✓	✓	✓	0000H
F050DH		CTSUCHAC1			✓	✓		
F050EH	CTSU channel enable control register AH	CTSUCHAC2	CTSUCHACAH	R/W	✓	✓	✓	0000H
F050FH		CTSUCHAC3			✓	✓		
F0510H	CTSU channel enable control register BL	CTSUCHAC4	CTSUCHACBL	R/W	✓	✓	✓	0000H
F0511H		CTSUCHAC5			✓	✓		
F0514H	CTSU channel transmit/receive control register AL	CTSUCHTRC0	CTSUCHTRCAL	R/W	✓	✓	✓	0000H
F0515H		CTSUCHTRC1			✓	✓		
F0516H	CTSU channel transmit/receive control register AH	CTSUCHTRC2	CTSUCHTRCAH	R/W	✓	✓	✓	0000H
F0517H		CTSUCHTRC3			✓	✓		
F0518H	CTSU channel transmit/receive control register BL	CTSUCHTRC4	CTSUCHTRCBL	R/W	✓	✓	✓	0000H
F0519H		CTSUCHTRC5			✓	✓		
F0558H	8-bit interval timer counter register 10	TRT10	TRT1	R	—	✓	✓	00H
F0559H	8-bit interval timer counter register 11	TRT11		R	—	✓		00H

Correct:

Table 3 - 6 List of 2nd Special Function Registers (14/19)

Address	Extended Special Function Register (2nd SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F050AH	CTSU measurement channel register H	CTSUMFAF	CTSUMCHH	R/W	✓	✓	✓	0000H
F050BH		—			—	—		
F050CH	CTSU channel enable control register AL	CTSUCHAC0	CTSUCHACAL	R/W	✓	✓	✓	0000H
F050DH		CTSUCHAC1			✓	✓		
F050EH	CTSU channel enable control register AH	CTSUCHAC2	CTSUCHACAH	R/W	✓	✓	✓	0000H
F050FH		CTSUCHAC3			✓	✓		
F0510H	CTSU channel enable control register BL	CTSUCHAC4	CTSUCHACBL	R/W	✓	✓	✓	0000H
F0511H		—			—	—		
F0514H	CTSU channel transmit/receive control register AL	CTSUCHTRC0	CTSUCHTRCAL	R/W	✓	✓	✓	0000H
F0515H		CTSUCHTRC1			✓	✓		
F0516H	CTSU channel transmit/receive control register AH	CTSUCHTRC2	CTSUCHTRCAH	R/W	✓	✓	✓	0000H
F0517H		CTSUCHTRC3			✓	✓		
F0518H	CTSU channel transmit/receive control register BL	CTSUCHTRC4	CTSUCHTRCBL	R/W	✓	✓	✓	0000H
F0519H		—			—	—		
F0558H	8-bit interval timer counter register 10	TRT10	TRT1	R	—	✓	✓	00H
F0559H	8-bit interval timer counter register 11	TRT11		R	—	✓		00H

2. Table 4 - 6 Examples of Register and Output Latch Settings for Alternate Functions (Page 255)

Incorrect:

Table 4 - 6 Examples of Register and Output Latch Settings for Alternate Functions (10/46)

Pin Name	Used Function		PIORx	POMxx	PMCAxx	PMxx	Pxx	PFSEGx (PFCOMy/PFSEGz) or ISCLCD (ISCVLx/ISCCAP) Note 1	Alternate Function Output		44-Pin	48-Pin	52-Pin	64-Pin	80-Pin	100-Pin
	Function Name	Input/Output							SAU and UARTA (Excluding Clock Output of UARTA)	Other than SAU and UARTA (Including Clock Output of UARTA)						
P20	P20	Input	—	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
		Output	—	—	0	0	0/1	—	—	(PCLBUZ1) = 0	✓	✓	✓	✓	✓	✓
	ANI1	Analog input	—	—	1	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	AVREFM	Reference voltage	—	—	1	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	EI20	Input	—	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	(TI00)	Input	PIOR01 = 0 PIOR00 = 1	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	(INTP7)	Input	PIOR95 = 0 PIOR94 = 0 PIOR93 = 1	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	(PCLBUZ1)	Output	PIOR52 = 0 PIOR51 = 1 PIOR50 = 0	—	0	0	0	—	—	—	✓	✓	✓	✓	✓	✓
P21	P21	Input	—	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
		Output	—	—	0	0	0/1	—	—	(TO00) = 0 (PCLBUZ0) = 0	✓	✓	✓	✓	✓	✓
	ANI0	Analog input	—	—	1	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	AVREFP	Reference voltage	—	—	1	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	VBAT1	Input	—	—	0	0	1	—	—	—	✓	✓	✓	✓	✓	✓
	EI21	Input	—	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	(TO00)	Output	PIOR01 = 0 PIOR00 = 1	—	0	0	0	—	—	(PCLBUZ0) = 0	✓	✓	✓	✓	✓	✓
	(INTP6)	Input	PIOR92 = 0 PIOR91 = 1 PIOR90 = 0	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	(PCLBUZ0)	Output	PIOR52 = 0 PIOR51 = 1 PIOR50 = 1	—	0	0	0	—	—	(TO00) = 0	✓	✓	✓	✓	✓	✓

Correct:

Table 4 - 6 Examples of Register and Output Latch Settings for Alternate Functions (10/46)

Pin Name	Used Function		PIORx	POMxx	PMCAxx	PMxx	Pxx	PFSEGx (PFCOMy/PFSEGz) or ISCLCD (ISCVLx/ISCCAP) Note 1	Alternate Function Output		44-Pin	48-Pin	52-Pin	64-Pin	80-Pin	100-Pin
	Function Name	Input/Output							SAU and UARTA (Excluding Clock Output of UARTA)	Other than SAU and UARTA (Including Clock Output of UARTA)						
P20	P20	Input	—	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
		Output	—	—	0	0	0/1	—	—	(PCLBUZ1) = 0	✓	✓	✓	✓	✓	✓
	ANI1	Analog input	—	—	1	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	AVREFM	Reference voltage	—	—	1	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	EI20	Input	—	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	(TI00)	Input	PIOR01 = 0 PIOR00 = 1	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	(INTP7)	Input	PIOR95 = 0 PIOR94 = 0 PIOR93 = 1	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	(PCLBUZ1)	Output	PIOR52 = 0 PIOR51 = 1 PIOR50 = 0	—	0	0	0	—	—	—	✓	✓	✓	✓	✓	✓
P21	P21	Input	—	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
		Output	—	—	0	0	0/1	—	—	(TO00) = 0 (PCLBUZ0) = 0	✓	✓	✓	✓	✓	✓
	ANI0	Analog input	—	—	1	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	AVREFP	Reference voltage	—	—	1	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	VBAT1	—	—	—	1	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	EI21	Input	—	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	(TO00)	Output	PIOR01 = 0 PIOR00 = 1	—	0	0	0	—	—	(PCLBUZ0) = 0	✓	✓	✓	✓	✓	✓
	(INTP6)	Input	PIOR92 = 0 PIOR91 = 1 PIOR90 = 0	—	0	1	×	—	—	—	✓	✓	✓	✓	✓	✓
	(PCLBUZ0)	Output	PIOR52 = 0 PIOR51 = 1 PIOR50 = 1	—	0	0	0	—	—	(TO00) = 0	✓	✓	✓	✓	✓	✓

3. **6.3.1 Clock operation mode control register (CMC) (Page 312, Page 313)**

Incorrect:
(p.312)

(Omitted)

AMPH	Control of the X1 clock oscillation frequency
0	1 MHz ≦ fx ≦ 10 MHz
1	10 MHz ＜ fx ≦ 20 MHz

Note 1. The EXCLKS, OSCSELS, and AMPHS[1:0] bits are only initialized by a power-on reset; they retain the values when a reset caused by another source occurs.

Note 2. The gain and operating current of the XT1 clock oscillator decrease in the following order: low power consumption oscillation 1 > low power consumption oscillation 2 > low power consumption oscillation 3.

Correct:

(Omitted)

MODRV.AMPH1	AMPH	Control of the X1 clock oscillation frequency
0	0	Normal mode (1 MHz ≦ fx ≦ 10 MHz)
0	1	Normal mode (10 MHz ＜ fx ≦ 20 MHz)
1	1	Low driving mode (5 MHz ＜ fx ≦ 20 MHz)
1	0	Setting prohibited

Note 1. The EXCLKS, OSCSELS, and AMPHS[1:0] bits are only initialized by a power-on reset; they retain the values when a reset caused by another source occurs.

Note 2. The gain and operating current of the XT1 clock oscillator decrease in the following order: low power consumption oscillation 1 > low power consumption oscillation 2 > low power consumption oscillation 3.

(p.313)

Caution 1. The CMC register can be written only once by an 8-bit memory manipulation instruction after release from the reset state. Even if you intend to use the CMC register with its initial value (00H), be sure to write 00H to the register after release from the reset state as a precaution against malfunctions (since returning the value to 00H after erroneously having written a value other than 00H to it is not possible).

Caution 2. After release from the reset state, set the CMC register before X1 or XT1 oscillation is started by setting the clock operation status control register (CSC).

Caution 3. Be sure to set the AMPH bit to 1 **if** the X1 clock oscillation frequency exceeds 10 MHz.

(Omitted)

Caution 1. The CMC register can be written only once by an 8-bit memory manipulation instruction after release from the reset state. Even if you intend to use the CMC register with its initial value (00H), be sure to write 00H to the register after release from the reset state as a precaution against malfunctions (since returning the value to 00H after erroneously having written a value other than 00H to it is not possible).

Caution 2. After release from the reset state, set the CMC register before X1 or XT1 oscillation is started by setting the clock operation status control register (CSC).

Caution 3. Be sure to set the AMPH bit to 1 when the normal operation mode is selected in the main oscillator oscillation mode select register (MODRV) while the X1 clock oscillation frequency exceeds 10 MHz.

(Omitted)

4. 6.3.2 Main oscillator oscillation mode select register (MODRV) (Page 314)

Incorrect:

(Omitted)

Caution 1. The MODRV register can be written only once by an 8-bit memory manipulation instruction after release from the reset state. Even if you intend to use the MODRV register with its initial value (00H), be sure to write 00H to the register after release from the reset state as a precaution against malfunctions (since returning the value to 00H after erroneously having written a value other than 00H to it is not possible).

Caution 2. After release from the reset state, set the MODRV register before X1 oscillation is started by setting the clock operation status control register (CSC).

Caution 3. Make the setting of the AMPH1 bit while f_{IH} is selected as f_{CLK} after release from the reset state (before f_{CLK} is switched to f_{MX} or f_{SUB}).

Correct:

(Omitted)

Caution 1. The MODRV register can be written only once by an 8-bit memory manipulation instruction after release from the reset state. Even if you intend to use the MODRV register with its initial value (00H), be sure to write 00H to the register after release from the reset state as a precaution against malfunctions (since returning the value to 00H after erroneously having written a value other than 00H to it is not possible).

Caution 2. After release from the reset state, set the MODRV register before X1 oscillation is started by setting the clock operation status control register (CSC).

Caution 3. Make the setting of the AMPH1 bit while f_{IH} is selected as f_{CLK} after release from the reset state (before f_{CLK} is switched to f_{MX} or f_{SUB}).

Caution 4. The AMPH1 bit is used in combination with the AMPH bit in the CMC register. For details, see Section 6.3.1, Clock Mode Control Register (CMC).

5. 35.2.4 CTSU control registers BL and BH (CTSUCRBL, CTSUCRBH) (Page 1533)

Incorrect:

(Omitted)

SSCNT[1:0]		SUCLK Spread Spectrum Control
0	0	**CTSUTRIM1.SUADJD[7:0] + 00H**
0	1	**CTSUTRIM1.SUADJD[7:0] + 20H**
1	0	**CTSUTRIM1.SUADJD[7:0] + 40H**
1	1	**CTSUTRIM1.SUADJD[7:0] + 60H**
The SSCNT[1:0] bits adjust the frequency of SUCLK specified in the CTSUTRIM1.SUADJD[7:0] bits.		

(Omitted)

Correct:

(Omitted)

SSCNT[1:0]		SUCLK Spread Spectrum Control
0	0	CTSUCRAH.SDPSEL = 0: CTSUTRIMx.SUADJD[7:0] + 00H
		CTSUCRAH.SDPSEL = 1: CTSUSUCLKx.SUADJx[7:0] + 00H
0	1	CTSUCRAH.SDPSEL = 0: CTSUTRIMx.SUADJD[7:0] + 10H
		CTSUCRAH.SDPSEL = 1: CTSUSUCLKx.SUADJx[7:0] + 20H
1	0	CTSUCRAH.SDPSEL = 0: CTSUTRIMx.SUADJD[7:0] + 20H
		CTSUCRAH.SDPSEL = 1: CTSUSUCLKx.SUADJx[7:0] + 40H
1	1	CTSUCRAH.SDPSEL = 0: CTSUTRIMx.SUADJD[7:0] + 30H
		CTSUCRAH.SDPSEL = 1: CTSUSUCLKx.SUADJx[7:0] + 60H
These bits adjust the frequency of SUCLK.		

(Omitted)

6. 35.4.2 TSCAP pin (Page 1566)

Incorrect:

35.4.2 TSCAP pin

A capacitor must be connected to the TSCAP pin to stabilize the internal voltage of the CTSU. Make sure the wiring between the TSCAP pin and the capacitor, and between the capacitor and GND, is as thick and as short as possible.

Before setting the CTSUCRAL.CSW bit to 1 (the external capacitance connection switch turned on), the capacitor connected to the TSCAP pin must output a low level from the port to which the TSCAP function is assigned and be fully discharged.

Correct:

35.4.2 TSCAP pin

A capacitor must be connected to the TSCAP pin to stabilize the internal voltage of the CTSU. Make sure the wiring between the TSCAP pin and the capacitor, and between the capacitor and GND, is as thick and as short as possible. Table 30 - 3 states the condition for the capacitor to be connected to the TSCAP pin.

Table 30 - 3 Condition for the Capacitor to be Connected to the TSCAP Pin

Item	Symbol	Condition
Capacitance of the smoothing capacitor to be externally connected to the TSCAP pin	C_{TSCAP}	10 nF ±10%Note

Note Use a multilayer ceramic capacitor with a stated capacitance of 10 nF and a capacitance tolerance no greater than ±10%. Select from among those with a capacitance change limited to ±15% in accord with the usage environment, such as X7R as specified by the EIA standard.

Before setting the CTSUCRAL.CSW bit to 1 (the external capacitance connection switch turned on), the capacitor connected to the TSCAP pin must output a low level from the port to which the TSCAP function is assigned and be fully discharged.

7. 42.3.2 Supply current characteristics (Page 1705, Page 1708 to Page 1710)

Incorrect:
(Page 1705)

1. 44- to 64-pin products with 256 to 512 Kbytes of flash ROM and 80- to 100-pin products

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (3/4)

Item	Symbols	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.61	2.24	mA
					V_{DD} = 1.8 V		0.60	2.23	
			HS (high-speed main) mode	f_{MX} = 20 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.21	1.19	mA
					V_{DD} = 1.8 V		0.14	1.10	
			LS (low-speed main) mode	f_{MX} = 20 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.20	1.17	mA
					V_{DD} = 1.8 V		0.14	1.10	
				f_{MX} = 20 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.51	1.56	mA
					V_{DD} = 1.8 V		0.49	1.54	
				f_{MX} = 10 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.15	0.65	mA
					V_{DD} = 1.8 V		0.12	0.61	
				f_{MX} = 10 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.30	0.84	mA
					V_{DD} = 1.8 V		0.29	0.82	
				f_{MX} = 8 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.13	0.54	mA
					V_{DD} = 1.8 V		0.10	0.50	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.26	0.70	mA
					V_{DD} = 1.8 V		0.25	0.68	

(Omitted)

Correct:

1. 44- to 64-pin products with 256 to 512 Kbytes of flash ROM and 80- to 100-pin products

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (3/4)

Item	Symbols	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.61	2.24	mA
					V_{DD} = 1.8 V		0.60	2.23	
			HS (high-speed main) mode	f_{MX} = 20 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.24	1.23	mA
					V_{DD} = 1.8 V		0.23	1.21	
			LS (low-speed main) mode	f_{MX} = 20 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.24	1.22	mA
					V_{DD} = 1.8 V		0.23	1.22	
				f_{MX} = 20 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.51	1.56	mA
					V_{DD} = 1.8 V		0.49	1.54	
				f_{MX} = 10 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.15	0.65	mA
					V_{DD} = 1.8 V		0.12	0.61	
				f_{MX} = 10 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.30	0.84	mA
					V_{DD} = 1.8 V		0.29	0.82	
				f_{MX} = 8 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.13	0.54	mA
					V_{DD} = 1.8 V		0.10	0.50	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.26	0.70	mA
					V_{DD} = 1.8 V		0.25	0.68	

(Omitted)

(p.1708)
In the next revision of the user's manual, the power supply current characteristics of the "44- to 64-pin products with 64 to 128 Kbytes of flash ROM" will be included.

(Page 1709)

2. Peripheral functions (common to all products)

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/3)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	I_{FIH} **Note 1**				345		μA
Middle-speed on-chip oscillator operating current	I_{FIM} **Note 1**				20		μA
Low-speed on-chip oscillator operating current	I_{FIL} **Note 1**				0.3		μA
RTC operating current	I_{RTC} **Notes 1, 2, 3**	f_{RTCCLK} = 32.768 kHz			0.005		μA
		f_{RTCCLK} = 128 Hz			0.002		μA
32-bit interval timer operating current	I_{IT} **Notes 1, 2, 4**				0.04		μA
8-bit interval timers operating current	I_{TMT} **Notes 1, 2, 5**	f_{SUB} = 32.768 kHz, f_{MAIN} stopped	8-bit counter mode × 2 ch operation		0.08		μA
			16-bit counter mode operation		0.06		μA
Timer RJ operating current	I_{TMRJ} **Note 6**	f_{SUB} = 32.768 kHz, f_{MAIN} stopped, per unit			0.14		μA
16-bit timers KB40, KB41, and KB42 operating current	I_{TMKB} **Note 7**	Standalone mode, timer output disabled, f_{HOCO} = 64 MHz, per unit			530		μA
LVD operating current	I_{LVD0} **Notes 1, 14**				0.02		μA
	I_{LVD1} **Notes 1, 14**				0.02		μA

2. Peripheral functions (common to all products)

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/3)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	I_{FIH} **Note 1**				345		μA
Middle-speed on-chip oscillator operating current	I_{FIM} **Note 1**				20		μA
Low-speed on-chip oscillator operating current	I_{FIL} **Note 1**				0.3		μA
RTC operating current	I_{RTC} **Notes 1, 2, 3**	f_{RTCCLK} = 32.768 kHz			0.005		μA
		f_{RTCCLK} = 128 Hz			0.002		μA
32-bit interval timer operating current	I_{IT} **Notes 1, 2, 4**				0.04		μA
8-bit interval timers operating current	I_{TMT} **Notes 1, 2, 5**	f_{SUB} = 32.768 kHz, f_{MAIN} stopped	8-bit counter mode × 2 ch operation		0.08		μA
			16-bit counter mode operation		0.06		μA
Timer RJ operating current	I_{TMRJ} **Note 6**	f_{SUB} = 32.768 kHz, f_{MAIN} stopped, per unit			0.14		μA
16-bit timers KB40, KB41, and KB42 operating current	I_{TMKB} **Note 7**	Standalone mode, timer output disabled, f_{HOCO} = 64 MHz	44- to 64-pin products with 64 to 128 Kbytes of code flash memory, per unit		235		μA
			44- to 64-pin products with 256 to 512 Kbytes of code flash memory and 80- to 100-pin products, per 3 units		530		μA
LVD operating current	I_{LVD0} **Notes 1, 14**				0.02		μA
	I_{LVD1} **Notes 1, 14**				0.02		μA

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(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/3)

Item	Symbols	Conditions			Min.	Typ.	Max.	Unit
Self-programming operating current	I_{FSP} Notes 1, 15					2.5	12.2	mA
Data flash rewrite operating current	I_{BGO} Notes 1, 16					2.5	12.2	mA
SNOOZE mode sequencer operating current	I_{SMS} Notes 1, 17	f_{IH} = 32 MHz	44- to 64-pin products with 256 to 512 Kbytes of flash ROM and 80- and 100-pin products			1.5		mA
		f_{IL} = 32.768 kHz	44- to 64-pin products with 256 to 512 Kbytes of flash ROM and 80- and 100-pin products			1.6		μA
SNOOZE operating current	I_{SNOZ} Note 1	f_{IH} = 32 MHz	ADC is in use	The ADC is shifting from the STOP mode to the SNOOZE mode. Note 18		0.6	0.81	mA
				The ADC is operating in the low-voltage mode. AV_{REFP} = V_{DD} = 3.0 V		1.2	1.56	mA
			Simplified SPI (CSI)/UART is in use			0.7	0.92	mA
			SMS Note 19	44- to 64-pin products with 256 to 512 Kbytes of flash ROM and 80- and 100-pin products		2.0		mA
Low-speed peripheral clock supply current	I_{SXP} Notes 1, 20	RTCLPC = 0				0.22		μA
Output current control operating current	I_{CCDA} Notes 1, 21	The setting of the CCDE register is not 00H.				100		μA
	I_{CCDP} Notes 22, 23	Per single controlled current drive port pin	Setting of the low-level output current: Hi-Z			30		μA
			Setting of the low-level output current: 2 to 15 mA			200		μA
Operating current of the true random number generator	I_{TRNG} Note 1					1.1		mA

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/3)

Item	Symbols	Conditions			Min.	Typ.	Max.	Unit
Self-programming operating current	I_{FSP} Notes 1, 15					2.5	12.2	mA
Data flash rewrite operating current	I_{BGO} Notes 1, 16					2.5	12.2	mA
SNOOZE mode sequencer operating current	I_{SMS} Notes 1, 17	f_{IH} = 32 MHz	44- to 64-pin products with 64 to 128 Kbytes of code flash memory			1.1		mA
			44- to 64-pin products with 256 to 512 Kbytes of code flash memory and 80- to 100-pin products			1.5		mA
		f_{IL} = 32.768 kHz	44- to 64-pin products with 64 to 128 Kbytes of code flash memory			1.2		μA
			44- to 64-pin products with 256 to 512 Kbytes of code flash memory and 80- to 100-pin products			1.6		μA
SNOOZE operating current	I_{SNOZ} Note 1	f_{IH} = 32 MHz	ADC is in use	The ADC is shifting from the STOP mode to the SNOOZE mode. Note 18		0.6	0.81	mA
				The ADC is operating in the low-voltage mode. AV_{REFP} = V_{DD} = 3.0 V		1.2	1.56	mA
			Simplified SPI (CSI)/UART is in use			0.7	0.92	mA
			SMS Note 19	44- to 64-pin products with 64 to 128 Kbytes of code flash memory		1.6		mA
				44- to 64-pin products with 256 to 512 Kbytes of code flash memory and 80- to 100-pin		2.0		mA
Low-speed peripheral clock supply current	I_{SXP} Notes 1, 20	RTCLPC = 0				0.22		μA
Output current control operating current	I_{CCDA} Notes 1, 21	The setting of the CCDE register is not 00H.				100		μA
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			Setting of the low-level output current: 2 to 15 mA			200		μA
Operating current of the true random number generator	I_{TRNG} Note 1					1.1		mA