Date : Jun. 4, 2025

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0144A/E	Rev.	1.00
Title	DDR Memory Controller issue		Information Category	Technical Notification		
Applicable Product	RZ/V2N Group	Lot No.	Reference Document	RZ/V2N Group User's Manual: Hardware Rev.1.10		
		All lots				

This document describes an issue with the DDR Memory Controller.

1. Target product

Group	Name	Part Number	GE3D	Security	ISP
RZ/V2N	RZ/V2N	R9A09G056N41GBG#AC0	N/A	N/A	N/A
		R9A09G056N41GBG#BC0			
		R9A09G056N42GBG#AC0	Available (Mali-G31)		
		R9A09G056N42GBG#BC0			
		R9A09G056N45GBG#AC0	N/A	Available	
		R9A09G056N45GBG#BC0			
		R9A09G056N46GBG#AC0	Available (Mali-G31)		
		R9A09G056N46GBG#BC0			
	RZ/V2NP	R9A09G056N43GBG#AC0	N/A	N/A	Available (Mali-C55)
		R9A09G056N43GBG#BC0			
		R9A09G056N44GBG#AC0	Available (Mali-G31)		
		R9A09G056N44GBG#BC0			
		R9A09G056N47GBG#AC0	N/A	Available	
		R9A09G056N47GBG#BC0			
		R9A09G056N48GBG#AC0	Available (Mali-G31)		
		R9A09G056N48GBG#BC0			

2. Issue

In rare cases, abnormal read data may be returned when the following bus masters access DDR memory.

Target bus master

• Port 1: MIPI DSI

Note. This issue does not affect Port 1 (VCD, LCDC, ISU).

3. Limitation

Setting the following restrictions for the products with #AC0 or #BC0 in the part number

・Not supported controlling MIPI LCDs with the Display Command Set over MIPI-DSI.

4. User's manual Update

Please see the next page.

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5. Revision plan

   To address this issue, we will revise the target product.

   Mass production of the revised version is scheduled to begin in December 2025, and the current version will be replaced

   by the revised one with PCN.

User's Manual
1.1 Overview
1.1.2 Product Lineup

[From]

1.1.2 Product Lineup

Table 1.1-1   Product Lineup

Group	Name	Part Number	GE3D	Security	ISP
RZ/V2N	RZ/V2N	R9A09G056N41GBG	N/A	N/A	N/A
		R9A09G056N42GBG	Available (Mali-G31)		
		R9A09G056N45GBG	N/A	Available	
		R9A09G056N46GBG	Available (Mali-G31)		
	RZ/V2NP	R9A09G056N43GBG	N/A	N/A	Available (Mali-C55)
		R9A09G056N44GBG	Available (Mali-G31)		
		R9A09G056N47GBG	N/A	Available	
		R9A09G056N48GBG	Available (Mali-G31)		

Note: "#ACx" or "#BCx" is added to the end of part numbers. "#ACx" is packaged in the individual tray, and "#BCx" is packaged in the full carton.

[To]

1.1.2 Product Lineup

Table 1.1-1   Product Lineup

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		R9A09G056N46GBG	Available (Mali-G31)		
	RZ/V2NP	R9A09G056N43GBG	N/A	N/A	Available (Mali-C55)
		R9A09G056N44GBG	Available (Mali-G31)		
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Note: "#ACx" or "#BCx" is added to the end of part numbers. "#ACx" is packaged in the individual tray, and "#BCx" is packaged in the full carton.

Note : The products with #AC0 or #BC0 in the part number have the following restrictions.

・Not supported controlling MIPI LCDs with the Display Command Set over MIPI-DSI.

User's Manual
1.1 Overview
1.1.3 Functions

[From]

Table 1.1-7   Various Communication/Storage/Network Interfaces (1/3)

Item	Description
USB3.2 Host (USB3)	• 1 channel • Compliant with USB3.2 Gen2 × 1 • Maximum rate: 10 Gbps • Support for control, bulk, interrupt, and isochronous transfer • Internal dedicated DMA

Item	Description
MIPI DSI Interface with LCD controller (LCDC)	• 1 channel • Number of lanes: 1, 2, or 4 lanes • Support for the throughput up to 1920 × 1200 RGB888 60 fps • Support for the throughput up to 1280 × 1024 RGB888 120 fps • Maximum bandwidth: 1.5 Gbps per lane • Support for 2-plane blending (with the ability to blend 2 differently sized images) • Support for image processing: – Dither processing (RGB666) – Clipping – RGB gamma correction LUT • Support for input data formats: – RGB565, RGB666, RGB888 – ARGB1555, ARGB4444, ARGB8888 – YUV (YcbCr) 444 8-bits, YUV (YcbCr) 422 8-bits, YUV (YcbCr) 420 8-bits • Support for output data formats: – RGB666, RGB888

[To]

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MIPI DSI Interface with LCD controller (LCDC) *1	• 1 channel • Number of lanes: 1, 2, or 4 lanes • Support for the throughput up to 1920 × 1200 RGB888 60 fps • Support for the throughput up to 1280 × 1024 RGB888 120 fps • Maximum bandwidth: 1.5 Gbps per lane • Support for 2-plane blending (with the ability to blend 2 differently sized images) • Support for image processing: – Dither processing (RGB666) – Clipping – RGB gamma correction LUT • Support for input data formats: – RGB565, RGB666, RGB888 – ARGB1555, ARGB4444, ARGB8888 – YUV (YcbCr) 444 8-bits, YUV (YcbCr) 422 8-bits, YUV (YcbCr) 420 8-bits • Support for output data formats: – RGB666, RGB888

Note1 : The products with #AC0 or #BC0 in the part number have the following restrictions.

・Not supported controlling MIPI LCDs with the Display Command Set over MIPI-DSI.