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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0150A/E	Rev.	1.00
Title	Error Correction Notification Changes to Descriptions in the RL78/G16 User's Manual Rev.1.30		Information Category	Technical Notification		
Applicable Product	RL78/G16 Group	Lot No. All	Reference Document	RL78/G16 User's Manual: Hardware Rev. 1.30 R01UH0980EJ0130 (May 2025)		

Errors in the RL78/G16 User's Manual: Hardware Rev.1.30 (R01UH0980EJ0130) are to be corrected as follows.

Corrections Stated in This Notification

Section to be Corrected	Page	Content
1.5.1 10-pin products	Page.41	Incorrect descriptions revised
Figure 2-6. Pin Block Diagram for Pin Type 7-31-5	Page 68	Incorrect descriptions revised
Table 3-6. Extended SFR (2nd SFR) List (1/6)	Page 100	Incorrect descriptions revised
4.3.7 Touch pin function select registers 0, 1 (TSSEL0, TSSEL1)	Page 149	Incorrect descriptions revised
4.3.8 TSCAP pin setting register (VTSEL)	Page 150	Incorrect descriptions revised
Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (3/14)	Page 156	Incorrect descriptions revised
4.5.3 Register setting examples for used port and alternate functions	Page 166	Incorrect descriptions revised
15.3.2 CTSU control register 0 (CTSUCR0)	Page 704, Page705	Incorrect descriptions revised
15.3.20 Touch pin function select registers 0, 1 (TSSEL0, TSSEL1)	Page 733	Incorrect descriptions revised
15.3.21 TSCAP pin setting register (VTSEL)	Page 734	Incorrect descriptions revised
15.4.2 Measurement modes	Page 743, Page 746 Page 750	Incorrect descriptions revised
15.4.3 Items common to multiple modes	Page 756, Page 757	Incorrect descriptions revised
26.6.4 SPOR circuit characteristics	Page 914	Incorrect descriptions revised
27.6.4 SPOR circuit characteristics	Page 939	Incorrect descriptions revised

Document Improvement

The corrections stated in this notification will be made at the time of the next revision of the user's manual.

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List of Corrections in the User's Manual

No	Content to be Corrected and Location			Page in This Notification
	Document No.	English	R01UH0980EJ0130	
1	1.5.1 10-pin products		Page.41	Page 3
2	Figure 2-6. Pin Block Diagram for Pin Type 7-31-5		Page 68	Page 4
3	Table 3-6. Extended SFR (2nd SFR) List (1/6)		Page 100	Page 5
4	4.3.7 Touch pin function select registers 0, 1 (TSSEL0, TSSEL1)		Page 149	Page 6
5	4.3.8 TSCAP pin setting register (VTSEL)		Page 150	Page 7
6	Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (3/14)		Page 156	Page 8
7	4.5.3 Register setting examples for used port and alternate functions		Page 166	Page 9
8	15.3.2 CTSU control register 0 (CTSUCR0)		Page 704, Page 705	Page 10, Page.12
9	15.3.20 Touch pin function select registers 0, 1 (TSSEL0, TSSEL1)		Page 733	Page 13
10	15.3.21 TSCAP pin setting register (VTSEL) Page 734		Page 734	Page 14
11	15.4.2 Measurement modes		Page 743, Page 746, Page 750	Page 15 to Page 17
12	15.4.3 Items common to multiple modes		Page 756, Page 757	Page 18 to Page 21
13	26.6.4 SPOR circuit characteristics		Page 914	Page 22
14	27.6.4 SPOR circuit characteristics		Page 939	Page 23

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G16 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0150A/E	Oct. 30, 2025	First edition issued Correction No.1 to No.14 revised (this document)

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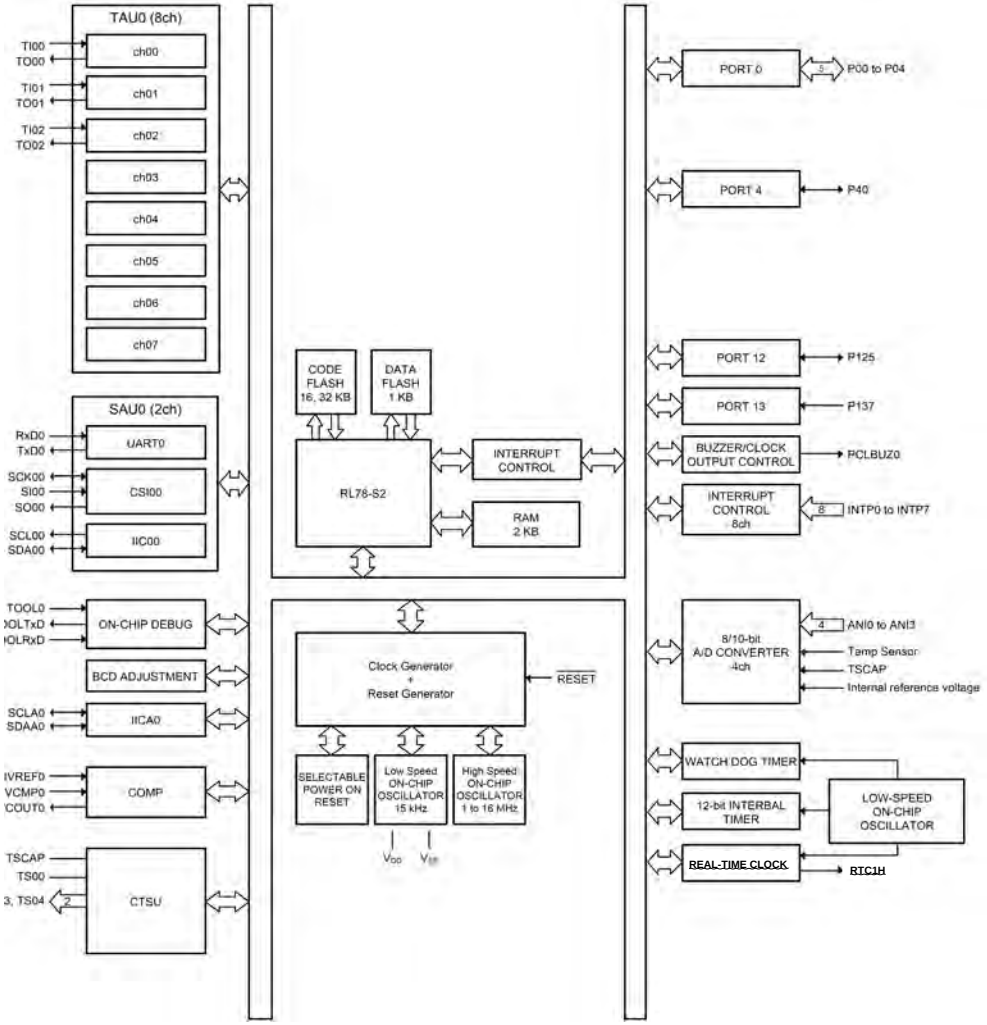
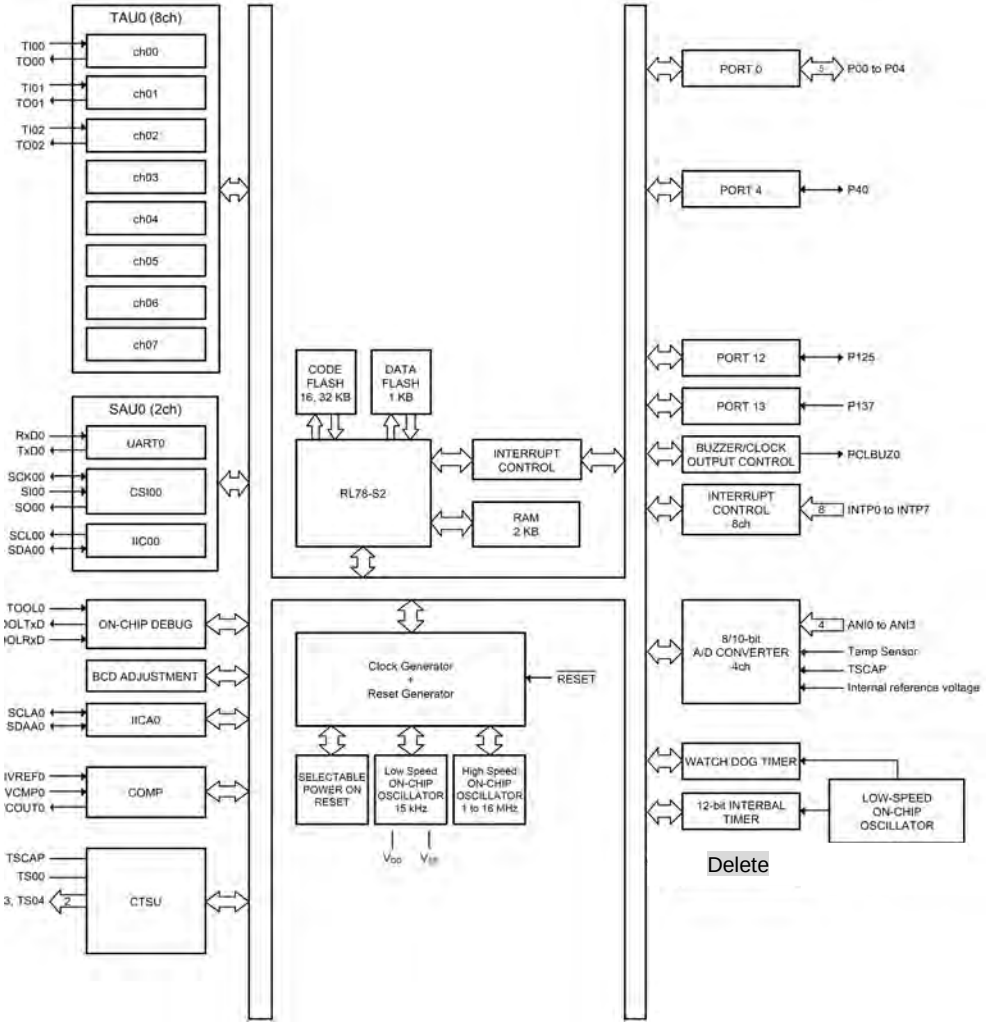
1. 1.5.1 10-pin products (Page 41)

Incorrect:



Correct:



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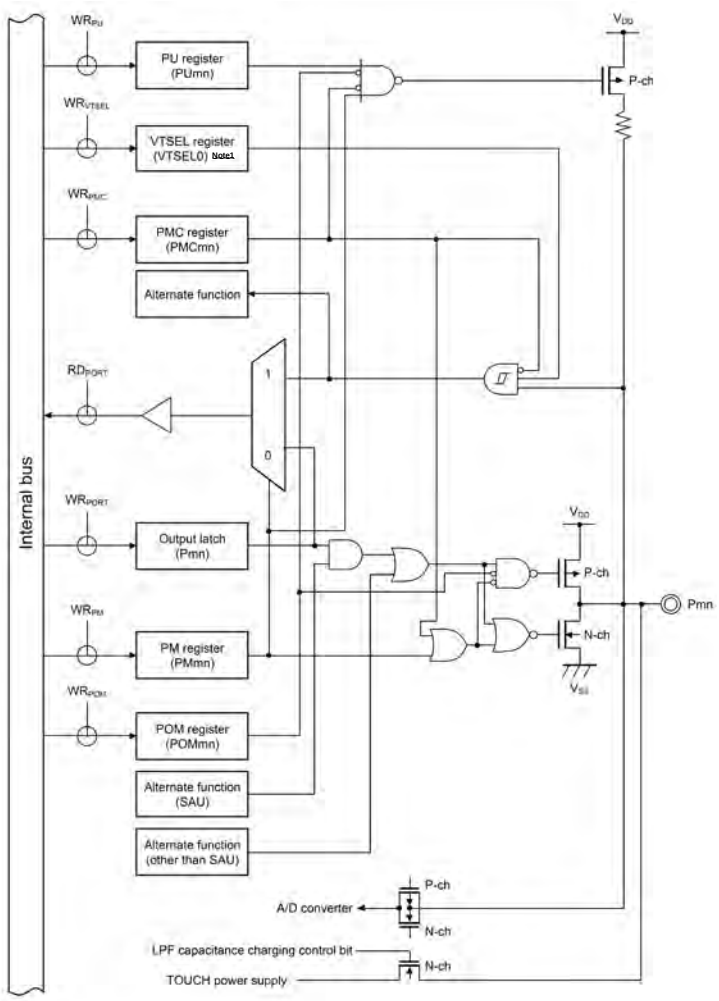
2. **Figure 2-6. Pin Block Diagram for Pin Type 7-31-5 (Page 68)**

Incorrect:

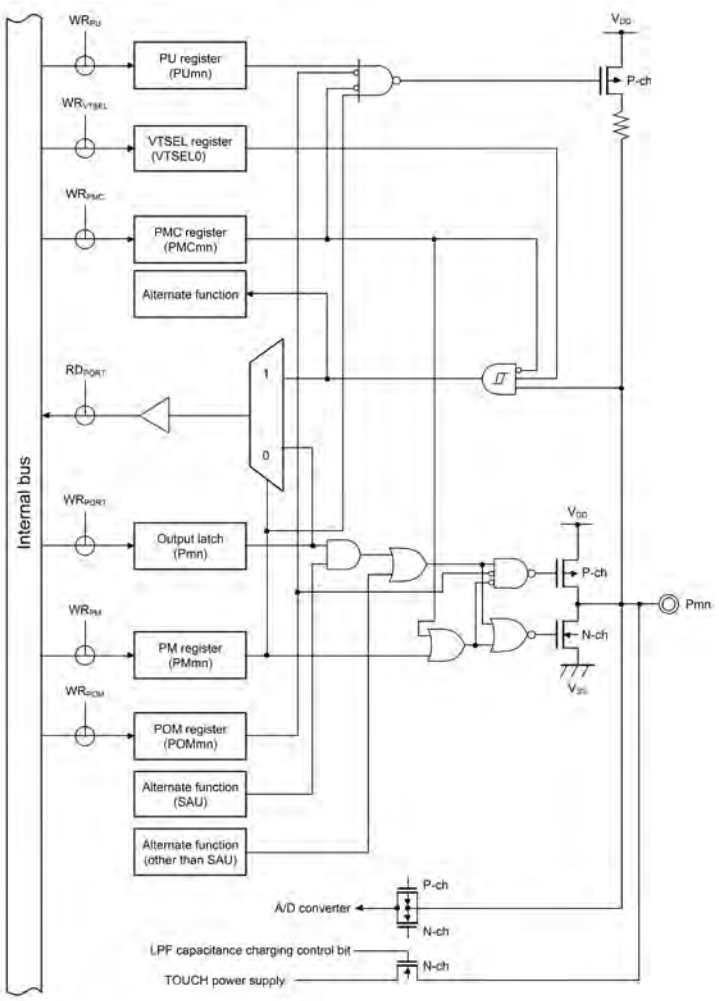


Note 1. The function of the VTSEL register in the figure of I/O circuit 7-31-5 is only enabled when any of the bits in the TSSELn (n = 0 to 2) registers is set to 1.

Remark 1. For alternate functions, see 2.1 Port Function.

Remark 2. SAU: Serial array unit

Correct:



Remark 1. For alternate functions, see 2.1 Port Function.

Remark 2. SAU: Serial array unit

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3. **Table 3-6. Extended SFR (2nd SFR) List (1/6) (Page 100)**

Incorrect:

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F0010H	A/D converter mode register 2	ADM2	R/W	✓	✓	—	00H
F0013H	A/D test register	ADTES	R/W	—	✓	—	00H
F0030H	Pull-up resistor option register 0	PU0	R/W	✓	✓	—	00H
F0031H	Pull-up resistor option register 1	PU1	R/W	✓	✓	—	00H
F0032H	Pull-up resistor option register 2	PU2	R/W	✓	✓	—	00H
F0034H	Pull-up resistor option register 4	PU4	R/W	✓	✓	—	01H
F003CH	Pull-up resistor option register 12	PU12	R/W	✓	✓	—	00H
~~F004EH~~	~~Port input mode register 14~~	~~PIM14~~	~~R/W~~	~~✓~~	~~✓~~	~~—~~	~~00H~~
F0050H	Port output mode register 0	POM0	R/W	✓	✓	—	00H
F0051H	Port output mode register 1	POM1	R/W	✓	✓	—	00H
F0052H	Port output mode register 2	POM2	R/W	✓	✓	—	00H
F0054H	Port output mode register 4	POM4	R/W	✓	✓	—	00H
F0060H	Port mode control register 0	PMC0	R/W	✓	✓	—	FFH
F0062H	Port mode control register 2	PMC2	R/W	✓	✓	—	FFH
F0070H	Noise filter enable register 0	NFEN0	R/W	✓	✓	—	00H
F0071H	Noise filter enable register 1	NFEN1	R/W	✓	✓	—	00H
F0073H	Input switch control register	ISC	R/W	✓	✓	—	00H
F0074H	Timer input select register 0	TIS0	R/W	—	✓	—	00H
F0075H	Peripheral I/O redirection register 2	PIOR2	R/W	—	✓	—	00H
F0076H	Peripheral I/O redirection register 6	PIOR6	R/W	—	✓	—	00H
F0077H	Peripheral I/O redirection register 0	PIOR0	R/W	—	✓	—	00H
F0078H	Illegal memory access detection control register	IAWCTL	R/W	—	✓	—	00H
F0079H	Peripheral I/O redirection register 1	PIOR1	R/W	—	✓	—	00H
F007AH	Peripheral enable register 1	PER1	R/W	✓	✓	—	00H
F007BH	Peripheral I/O redirection register 4	PIOR4	R/W	—	✓	—	00H
F007CH	Peripheral I/O redirection register 3	PIOR3	R/W	—	✓	—	00H
F007DH	Peripheral I/O redirection register 5	PIOR5	R/W	—	✓	—	00H
F00A0H	High-speed on-chip oscillator trimming register	HIOTRM	R/W	—	✓	—	Undefined Note 1
F00A8H	High-speed on-chip oscillator frequency select register	HOCODIV	R/W	—	✓	—	Undefined Note 2
F00BEH	Flash sequencer frequency setting register	FSSET	R/W	—	✓	—	00H
F00C0H	Flash programming mode control register	FLPMC	R/W	—	✓	—	08H
F00C1H	Flash sequencer control register	FSSQ	R/W	—	✓	—	00H
F00C2H	Flash address pointer L	FLAPL	R/W	—	✓	—	00H
F00C3H	Flash address pointer H	FLAPH	R/W	—	✓	—	00H
F00C4H	Flash end address pointer L	FLSEDL	R/W	—	✓	—	00H
F00C5H	Flash end address pointer H	FLSEDH	R/W	—	✓	—	00H
F00C6H	Flash sequencer status register L	FSASTL	R	—	✓	—	00H
F00C7H	Flash sequence status register H	FSASTH	R	—	✓	—	00H

Correct:

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F0010H	A/D converter mode register 2	ADM2	R/W	✓	✓	—	00H
F0013H	A/D test register	ADTES	R/W	—	✓	—	00H
F0030H	Pull-up resistor option register 0	PU0	R/W	✓	✓	—	00H
F0031H	Pull-up resistor option register 1	PU1	R/W	✓	✓	—	00H
F0032H	Pull-up resistor option register 2	PU2	R/W	✓	✓	—	00H
F0034H	Pull-up resistor option register 4	PU4	R/W	✓	✓	—	01H
F003CH	Pull-up resistor option register 12	PU12	R/W	✓	✓	—	00H
	Delete						
F0050H	Port output mode register 0	POM0	R/W	✓	✓	—	00H
F0051H	Port output mode register 1	POM1	R/W	✓	✓	—	00H
F0052H	Port output mode register 2	POM2	R/W	✓	✓	—	00H
F0054H	Port output mode register 4	POM4	R/W	✓	✓	—	00H
F0060H	Port mode control register 0	PMC0	R/W	✓	✓	—	FFH
F0062H	Port mode control register 2	PMC2	R/W	✓	✓	—	FFH
F0070H	Noise filter enable register 0	NFEN0	R/W	✓	✓	—	00H
F0071H	Noise filter enable register 1	NFEN1	R/W	✓	✓	—	00H
F0073H	Input switch control register	ISC	R/W	✓	✓	—	00H
F0074H	Timer input select register 0	TIS0	R/W	—	✓	—	00H
F0075H	Peripheral I/O redirection register 2	PIOR2	R/W	—	✓	—	00H
F0076H	Peripheral I/O redirection register 6	PIOR6	R/W	—	✓	—	00H
F0077H	Peripheral I/O redirection register 0	PIOR0	R/W	—	✓	—	00H
F0078H	Illegal memory access detection control register	IAWCTL	R/W	—	✓	—	00H
F0079H	Peripheral I/O redirection register 1	PIOR1	R/W	—	✓	—	00H
F007AH	Peripheral enable register 1	PER1	R/W	✓	✓	—	00H
F007BH	Peripheral I/O redirection register 4	PIOR4	R/W	—	✓	—	00H
F007CH	Peripheral I/O redirection register 3	PIOR3	R/W	—	✓	—	00H
F007DH	Peripheral I/O redirection register 5	PIOR5	R/W	—	✓	—	00H
F00A0H	High-speed on-chip oscillator trimming register	HIOTRM	R/W	—	✓	—	Undefined Note 1
F00A8H	High-speed on-chip oscillator frequency select register	HOCODIV	R/W	—	✓	—	Undefined Note 2
F00BEH	Flash sequencer frequency setting register	FSSET	R/W	—	✓	—	00H
F00C0H	Flash programming mode control register	FLPMC	R/W	—	✓	—	08H
F00C1H	Flash sequencer control register	FSSQ	R/W	—	✓	—	00H
F00C2H	Flash address pointer L	FLAPL	R/W	—	✓	—	00H
F00C3H	Flash address pointer H	FLAPH	R/W	—	✓	—	00H
F00C4H	Flash end address pointer L	FLSEDL	R/W	—	✓	—	00H
F00C5H	Flash end address pointer H	FLSEDH	R/W	—	✓	—	00H
F00C6H	Flash sequencer status register L	FSASTL	R	—	✓	—	00H
F00C7H	Flash sequence status register H	FSASTH	R	—	✓	—	00H

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4. 4.3.7 Touch pin function select registers 0, 1 (TSSEL0, TSSEL1) (Page 149)

Incorrect:

These registers select whether the touch pin function or another multiplexed function is used with the P01, P03 to P07,P16, P17, P20 to P23, and P41 to P43 pins.
These registers can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation clears these registers to 00H.

Figure 4-7. Format of Touch Pin Function Select Registers 0, 1 (TSSEL0, TSSEL1)

Address: F030AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TSSEL0	TSSEL07	TSSEL06	TSSEL05	TSSEL04	TSSEL03	TSSEL02	TSSEL01	TSSEL00

Address: F030BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TSSEL1	0	TSSEL14	TSSEL13	TSSEL12	TSSEL11	TSSEL10	TSSEL09	TSSEL08

TSSELxx **(xx = 0 to 14)**	Selection of a function other than the touch pin function (multiplexed function) or the touch pin function for the Pmn pin **(m = 0, 1, 2, 4; n = 0 to 7)**
0	Use the Pmn pin for a function other than the touch pin function (multiplexed function).
1	Use the Pmn pin for the touch pin function.

Remark To use the Pmn pins as touch pins (TSSELxx = 1), be sure to set the PUmn bit of the PUm register, POMmn bit of the POMm register**, and PIMmn bit of the PIMm register** to “0”.

- 10-pin products: Only TSSEL00, 03, and 04 are valid.
- 16-pin products: Only TSSEL00, 03, 04, 05, 06, 07, and 13 are valid.
- 20- and 24-pin products: TSSEL00, 03, 04, 05, 06, 07, 08, 09, 10, 11, and 13 are valid.

Correct:

These registers select whether the touch pin function or another multiplexed function is used with the P01, P03 to P07,P16, P17, P20 to P23, and P41 to P43 pins.
These registers can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation clears these registers to 00H.

Figure 4-7. Format of Touch Pin Function Select Registers 0, 1 (TSSEL0, TSSEL1)

Address: F030AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TSSEL0	TSSEL07	TSSEL06	TSSEL05	TSSEL04	TSSEL03	TSSEL02	TSSEL01	TSSEL00

Address: F030BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TSSEL1	0	TSSEL14	TSSEL13	TSSEL12	TSSEL11	TSSEL10	TSSEL09	TSSEL08

TSSELxx	Selection of a function other than the touch pin function (multiplexed function) or the touch pin function for the Pmn pin.
0	Use the Pmn pin for a function other than the touch pin function (multiplexed function).
1	Use the Pmn pin for the touch pin function.

TSSELxx	Pmn/TSxx
TSSEL00	P01/TS00
TSSEL01	P16/TS01
TSSEL02	P17/TS02
TSSEL03	P03/TS03
TSSEL04	P04/TS04

TSSELxx	Pmn/TSxx
TSSEL05	P05/TS05
TSSEL06	P06/TS06
TSSEL07	P07/TS07
TSSEL08	P23/TS08
TSSEL09	P22/TS09

TSSELxx	Pmn/TSxx
TSSEL10	P21/TS10
TSSEL11	P20/TS11
TSSEL12	P42/TS12
TSSEL13	P41/TS13
TSSEL14	P43/TS14

Remark To use the Pmn pins as touch pins (TSSELxx = 1), be sure to set the PUmn bit of the PUm register, POMmn bit of the POMm register to “0”.

- 10-pin products: Only TSSEL00, 03, and 04 are valid.
- 16-pin products: Only TSSEL00, 03, 04, 05, 06, 07, and 13 are valid.
- 20- and 24-pin products: TSSEL00, 03, 04, 05, 06, 07, 08, 09, 10, 11, and 13 are valid.

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5. 4.3.8 TSCAP pin setting register (VTSEL) (Page 150)

Incorrect:

When the touch pin function is in use (when the TSSELxx bit is set to 1), the setting of the VTSEL register is effective.This register disables or enables input to the P02 pin.
The VTSEL register can be set by an 8-bit memory manipulation instruction.
Reset signal generation clears this register to 00H.

Figure 4-8. Format of TSCAP Pin Setting Register (VTSEL)

32-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
VTSEL	0	0	0	0	0	0	0	VTSEL0	F030DH	00H	R/W

VTSEL0	Disabling or enabling of input to the P02 pin
0	When the touch pin function is in use, input to the P02 pin is disabled.
1	**When the touch pin function is in use**, input to the P02 pin is enabled.

Correct:

When the touch pin function is in use (when the TSSELxx bit is set to 1), the setting of the VTSEL register is effective.This register disables or enables input to the P02 pin.
The VTSEL register can be set by an 8-bit memory manipulation instruction.
Reset signal generation clears this register to 00H.

Figure 4-8. Format of TSCAP Pin Setting Register (VTSEL)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
VTSEL	0	0	0	0	0	0	0	VTSEL0	F030DH	00H	R/W

VTSEL0	Disabling or enabling of input to the P02 pin
0	When the touch pin function is in use, input to the P02 pin is disabled.
1	When the digital I/O port function is in use, input to the P02 pin is enabled.

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6. Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (3/14) (Page 156)

Incorrect:

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	~~TSSELt~~	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	Function Name	I/O							SAU Output Function	Other than SAU					
P02	P02	Input	—	—	0	1	×	~~×~~	×	×	✓	✓	✓	✓	✓
		Output	—	—	0	0	0/1	~~×~~	SCK00/SCL00 = 1 (SCK20/SCL20) = 1 Note 4 (SO11) = 1 Note 1	PCLBUZ0 = 0 VCOUT0 = 0 TO01 = 0 (TO02) = 0 Note 1					
	ANI1	Analog input	—	—	1	1	×	~~×~~	×	×	✓	✓	✓	✓	✓
	TSCAP Note 7	—	—	—	×	1	×	~~×~~	×	×	✓	✓	✓	✓	✓
	SCK00	Input	PIOR21 = 0 PIOR20 = 0	—	0	1	×	~~×~~	×	×	✓	✓	✓	✓	✓
		Output		—	0	0	1	~~×~~	(SCK20/SCL20) = 1 Note 4 (SO11) = 1 Note 1	PCLBUZ0 = 0 VCOUT0 = 0 TO01 = 0 (TO02) = 0 Note 1					
	SCL00	Output		—	0	0	1	~~×~~			✓	✓	✓	✓	✓
	(SCK20)	Input	PIOR26 = 0 PIOR25 = 1	—	0	1	×	~~×~~	×	×	✓	—	—	—	—
		Output		—	0	0	1	~~×~~	SCK00/SCL00 = 1 (SO11) = 1 Note 1	PCLBUZ0 = 0 VCOUT0 = 0 TO01 = 0 (TO02) = 0 Note 1					
	(SCL20)	Output		—	0	0	1	~~×~~			✓	—	—	—	—
	PCLBUZ0	Output	PIOR62 = 0 PIOR61 = 0 PIOR60 = 0	—	0	0	0	~~×~~	×	VCOUT0 = 0 TO01 = 0 (TO02) = 0 Note 1	✓	✓	✓	✓	✓
	VCOUT0	Output	PIOR65 = 0 PIOR64 = 0 PIOR63 = 0	—	0	0	0	~~×~~	×	PCLBUZ0 = 0 TO01 = 0 (TO02) = 0 Note 1	✓	✓	✓	✓	✓
	INTP7	Input	PIOR55 = 0 PIOR54 = 0	—	0	1	×	~~×~~	×	×	✓	✓	✓	✓	✓
	(TI02)	Input	PIOR06 = 0 PIOR05 = 1 PIOR04 = 0	—	0	1	×	~~×~~	×	×	✓	✓	✓	✓	—
	(TO02)	Output		—	0	0	0	~~×~~	×	PCLBUZ0 = 0 VCOUT0 = 0 TO01 = 0	✓	✓	✓	✓	—
	TI01	Input	PIOR03 = 0 PIOR02 = 0	—	0	1	×	~~×~~	×	×	✓	✓	✓	✓	✓
	TO01	Output		—	0	0	0	~~×~~	×	PCLBUZ0 = 0 VCOUT0 = 0 (TO02) = 0 Note 1	✓	✓	✓	✓	✓
	(SO11)	Output	PIOR24 = 0 PIOR23 = 0 PIOR22 = 1	—	0	0	1	~~×~~	SCK00/SCL00 = 1 (SCK20/SCL20) = 1 Note 4	PCLBUZ0 = 0 VCOUT0 = 0 TO01 = 0 (TO02) = 0 Note 1	✓	✓	✓	✓	—

Correct:

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	VTSEL	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	Function Name	I/O							SAU Output Function	Other than SAU					
P02	P02	Input	—	—	0	1	×	1	×	×	✓	✓	✓	✓	✓
		Output	—	—	0	0	0/1	×	SCK00/SCL00 = 1 (SCK20/SCL20) = 1 Note 4 (SO11) = 1 Note 1	PCLBUZ0 = 0 VCOUT0 = 0 TO01 = 0 (TO02) = 0 Note 1					
	ANI1	Analog input	—	—	1	1	×	×	×	×	✓	✓	✓	✓	✓
	TSCAP Note 7	—	—	—	×	1	×	0	×	×	✓	✓	✓	✓	✓
	SCK00	Input	PIOR21 = 0 PIOR20 = 0	—	0	1	×	1	×	×	✓	✓	✓	✓	✓
		Output		—	0	0	1	×	(SCK20/SCL20) = 1 Note 4 (SO11) = 1 Note 1	PCLBUZ0 = 0 VCOUT0 = 0 TO01 = 0 (TO02) = 0 Note 1					
	SCL00	Output		—	0	0	1	×			✓	✓	✓	✓	✓
	(SCK20)	Input	PIOR26 = 0 PIOR25 = 1	—	0	1	×	1	×	×	✓	—	—	—	—
		Output		—	0	0	1	×	SCK00/SCL00 = 1 (SO11) = 1 Note 1	PCLBUZ0 = 0 VCOUT0 = 0 TO01 = 0 (TO02) = 0 Note 1					
	(SCL20)	Output		—	0	0	1	×			✓	—	—	—	—
	PCLBUZ0	Output	PIOR62 = 0 PIOR61 = 0 PIOR60 = 0	—	0	0	0	×	×	VCOUT0 = 0 TO01 = 0 (TO02) = 0 Note 1	✓	✓	✓	✓	✓
	VCOUT0	Output	PIOR65 = 0 PIOR64 = 0 PIOR63 = 0	—	0	0	0	×	×	PCLBUZ0 = 0 TO01 = 0 (TO02) = 0 Note 1	✓	✓	✓	✓	✓
	INTP7	Input	PIOR55 = 0 PIOR54 = 0	—	0	1	×	1	×	×	✓	✓	✓	✓	✓
	(TI02)	Input	PIOR06 = 0 PIOR05 = 1 PIOR04 = 0	—	0	1	×	1	×	×	✓	✓	✓	✓	—
	(TO02)	Output		—	0	0	0	×	×	PCLBUZ0 = 0 VCOUT0 = 0 TO01 = 0	✓	✓	✓	✓	—
	TI01	Input	PIOR03 = 0 PIOR02 = 0	—	0	1	×	1	×	×	✓	✓	✓	✓	✓
	TO01	Output		—	0	0	0	×	×	PCLBUZ0 = 0 VCOUT0 = 0 (TO02) = 0 Note 1	✓	✓	✓	✓	✓
	(SO11)	Output	PIOR24 = 0 PIOR23 = 0 PIOR22 = 1	—	0	0	1	×	SCK00/SCL00 = 1 (SCK20/SCL20) = 1 Note 4	PCLBUZ0 = 0 VCOUT0 = 0 TO01 = 0 (TO02) = 0 Note 1	✓	✓	✓	✓	—

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7. 4.5.3 Register setting examples for used port and alternate functions (Page 166)

Incorrect:

[omitted]

Note 1. 16-pin to 32-pin products only.
Note 2. 20-pin to 32-pin products only.
Note 3. 24-pin to 32-pin products only.
Note 4. 32-pin products only.
Note 5. 10-pin products only.
Note 6. 16-pin to 20-pin products only.
Note 7. When the touch pin function is in use (when the TSSELxx bit is set to 1), the P02/TSCAP pin automatically functions as TSCAP.

Correct:

[omitted]

Note 1. 16-pin to 32-pin products only.
Note 2. 20-pin to 32-pin products only.
Note 3. 24-pin to 32-pin products only.
Note 4. 32-pin products only.
Note 5. 10-pin products only.
Note 6. 16-pin to 20-pin products only.

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8. 5.3.2 CTSU control register 0 (CTSUCR0) (Page 704, Page 705)

Incorrect:
(Page 704)

Figure 15-5. Format of CTSU Control Register 0 (CTSUCR0) (2/3)

[omitted]

(1) Suspended state
While the CTSU is in the wait state for an external trigger by setting the CTSUSTRT bit to 1 after selecting an external trigger (the CTSUCAP bit = 1) and enabling suspension (the CTSUSNZ bit = 1), the CPU can be placed in STOP mode.
When a rising edge of the external trigger is detected during STOP mode, the CTSU issues a clock request to the clock generating block and makes a transition to normal operating mode to start measurement

Correct:

Figure 15-5. Format of CTSU Control Register 0 (CTSUCR0) (2/3)

[omitted]

(1) Suspended state (waiting for an external trigger)
The CPU is placed in this state by setting the CTSUSTRT bit to 1 after selecting an external trigger (the CTSUCAP bit = 1) and enabling suspension (the CTSUSNZ bit = 1). In the suspended state, placing the CPU in STOP mode is possible.

When a rising edge of the external trigger signal is detected, the CTSU starts measurement.

To proceed with re-measurement after the end of measurement, make settings by following steps (a), (b), and (c) below after the measurement end interrupt.

(a) Write 0 to the CTSUSTRT bit and 1 to the CTSUINIT bit at the same time (for a forced stop).
(b) Set the CTSUSNZ bit to 0 (suspension disabled)
(c) Set the CTSUCAP and CTSUSNZ bits to 1, and set the CTSUSTRT bit to 1 (the suspended state (waiting for an external trigger)).

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(2) SW suspended state

The SW suspended state refers to the state of suspension initiated when the software trigger has been selected (the CTSUCA bit = 0) and suspension has been enabled (the CTSUSNZ = 1).

This state is used when placing the CTSU hard macro in the suspended state to decrease power consumption by software. In the SW suspended state, placing the CPU in STOP mode is also possible. For return from STOP state, an interrupt **is used.**

To start measurement from the SW suspended state, set the CTSUSNZ bit to 0 and then wait for at least 64 cycles of the base clock (e.g.: at least 128 µs when the base clock is at 0.5 MHz) before setting the CTSUSTRT bit to 1.

To resume the SW suspended state after the end of measurement, set the CTSUSNZ bit to 1.

(2) SW suspended state

The CPU is placed in this state by selecting the software trigger (the CTSUCAP bit = 0), enabling suspension (the CTSUSNZ bit = 1) and setting the CTSUSTRT bit to 0. In the SW suspended state, placing the CPU in STOP mode is possible. For return from STOP state, an interrupt signal is used.

To start measurement from the SW suspended state, set the CTSUSNZ bit to 0 and then wait for at least 64 cycles of the base clock (e.g.: at least 128 µs when the base clock is at 0.5 MHz) before setting the CTSUSTRT bit to 1.

To resume the SW suspended state after the end of measurement, set the CTSUSNZ bit to 1.

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(Page 705)

Figure 15-5. Format of CTSU Control Register 0 (CTSUCR0) (3/3)

[omitted]

Note 1. Do not write 1 to the CTSUINIT bit at the same time as setting the CTSUSTRT bit to 1 (CTSU operation starts).
Note 2. The CTSUSC, CTSUMCH0, CTSUMCH1, and CTSUST registers are initialized.
Note 3. The CTSUCAP and CTSUSNZ bits should be set while the CTSUSTRT bit is 0. These bits can be set at the same time as the CTSUSTRT bit is set to 1.
Note 4. When a trigger occurs during STOP mode, measurement is performed in normal measurement mode.
Note 5. The state can be read from the CTSUSTC[2:0] flags in the CTSUST register.
During measurement: CTSUSTC[2:0] flags in the CTSUST register ≠ 000B
Wait for an external trigger: CTSUSTC[2:0] flags in the CTSUST register = 000B

Figure 15-5. Format of CTSU Control Register 0 (CTSUCR0) (3/3)

[omitted]

Note 1. Do not write 1 to the CTSUINIT bit at the same time as setting the CTSUSTRT bit to 1 (CTSU measurement operation starts).
In the CTSUCR0 register, the only possible setting is writing 0 to the CTSUSTRT bit and 1 to the CTSUINIT bit at the same time (for a forced stop) while the CTSUSTRT bit is 1.
Note 2. The CTSUSC, CTSUMCH0, CTSUMCH1, and CTSUST registers are initialized.
Note 3. Set the CTSUCAP and CTSUSNZ bits while the CTSUSTRT bit is 0. These bits can be set at the same time as the CTSUSTRT bit is set to 1.
Note 4. When a trigger occurs during STOP mode, measurement is performed in normal measurement mode.
Note 5. The state can be read from the CTSUSTC[2:0] flags in the CTSUST register.
During measurement: CTSUSTC[2:0] flags in the CTSUST register ≠ 000B
Wait for an external trigger: CTSUSTC[2:0] flags in the CTSUST register = 000B

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9. 15.3.20 Touch pin function select registers 0, 1 (TSSEL0, TSSEL1) (Page 733)

Incorrect:

These registers select whether the touch pin function or another multiplexed function is used with the P01, P03 to P07, P16, P17, P20 to P23, and P41 to P43 pins.
These registers can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation clears these registers to 00H.

Figure 15-23. Format of Touch Pin Function Select Registers 0, 1 (TSSEL0, TSSEL1)

Address: F030AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TSSEL0	TSSEL07	TSSEL06	TSSEL05	TSSEL04	TSSEL03	TSSEL02	TSSEL01	TSSEL00

Address: F030BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TSSEL1	0	TSSEL14	TSSEL13	TSSEL12	TSSEL11	TSSEL10	TSSEL09	TSSEL08

TSSELxx **(xx = 0 to 14)**	Selection of a function other than the touch pin function (multiplexed function) or the touch pin function for the Pmn pin **(m = 0, 1, 2, 4; n = 0 to 7)**
0	Use the Pmn pin for a function other than the touch pin function (multiplexed function).
1	Use the Pmn pin for the touch pin function.

Remark To use the Pmn pins as touch pins (TSSELxx = 1), be sure to set the PUmn bit of the PUm register, POMmn bit of the POMm register, and **PIMmn bit of the PIMm register** to “0”.

- 10-pin products: Only TSSEL00, 03, and 04 are valid.
- 16-pin products: Only TSSEL00, 03, 04, 05, 06, 07, and 13 are valid.
- 20- and 24-pin products: TSSEL00, 03, 04, 05, 06, 07, 08, 09, 10, 11, and 13 are valid.

Correct:

These registers select whether the touch pin function or another multiplexed function is used with the P01, P03 to P07, P16, P17, P20 to P23, and P41 to P43 pins.
These registers can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation clears these registers to 00H.

Figure 15-23. Format of Touch Pin Function Select Registers 0, 1 (TSSEL0, TSSEL1)

Address: F030AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TSSEL0	TSSEL07	TSSEL06	TSSEL05	TSSEL04	TSSEL03	TSSEL02	TSSEL01	TSSEL00

Address: F030BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TSSEL1	0	TSSEL14	TSSEL13	TSSEL12	TSSEL11	TSSEL10	TSSEL09	TSSEL08

TSSELxx	Selection of a function other than the TSxx touch pin function (multiplexed function) or the touch pin function for the Pmn pin
0	Use the Pmn pin for a function other than the touch pin function (multiplexed function).
1	Use the Pmn pin for the touch pin function.

TSSELxx	Pmn/TSxx
TSSEL00	P01/TS00
TSSEL01	P16/TS01
TSSEL02	P16/TS02
TSSEL03	P03/TS03
TSSEL04	P04/TS04

TSSELxx	Pmn/TSxx
P01/TS00	P05/TS05
TSSEL06	P06/TS06
TSSEL07	P07/TS07
TSSEL08	P23/TS08
TSSEL09	P22/TS09

TSSELxx	Pmn/TSxx
TSSEL10	P21/TS10
TSSEL11	P20/TS11
TSSEL12	P42/TS12
TSSEL13	P41/TS13
TSSEL14	P43/TS14

Remark To use the Pmn pins as touch pins (TSSELxx = 1), be sure to set the PUmn bit of the PUm register, and POMmn bit of the POMm register to “0”.

- 10-pin products: Only TSSEL00, 03, and 04 are valid.
- 16-pin products: Only TSSEL00, 03, 04, 05, 06, 07, and 13 are valid.
- 20- and 24-pin products: TSSEL00, 03, 04, 05, 06, 07, 08, 09, 10, 11, and 13 are valid.

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10. 15.3.21 TSCAP pin setting register (VTSEL) (Page 734)

Incorrect:

When the touch pin function is in use (when the TSSELxx bit is set to 1), the setting of the VTSEL register is effective.

This register disables or enables input to the P02 pin.

The VTSEL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 15-24. Format of TSCAP Pin Setting Register (VTSEL)

Address: F030DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
VTSEL	0	0	0	0	0	0	0	VTSEL0

VTSEL0	Disabling or enabling of input to the P02 pin
0	When the touch pin function is in use, input to the P02 pin is disabled.
1	**When the touch pin function is in use**, input to the P02 pin is enabled.

Correct:

When the touch pin function is in use (when the TSSELxx bit is set to 1), the setting of the VTSEL register is effective.

This register disables or enables input to the P02 pin.

The VTSEL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 15-24. Format of TSCAP Pin Setting Register (VTSEL)

Address: F030DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
VTSEL	0	0	0	0	0	0	0	VTSEL0

VTSEL0	Disabling or enabling of input to the P02 pin
0	When the touch pin function is in use, input to the P02 pin is disabled.
1	When the digital I/O function is in use, input to the P02 pin is enabled.

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11. 15.4.2 Measurement modes (Page 743, Page 746, Page 750)

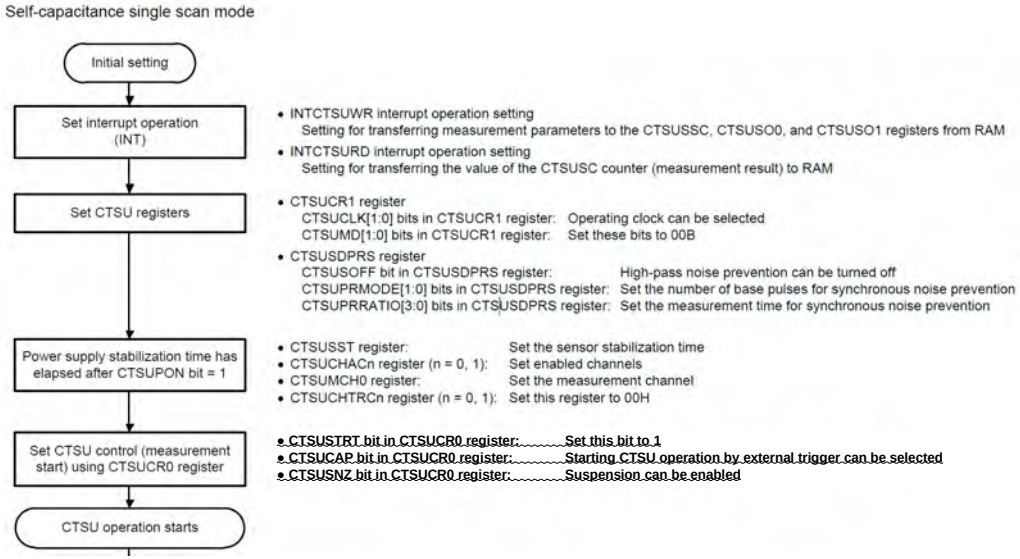
Incorrect:

(Page 743)

(3) Self-capacitance single scan mode operation

[omitted]

Figure 15-35. Software Flowchart and Operation Example of Self-Capacitance Single Scan Mode



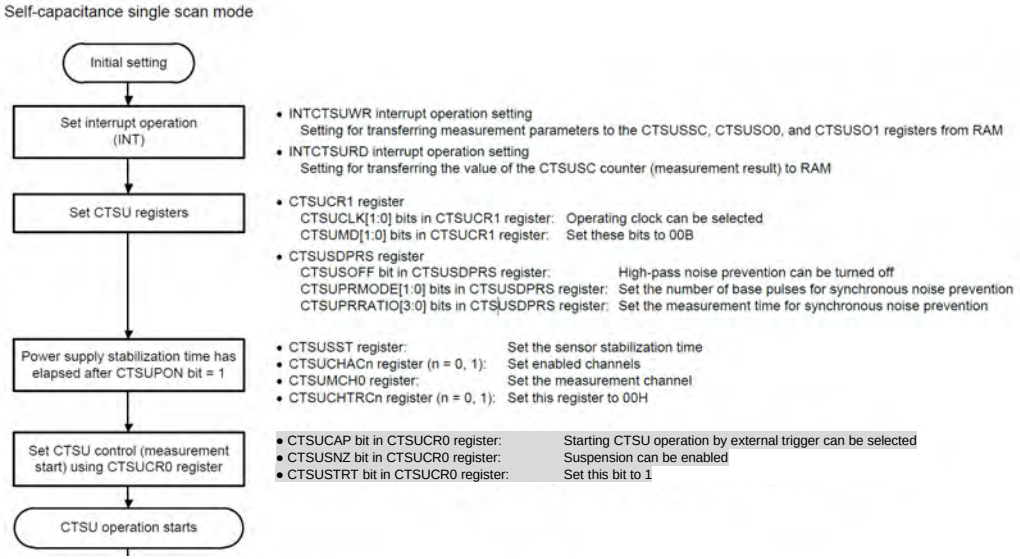
[omitted]

Correct:

(3) Self-capacitance single scan mode operation

[omitted]

Figure 15-35. Software Flowchart and Operation Example of Self-Capacitance Single Scan Mode



[omitted]

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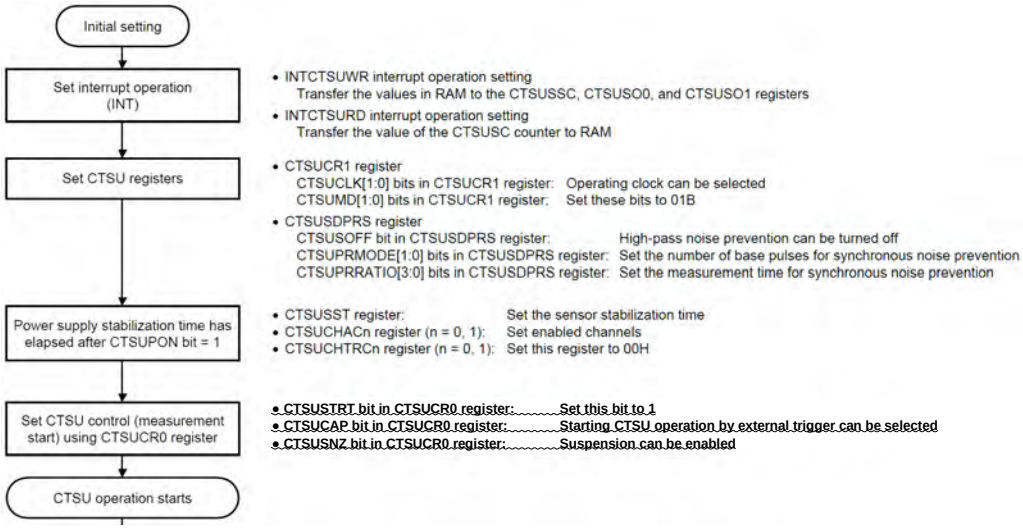
(4) Self-capacitance multi-scan mode operation

[omitted]

Figure 15-37. Software Flow and Operation Example of Self-Capacitance Multi-Scan Mode

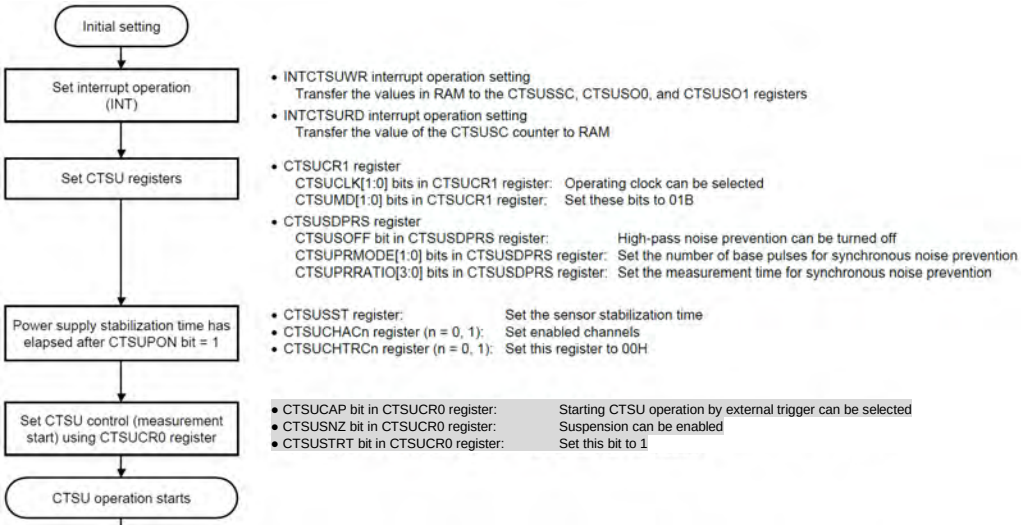


[omitted]

(4) Self-capacitance multi-scan mode operation

[omitted]

Figure 15-37. Software Flow and Operation Example of Self-Capacitance Multi-Scan Mode



[omitted]

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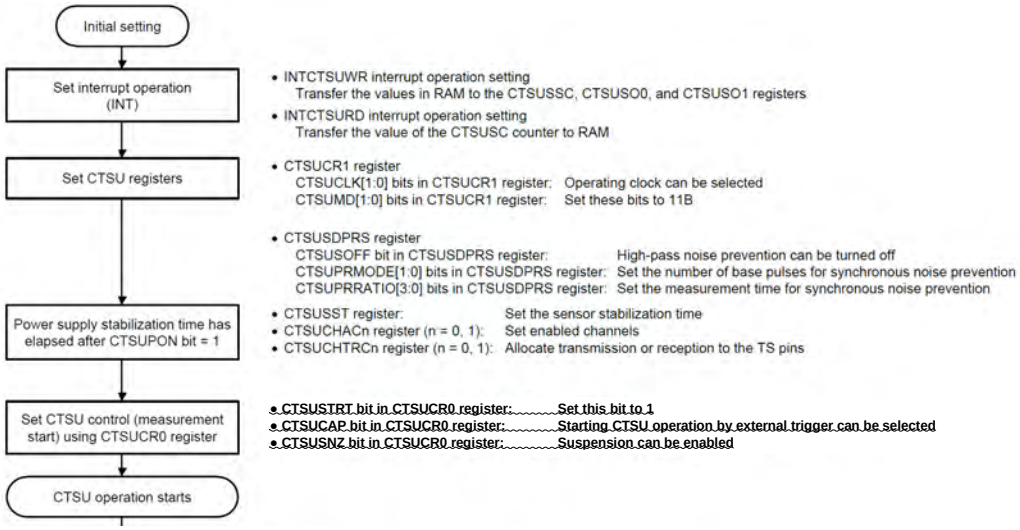
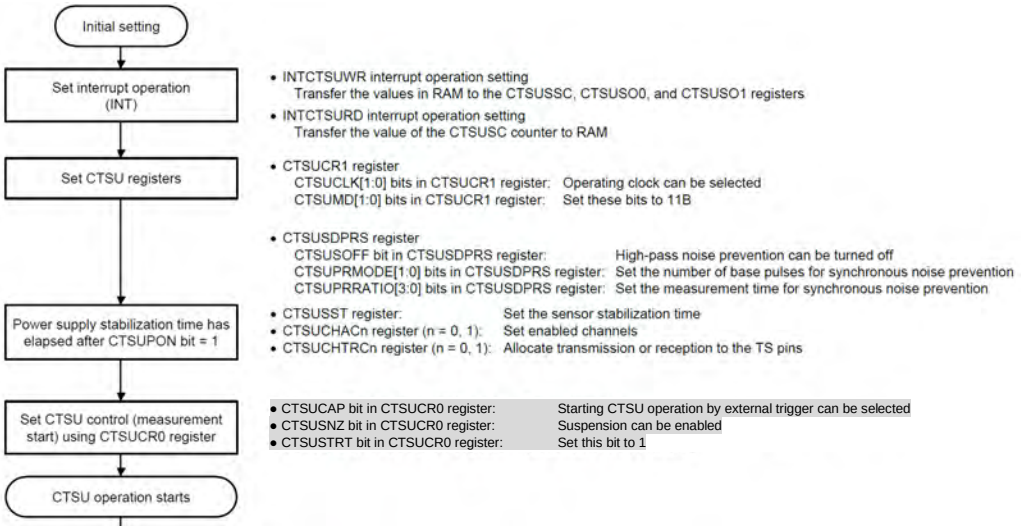
Figure 15-39. Software Flowchart and Operation Example of Mutual Capacitance Full Scan Mode



[omitted]

Figure 15-39. Software Flowchart and Operation Example of Mutual Capacitance Full Scan Mode



[omitted]

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12. 15.4.3 Items common to multiple modes (Page 756, Page 757)

Incorrect:
(Page 756)

(3) Measurement start conditions

[omitted]

● External trigger (an interval interrupt signal from the 12-bit interval timer)
Setting the CTSUCAP bit in the CTSUCR0 register to 1 selects an external trigger (an interval interrupt signal input from the 12-bit interval timer as the trigger to start measurement by the CTSU. **Start measurement by the CTSU after setting the 12-bit interval timer for the required external trigger**. After the CTSUSTRT bit in the CTSUCR0 register is set to 1, measurement starts in response to rising edges of the selected external trigger.

[omitted]

4. Activate the 12-bit interval timer.
   After activation of the timer, the CPU can be placed in STOP mode.

Correct:

(3) Measurement start conditions

[omitted]

● External trigger (an interval interrupt signal from the 12-bit interval timer)
Setting the CTSUCAP bit in the CTSUCR0 register to 1 selects an external trigger (an interval interrupt signal input from the 12-bit interval timer as the trigger to start measurement by the CTSU. In external trigger mode, set the 12-bit interval timer before starting measurement by the CTSU. After the CTSUSTRT bit in the CTSUCR0 register is set to 1, measurement starts in response to rising edges of the selected external trigger.

[omitted]

4. Activate the 12-bit interval timer.
   After activation of the timer, the CPU can be placed in STOP mode.

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(4) By enabling suspension of the CTSU and the start of measurement operation, low-power operation is possible during the period until an external trigger signal is detected (i.e., in the wait state for measurement).
The 12-bit interval timer generates the start-measurement trigger signal and controls the measurement interval (which is simply the timer period).
When low-power operation is required, follow the procedure below to start measurement.

● Configuration
Set the 12-bit interval timer to use an external trigger as the source for starting measurement.

● Setting before the start of measurement
Set the CTSUSTRT bit to 1 after selecting an external trigger (the CTSUCAP bit = 1) and enabling suspension (the CTSUSNZ bit = 1). In the suspended state, placing the CPU in STOP mode is possible.
The CTSU hard macro makes a transition to the suspended state when the CTSUSNZ bit is set to 1.

● Starting measurement from the suspended state
The CTSU starts measurement when a rising edge of the external trigger signal is detected.

● Setting after the end of measurement
A measurement end interrupt is generated after the end of measurement. After that, proceed with CPU processing.
To proceed with re-measurement after the end of measurement, make settings by following steps (a), (b), and (c) below after the measurement end interrupt. Note that the setting of the CTSUSTRT bit is 1 after the measurement end interrupt, and settings other than that stated in (a) are prohibited for the CTSUCR0 register at this time. Therefore, be sure to follow the steps below when making the settings.

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(a) End external trigger mode.
Write 0 to the CTSUSTRT bit and 1 to the CTSUINIT bit at the same time (for a forced stop).

Note that reading of the results of measurement must have been completed before operation is forcibly stopped.

(b) Disable suspension once.
Set the CTSUSNZ bit to 0.

(c) Place the CTSU in the suspended state (waiting for an external trigger) again.
Set the CTSUCAP and CTSUSNZ bits to 1, and set the CTSUSTRT bit to 1.

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(4) Intermittent operation using the software trigger (the CTSUCAP bit = 0)
In the system that does not use an external trigger (the CTSUCAP bit = 1), the interval of measurement is generated by an interrupt, etc. and touch measurement operation is started by software (the CTSUSTRT bit = 1).
By enabling suspension (the CTSUSNZ bit = 1) in the waiting state for the start of touch measurement, the CTSU hard macro is placed in the suspended state, which decreases power consumption during the wait state.
If the interval of measurement is long and lower power consumption is required, follow the procedure below to start measurement.

● Configuration
Set the 12-bit interval timer as the source for returning the system from standby.

● Setting the CTSU before standby of the system
Place the system in the standby state **while the CTSUCAP bit is 0, the CTSUSNZ bit is 1, and the CTSUSTRT bit is 0**. In the SW suspended mode, placing the CPU in STOP mode **is also possible**.
The CTSU hard macro makes a transition to the suspended state when the CTSUSNZ bit is set to 1.

● Starting measurement after return of the system from standby
To start measurement, follow the procedure below after return of the system from standby.

1. Set the CTSUSNZ bit to 0 to release the CTSU hard macro from the suspended state.
2. **Wait for** at least 64 cycles of the base clock.
   [Example] When the base clock is at 0.5 MHz, wait for at least 128 µs.
   (2 µs × 64 cycles = 128 µs)
3. **Start measurement by a software trigger.**

(5) Intermittent operation using the software trigger (the CTSUCAP bit = 0)
By enabling suspension in the state of waiting for the start of measurement. low-power operation is possible in the wait state for measurement.
In the system that uses a software trigger (i.e., the system that does not use an external trigger), the interval of measurement is generated by an interrupt, etc. and touch measurement operation is started by software.
When low-power operation is required, follow the procedure below to start measurement.

● Configuration
Set the 12-bit interval timer as the source for returning the system from standby.

● Setting the CTSU before standby of the system
Place the system in the standby state while a software trigger is selected (the CTSUCAP bit = 0), suspension is enabled (the CTSUSNZ bit = 1), and the setting of the CTSUSTRT bit is 0. In the SW suspended mode, placing the CPU in STOP mode is possible.
The CTSU hard macro makes a transition to the suspended state when the CTSUSNZ bit is set to 1.

● Starting measurement after return of the system from standby
To start measurement, follow the procedure below after return of the system from standby.

1. Set the CTSUSNZ bit to 0 to release the CTSU hard macro from the suspended state.
2. Secure a wait of at least 64 cycles of the base clock.
   [Example] When the base clock is at 0.5 MHz, wait for at least 128 µs.
   (2 µs × 64 cycles = 128 µs)
3. Start measurement by setting the CTSUSTRT bit to 1.

● Setting after the end of measurement
A measurement end interrupt is generated after the end of measurement. After that, proceed with CPU processing.
To resume the SW suspended state after the end of measurement, set the CTSUSNZ bit to 1.

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13. 26.6.4 SPOR circuit characteristics (Page 914)

Incorrect:

[T_A = −40 to +85°C, V_{SS} = 0 V]

Item		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage	Power supply voltage level	V_{SPOR0}	Power supply rising	4.08	4.28	4.45	V
		V_{SPDR0}	Power supply falling	4.00	4.20	4.37	V
		V_{SPOR1}	Power supply rising	2.76	2.90	3.02	V
		V_{SPDR1}	Power supply falling	2.70	2.84	2.96	V
		V_{SPOR2}	Power supply rising	2.44	2.57	2.68	V
		V_{SPDR2}	Power supply falling	2.40	2.52	2.62	V
		V_{SPOR3}	Power supply rising		2.16		V
		V_{SPDR3}	Power supply falling		2.11		V
Minimum pulse width[Note 1]		T_{SPW}		300			µs

Note 1. Time required for the reset operation by the SPOR circuit when VDD falls below VSPDR.

Caution Make sure to keep the internal reset state by the SPOR or an external reset until the power supply voltage (VDD) reaches the operating voltage range shown in 26.4 AC Characteristics.

Cncorrect:

[T_A = −40 to +85°C, V_{SS} = 0 V]

Item		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage	Power supply voltage level	V_{SPOR0}	Power supply rising	4.08	4.28	4.45	V
		V_{SPDR0}	Power supply falling	4.00	4.20	4.37	V
		V_{SPOR1}	Power supply rising	2.76	2.90	3.02	V
		V_{SPDR1}	Power supply falling	2.70	2.84	2.96	V
		V_{SPOR2}	Power supply rising	2.44	2.57	2.68	V
		V_{SPDR2}	Power supply falling	2.40	2.52	2.62	V
		V_{SPOR3}	Power supply rising		2.16	2.25	V
		V_{SPDR3}	Power supply falling		2.11	2.20	V
Minimum pulse width[Note 1]		T_{SPW}		300			µs

Note 1. Time required for the reset operation by the SPOR circuit when VDD falls below VSPDR.

Caution Make sure to keep the internal reset state by the SPOR or an external reset until the power supply voltage (VDD) reaches the operating voltage range shown in 26.4 AC Characteristics.

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14. 27.6.4 SPOR circuit characteristics (Page 939)

Incorrect:

[T_A = −40 to +85°C, V_{SS} = 0 V]

Item		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage	Power supply voltage level	V_{SPOR0}	Power supply rising	4.08	4.28	4.45	V
		V_{SPDR0}	Power supply falling	4.00	4.20	4.37	V
		V_{SPOR1}	Power supply rising	2.76	2.90	3.02	V
		V_{SPDR1}	Power supply falling	2.70	2.84	2.96	V
		V_{SPOR2}	Power supply rising	2.44	2.57	2.68	V
		V_{SPDR2}	Power supply falling	2.40	2.52	2.62	V
		V_{SPOR3}	Power supply rising		2.16		V
		V_{SPDR3}	Power supply falling		2.11		V
Minimum pulse width[Note 1]		T_{SPW}		300			µs

Note 1. Time required for the reset operation by the SPOR circuit when VDD falls below VSPDR.

Caution Make sure to keep the internal reset state by the SPOR or an external reset until the power supply voltage (VDD) reaches the operating voltage range shown in 26.4 AC Characteristics.

Correct:

[T_A = −40 to +105°C, V_{SS} = 0 V]

Item		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage	Power supply voltage level	V_{SPOR0}	Power supply rising	4.08	4.28	4.45	V
		V_{SPDR0}	Power supply falling	4.00	4.20	4.37	V
		V_{SPOR1}	Power supply rising	2.76	2.90	3.02	V
		V_{SPDR1}	Power supply falling	2.70	2.84	2.96	V
		V_{SPOR2}	Power supply rising	2.44	2.57	2.68	V
		V_{SPDR2}	Power supply falling	2.40	2.52	2.62	V
		V_{SPOR3}	Power supply rising		2.16	2.25	V
		V_{SPDR3}	Power supply falling		2.11	2.20	V
Minimum pulse width[Note 1]		T_{SPW}		300			µs

Note 1. Time required for the reset operation by the SPOR circuit when VDD falls below VSPDR.

Caution Make sure to keep the internal reset state by the SPOR or an external reset until the power supply voltage (VDD) reaches the operating voltage range shown in 27.4 AC Characteristics.

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