To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A287A/E	Rev.	1.0
Title	H8/38602 Group specification changes		Information Category	Technical Notification		
Applicable Product	H8/38602 Group	Lot No. All	Reference Document	H8/38602 Group Hardware manual (REJ09B0152-0100Z Rev.1.00)		

We wish to notify you of the following corrections of the H8/38602 Group Hardware Manual, as detailed below. Shaded parts indicate the difference from Rev.1.00 (except table 5.1, figures 21.1, 21.2, 21.3, 21.4, 21.5, 21.6, 21.7, and 21.8).

Section 1 Overview

1.4 Pin Functions

Table 1.1 Pin Functions

Type	Symbol	Pin No.	I/O	Functions
Interrupt pins	$\overline{NMI}$	16	Input	NMI interrupt request pin. Non-maskable interrupt request input pin. In the F-ZTAT version, user mode / boot mode is set up with this pin at the time of reset release. In order to transition to user mode, pull up this pin to Vcc level.

Section 5 Power-Down Modes

5.1 Register Descriptions

5.1.1 System Control Register 1 (SYSCR1)

Bit	Bit Name	Initial Value	R/W	Description
6	STS2	0	R/W	Standby Timer Select 2 to 0
5	STS1	0	R/W	Designate the time the CPU and peripheral modules wait for stable clock operation after exiting from standby mode, subactive mode, or watch mode to active mode or sleep mode due to an interrupt. The designation should be made according to the operating frequency so that the waiting time is at least equal to the oscillation stabilization time. The relationship between the specified value and the number of wait states is shown in table 5.1. When an external clock is to be used, the minimum value (STS2 = 1, STS1 = 1, STS0 = 1) is recommended. When the on-chip oscillator is to be used, the minimum value (STS2 = 1, STS1 = 1, STS0 = 1) is recommended. If a setting other than the recommended value is made, operation may start before the end of the waiting time.
4	STS0	0	R/W	

Table 5.1 Operating Frequency and Waiting Time

Bit				Operating Frequency						
STS2	STS1	STS0	Waiting Time	10 MHz	8 MHz	6 MHz	5 MHz	4 MHz	3 MHz	2 MHz
0	0	0	8,192 states	819.2	1,024.0	1,365.3	1,638.4	2,048.0	2,730.7	4,096.0
		1	16,384 states	1,638.4	2,048.0	2,730.7	3,276.8	4,096.0	5,461.3	8,192.0
	1	0	1,024 states	102.4	128.0	170.7	204.8	256.0	341.3	512.0
		1	2,048 states	204.8	256.0	341.3	409.6	512.0	682.7	1,024.0
1	0	0	4,096 states	409.6	512.0	682.7	819.2	1,024.0	1,365.3	2,048.0
		1	256 states	25.6	32.0	42.7	51.2	64.0	85.3	128.0
	1	0	512 states	51.2	64.0	85.3	102.4	128.0	170.7	256.0
		1	16 states	1.6	2.0	2.7	3.2	4.0	5.3	8.0

Note: 1. Time unit is µs.

2. For the oscillation stabilization time, refer to table 21.3, table 21.14, and figure 21.22 of section 21, Electrical Characteristics.

: Recommended value when crystal resonator is used (V_{CC} = 2.7 V to 3.6 V) : Reference value when crystal resonator is used

: Recommended value when ceramic resonator is used (V_{CC} = 2.2 V to 3.6 V) : Reference value when ceramic resonator is used

5.5 On-Chip Oscillator and Operation Mode

The on-chip oscillator can be used as the clock source for the watchdog timer (WDT), subclock generation circuit (ϕ_W=R_{OSC}/32), and system clock generation circuit (ϕ_{OSC}=R_{OSC}).

When the on-chip oscillator is used as the clock source for the watchdog timer (WDT), it operates in any modes, such as active, sleep, subactive, subsleep, watch, and standby modes.

When the on-chip oscillator is used as the clock source for the subclock generation circuit, it stops in standby mode and operates in other modes.

When the on-chip oscillator is used only as the clock source for the system clock generation circuit, it operates in active and sleep modes but halts the operation in subactive, subsleep, watch, and standby modes.

When the on-chip oscillator is not used as the clock source for the watchdog timer (WDT), subclock generation circuit, or system clock generation circuit, it halts the operation.

The on-chip oscillator operates at a reset and after a reset, because the watchdog timer (WDT) selects the on-chip oscillator as the clock source for the initial value.

Section 11 Realtime Clock (RTC)

11.3 Register Descriptions

11.3.7 Clock source Select Register (RTCCSR)

RTCCSR selects clock source. A free running counter controls start/stop of counter operation by the RUN bit in RTCCR1. When a clock other than 32.768 kHz is selected, the RTC is disabled and operates as an 8-bit free running counter. WHEN the RTC operates as an 8-bit free running counter, RSECDR enables counter values to be read. An interrupt can be generated by setting 1 to the FOIE bit in RTCCR2 and enabling an overflow interrupt of the free running counter. A clock in which the system clock is divided by 32, 16, 8, or 4 is output in active and sleep modes. ϕ_W is output in active, sleep, subactive, subsleep, and watch modes.

Section 13 Asynchronous Event Counter (AEC)

13.6 Usage Notes

2. For input to the AEVH and AEVL pins, use a clock with a frequency of up to 4.2 MHz within the range from 1.8 V to 3.6 V and up to 10 MHz within the range from 2.7 V to 3.6 V. Refer to table 21.3 and table 21.14 of section 21, Electrical Characteristics for the high and low widths of the clock. The duty cycle is immaterial.

6. As synchronization is established internally when an IRQAEC interrupt is generated, a maximum error of 1 tcyc or 1tsubcyc will occur between clock halting and interrupt acceptance.

Section 17 A/D Converter

17.3 Register Descriptions

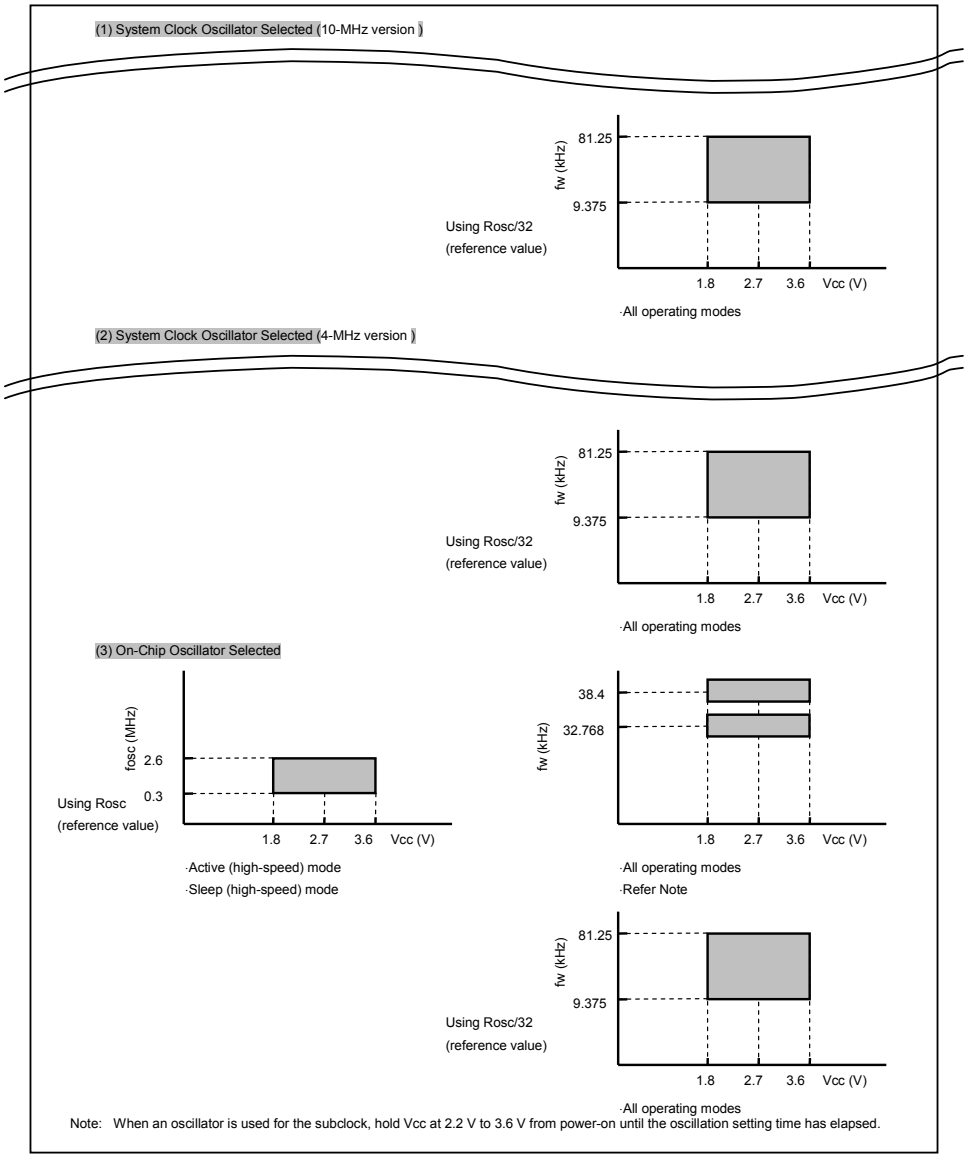
17.3.1 A/D Result Register (ADRR)

ADRR is a 16-bit read-only register that stores the results of A/D conversion. The upper 10 bits of the data are stored in ADRR. ADRR can be read by the CPU at any time, but the ADRR value during A/D conversion is undefined. After A/D conversion is completed, the conversion result is stored as 10-bit data, and this data is retained until the next conversion operation starts. The initial value of ADRR is undefined. When reading this register, read in WORD size.

Section 21 Electrical Characteristics

21.2 Electrical Characteristics for F-ZTAT Version

21.2.1 Power Supply Voltage and Operating Range



Note: When an oscillator is used for the subclock, hold Vcc at 2.2 V to 3.6 V from power-on until the oscillation setting time has elapsed.

Figure 21.1 Power Supply Voltage and Oscillation Frequency Range

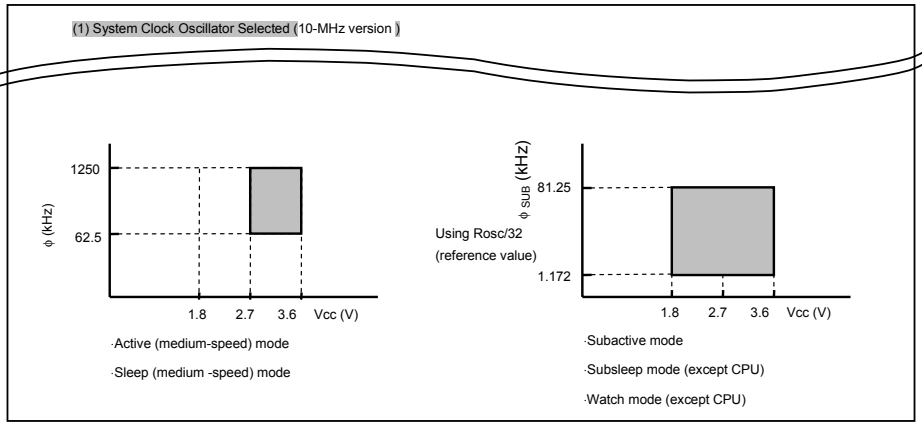


Figure 21.2 Power Supply Voltage and Operating Frequency Range (1)

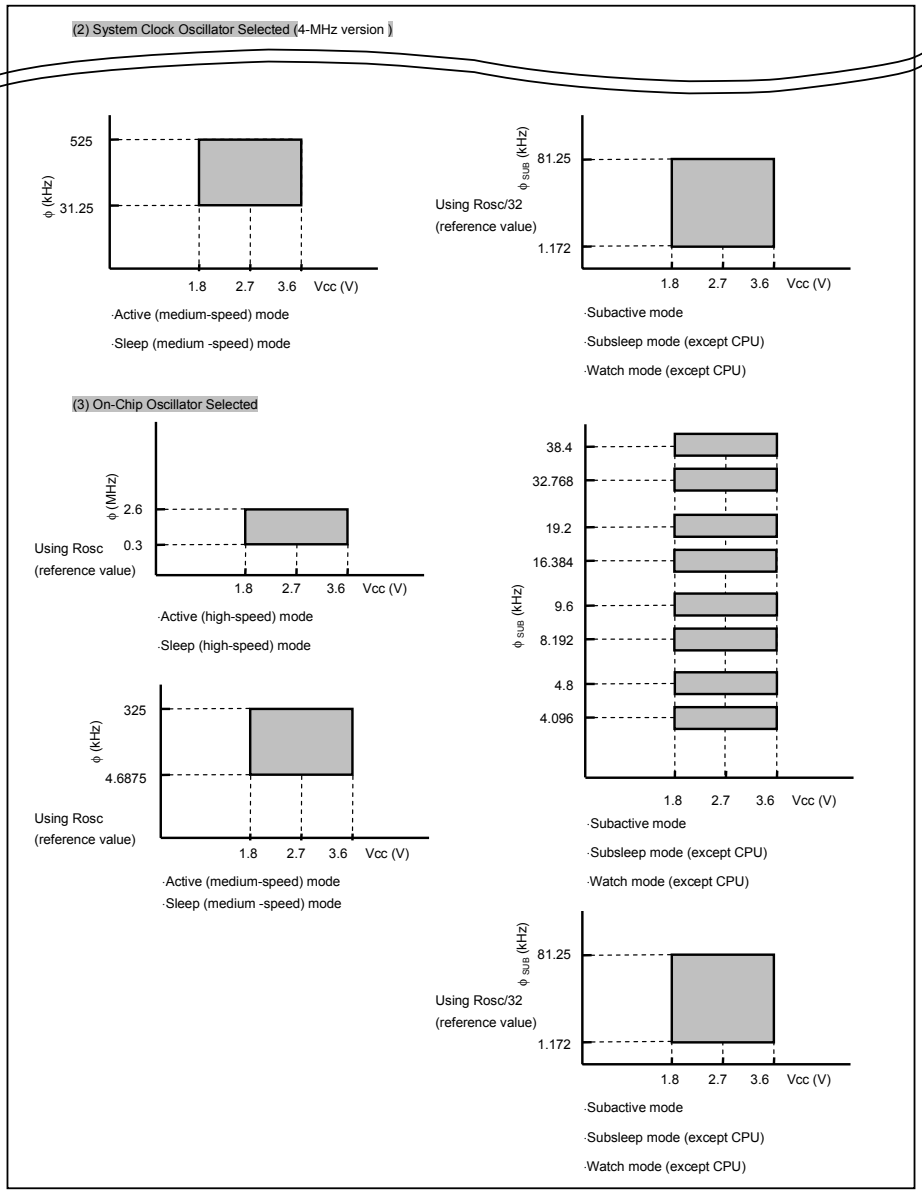


Figure 21.3 Power Supply Voltage and Operating Frequency Range (2)

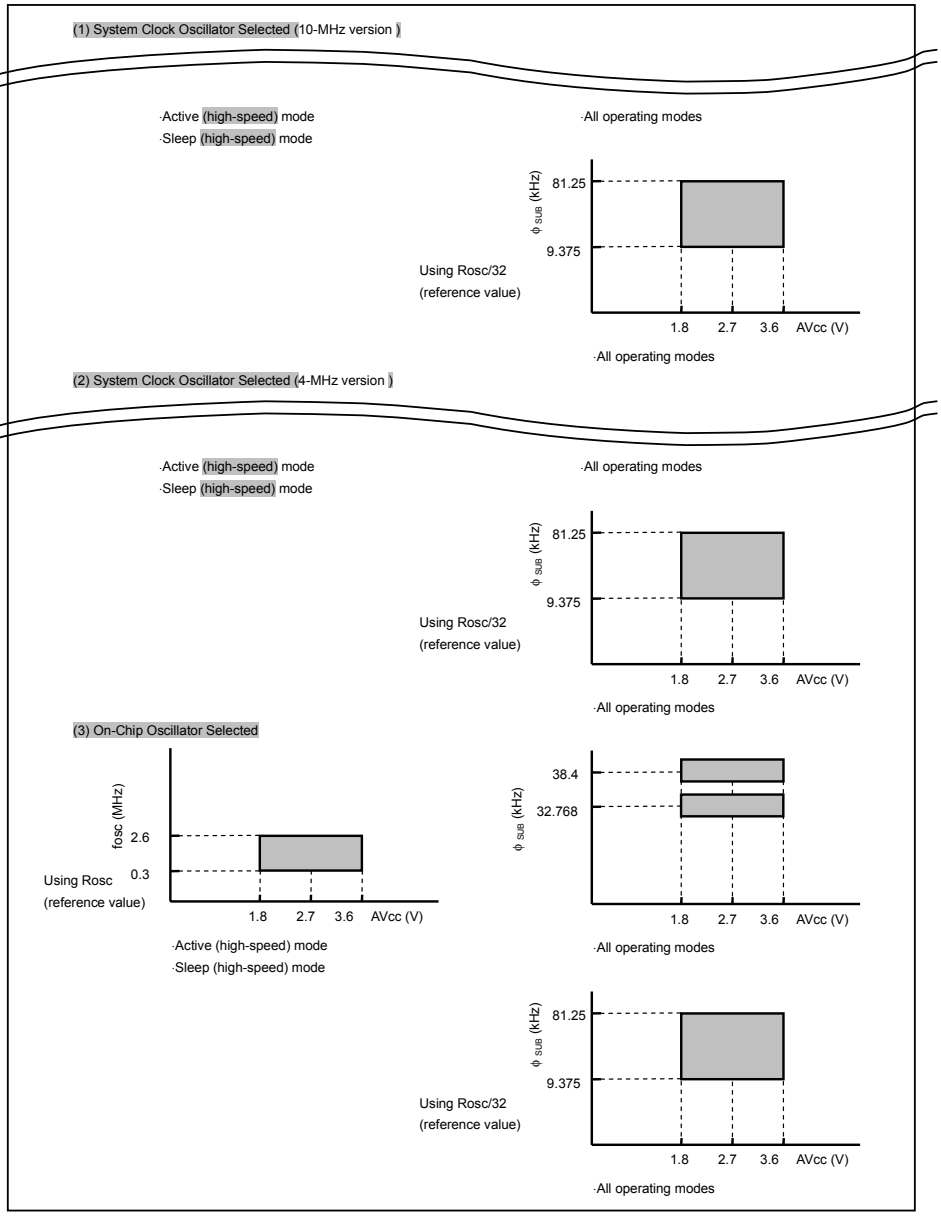


Figure 21.4 Analog Power Supply Voltage and Oscillation Frequency Range of A/D Converter

21.2.2 DC Characteristics

Table 21.2 lists the DC characteristics.

Table 21.2 DC Characteristics

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Input high voltage	V_{IH}	RES, TEST, NMI*3, AEVL, AEVH, ADTRG, SCK3, IRQAEC		0.9V_{CC}	–	V_{CC} + 0.3	V	
		IRQ0*4, IRQ1*4		0.9V_{CC}	–	AV_{CC} + 0.3		
		RXD3, IrRXD		0.8V_{CC}	–	V_{CC} + 0.3		
		OSC1		0.9V_{CC}	–	V_{CC} + 0.3		
		X1		0.9V_{CC}	–	V_{CC} + 0.3		
		P10 to P12, P30 to P32, P82 to P84, P90 to P93, SSI, SSO, SSCK, SCS, FTCI, FTIOA, FTIOB, FTIOC, FTIOD, E7_0 to E7_2, SCL, SDA		0.8V_{CC}	–	V_{CC} + 0.3		
		PB0 to PB5		0.8V_{CC}	–	AV_{CC} + 0.3		
Input low voltage	V_{IL}	RES, TEST, NMI*3, IRQ0, IRQ1, IRQAEC, AEVL, AEVH, ADTRG, SCK3		–0.3	–	0.1V_{CC}	V	
		RXD3, IrRXD		–0.3	–	0.2V_{CC}		
		OSC1		–0.3	–	0.1V_{CC}		
		X1		–0.3	–	0.1V_{CC}		
		P10 to P12, P30 to P32, P82 to P84, P90 to P93, PB0 to PB5, SSI, SSO, SSCK, SCS, FTCI, FTIOA, FTIOB, FTIOC, FTIOD, E7_0 to E7_2, SCL, SDA		–0.3	–	0.2V_{CC}		
Output high voltage	V_{OH}	P10 to P12, P30 to P32,	$-I_{OH}$ = 1.0 mA V_{CC} = 2.7 V to 3.6 V	V_{CC}–1.0	–	–	V	
		P90 to P93	$-I_{OH}$ = 0.1 mA	V_{CC}–0.3	–	–		
		P82 to P84	$-I_{OH}$ = 1.0 mA V_{CC} = 2.7 V to 3.6 V	V_{CC}–1.0	–	–		
			$-I_{OH}$ = 0.1 mA	V_{CC}–0.3	–	–		
Output low voltage	V_{OL}	P10 to P12, P30 to P32, P90 to P93	I_{OL} = 0.4 mA	–	–	0.5	V	
		P82 to P84	I_{OL} = 15 mA V_{CC} = 2.7 V to 3.6 V	–	–	1.0		
			I_{OL} = 10 mA V_{CC} = 2.2 V to 3.6 V	–	–	0.5		
			I_{OL} = 8 mA	–	–	0.5		
		SCL, SDA	I_{OL} = 3.0 mA	–	–	0.4		
Input/output leakage current	$\lvert I_{IL} \rvert$	RES, TEST, NMI*3, OSC1, X1, P10 to P12, P30 to P32, P82 to P84, P90 to P93, E7_0 to E7_2	V_{IN} = 0.5 V to V_{CC}–0.5 V	–	–	1.0	µA	
		PB0 to PB5	V_{IN} = 0.5 V to AV_{CC}–0.5 V	–	–	1.0		
Pull-up MOS current	$-I_P$	P10 to P12, P30 to P32, P82 to P84, P90 to P93	V_{CC} = 3 V, V_{IN} = 0 V	30	–	180	µA	
Input capacitance	C_{IN}	All input pins except power supply pin	f = 1 MHz, V_{IN} = 0 V, Ta = 25°C	–	–	15.0	pF	

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Active mode current consumption	I_{OPE1}	V_{CC}	Active (high -speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz	–	1.1	–	mA	Max. guideline = 1.1 × typ.*1*2
			Active (high-speed) mode, V_{CC} = 3 V, f_{OSC} = R_{OSC}	–	1.2	–		Max. guideline = 1.1 × typ.*1*2 Reference value
			Active (high-speed) mode, V_{CC} = 3 V, f_{OSC} = 4.2 MHz	–	2.6	4.0		*1*2 4 MHz version
			Active (high-speed) mode, V_{CC} = 3 V, f_{OSC} = 10 MHz	–	6.0	10.0		*1*2 10 MHz version
	I_{OPE2}	V_{CC}	Active (medium -speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz, ϕ_{OSC}/64	–	0.4	–	mA	Max. guideline = 1.1 × typ.*1*2
			Active (medium -speed) mode, V_{CC} = 3 V, f_{OSC} = 4.2 MHz, ϕ_{OSC}/64	–	0.7	1.1		*1*2 4 MHz version
			Active (medium -speed) mode, V_{CC} = 3 V, f_{OSC} = 10 MHz, ϕ_{OSC}/64	–	0.8	1.3		*1*2 10 MHz version
Sleep mode current consumption	I_{SLEEP}	V_{CC}	V_{CC} = 1.8 V, f_{OSC} = 2 MHz	–	0.9	–	mA	Max. guideline = 1.1 × typ.*1*2
			V_{CC} = 3 V, f_{OSC} = 4.2 MHz	–	2.0	3.2		*1*2 4 MHz version
			V_{CC} = 3 V, f_{OSC} = 10 MHz	–	4.2	6.4		*1*2 10 MHz version
Subactive mode current consumption	I_{SUB}	V_{CC}	V_{CC} = 2.7 V, 32-kHz crystal resonator (ϕ_{SUB} = ϕ_W/8)	–	7.0	–	µA	*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator (ϕ_{SUB} = ϕ_W/2)	–	25	–		*1*2 Reference value
			V_{CC} = 2.7 V, on-chip oscliiator/32 (ϕ_{SUB} = ϕ_W = R_{OSC}/32)	–	80	–		*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator (ϕ_{SUB} = ϕ_W)	–	45	75		*1*2
Subsleep mode current consumption	I_{SUBSP}	V_{CC}	V_{CC} = 2.7 V, 32-kHz crystal resonator (ϕ_{SUB} = ϕ_W/2)	–	3.5	–	µA	*1*2 Reference value
			V_{CC} = 2.7 V, on-chip oscliiator/32 (ϕ_{SUB} = ϕ_W = R_{OSC}/32)	–	34	–		*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator (ϕ_{SUB} = ϕ_W)	–	5.1	16.0		*1*2
Watch mode current consumption	I_{WATCH}	V_{CC}	V_{CC} = 1.8 V, Ta = 25°C, 32-kHz crystal resonator	–	0.5	–	µA	*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator	–	1.5	5.0		*1*2
Standby mode current consumption	I_{STBY}	V_{CC}	V_{CC} = 3.0 V, Ta = 25°C, 32-kHz crystal resonator not used	–	0.1	–	µA	*1*2 Reference value
			32-kHz crystal resonator not used	–	1.0	5.0		*1*2
RAM data retaining voltage	V_{RAM}	V_{CC}		1.5	–	–	V	
Allowable output low current (per pin)	I_{OL}	Output pins except port 8		–	–	0.5	mA	
		Port 8		–	–	15.0		
Allowable output low current (total)	ΣI_{OL}	Output pins except port 8		–	–	20.0	mA	
		Port 8		–	–	45.0		
Allowable output high current (per pin)	$-I_{OH}$	All output pins	V_{CC} = 2.7 V to 3.6 V	–	–	2.0	mA	
			Other than above	–	–	0.2		
Allowable output high current (total)	$\Sigma-I_{OH}$	All output pins		–	–	10.0	mA	

Notes: 1. Pin states during current measurement.

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	Oscillator Pins
Active (high-speed) mode (I_{OPE1})	V_{CC}	Only CPU operates	V_{CC}	System clock oscillator: Crystal resonator Subclock oscillator: Pin X1 = GND
Active (medium-speed) mode (I_{OPE2})				
Sleep mode	V_{CC}	Only on-chip timers operate	V_{CC}	
Subactive mode	V_{CC}	Only CPU operates	V_{CC}	System clock oscillator: Crystal resonator Subclock oscillator: Crystal resonator
Subsleep mode	V_{CC}	Only on-chip timers operate, CPU stops	V_{CC}	
Watch mode	V_{CC}	Only timer base operates, CPU stops	V_{CC}	
Standby mode	V_{CC}	CPU and timers both stop, SUBSTP = 1	V_{CC}	System clock oscillator: Crystal resonator Subclock oscillator: Crystal resonator

2. Excludes current in pull-up MOS transistors and output buffers.
3. Used for the determination of user mode or boot mode when the reset is released.
4. When bits IRQ0S1 and IRQ0S0 are set to B'01 or B'10, and bits IRQ1S1 and IRQ1S0 are set to B'01 or B'10, the Max. value becomes V_{CC} + 0.3 (V).

21.2.3 AC Characteristics

Table 21.3 lists the control signal timing, table 21.4 lists the serial interface timing, table 21.5 lists the synchronous serial communization unit timing, and table 21.6 lists the I^2C bus interface timing.

Table 21.3 Control Signal Timing

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Reference Figure
System clock oscillation frequency	f_{OSC}	OSC1, OSC2	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	4.0	–	10.0	MHz	
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	2.0	–	4.2		
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC1, OSC2	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	100	–	250	ns	Figure 21.9
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	238	–	500		
System clock (ϕ) cycle time	t_{cyc}			1	–	64	t_{OSC}	
				–	–	32	µs	
On-chip oscillator frequency	f_{ROSC}			0.3	–	2.6	MHz	Reference value
On-chip oscillator clock cycle time	t_{ROSC}			0.38	–	3.3	µs	Reference value
Subclock oscillation frequency	f_w	X1, X2		–	32.768 or 38.4	–	kHz	
Watch clock (ϕ_W) cycle time	t_w	X1, X2		–	30.5 or 26.0	–	µs	Figure 21.9
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}			1	–	8	t_w	*1
Instruction cycle time				2	–	–	t_{cyc} t_{subcyc}	
Oscillation stabilization time	t_{rc}	OSC1, OSC2	Ceramic resonator (V_{CC} = 2.2 V to 3.6 V)	–	20	45	µs	Figure 21.22
			Ceramic resonator Other than above	–	80	–		
			Crystal resonator (V_{CC} = 2.7 V to 3.6 V)	–	300	800		
			Crystal resonator (V_{CC} = 2.2 V to 3.6 V)	–	400	1000		
			Other than above	–	–	50	ms	
			On-chip oscillator (at power-on)	–	15	25	µs	
		X1, X2	V_{CC} = 2.2 V to 3.6 V	–	–	2	s	Figure 4.6 Figure 4.7
			Other than above	–	4	–		
External clock high width	t_{CPH}	OSC1	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	40	–	–	ns	Figure 21.9
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	95	–	–		
		X1		–	15.26 or 13.02	–	µs	
External clock low width	t_{CPL}	OSC1	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	40	–	–	ns	Figure 21.9
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	95	–	–		
		X1		–	15.26 or 13.02	–	µs	
External clock rise time	t_{CPr}	OSC1	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	–	–	10	ns	Figure 21.9
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	–	–	24		
		X1		–	–	55.0	µs	
External clock fall time	t_{CPf}	OSC1	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	–	–	10	ns	Figure 21.9
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	–	–	24		
		X1		–	–	55.0	µs	
$\overline{RES}$ pin low width	t_{REL}	$\overline{RES}$	At power-on or other than below	t_{rc} + 20 × t_{cyc}	–	–	µs	Figure 21.10*2
			Active mode or sleep mode	20	–	–	t_{cyc}	

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Reference Figure
Input pin high width	t_{IH}	IRQ0, IRQ1, NMI, IRQAEC, ADTRG, FTCI, FTIOA, FTIOB, FTIOC, FTIOD		2	–	–	t_{cyc} t_{subcyc}	Figure 21.11
		AEVL, AEVH	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	50	–	–	ns	
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	110				
Input pin low width	t_{IL}	IRQ0, IRQ1, NMI, IRQAEC, ADTRG, FTCI, FTIOA, FTIOB, FTIOC, FTIOD		2	–	–	t_{cyc} t_{subcyc}	Figure 21.11
		AEVL, AEVH	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	50	–	–	ns	
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	110				

Notes: 1. Selected with the SA1 and SA0 bits in the system control register 2 (SYSCR2).

2. For details on the power-on reset characteristics, refer to table 21.10 and figure 21.20.

21.2.4 A/D Converter Characteristics

Table 21.7 lists the A/D converter characteristics.

Table 21.7 A/D Converter Characteristics

V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Analog power supply voltage	AV_{CC}	AV_{CC}		1.8	–	3.6	V	*1
Analog input voltage	AV_{IN}	AN0 to AN5		–0.3	–	AV_{CC} + 0.3	V	
Analog power supply current	AI_{OPE}	AV_{CC}	AV_{CC} = 3.0 V	–	–	1.0	mA	
	AI_{STOP1}	AV_{CC}		–	600	–	µA	** Reference value
	AI_{STOP2}	AV_{CC}		–	–	5	µA	*3
Analog input capacitance	C_{AIN}	AN0 to AN5		–	–	15.0	pF	
Allowable signal source impedance	R_{AIN}			–	–	10.0	kΩ	
Resolution (data length)				–	–	10	Bits	
Nonlinearity error			AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	–	–	±3.5	LSB	
			AV_{CC} = 2.0 V to 3.6 V V_{CC} = 2.0 V to 3.6 V	–	–	±5.5		
			Subclock operating	–	–	±5.5		Subactive mode Subsleep mode *5
			Other than above	–	–	±7.5		*4
Quantization error				–	–	±0.5	LSB	
Absolute accuracy			AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	–	–	±4.0	LSB	
			AV_{CC} = 2.0 V to 3.6 V V_{CC} = 2.0 V to 3.6 V	–	–	±6.0		
			Subclock operating	–	–	±6.0		Subactive mode Subsleep mode *5
			Other than above	–	–	±8.0		*4
Conversion time			AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	12.4	–	124	µA	System clock oscillator Is selected
				31	62	124		On-chip oscillator Is selected Reference value (f_{ROSC} = 1 MHz)
				–	807	–		ϕ_{SUB} = 38.4 kHz
				–	945	–		ϕ_{SUB} = 32.8 kHz
				–	992	–		ϕ_{SUB} = R_{OSC}/32 Reference value (f_{ROSC} = 1 MHz)

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Conversion time			Other than AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	29.5	–	124	µA	System clock oscillator Is selected
				31	62	124		On-chip oscillator Is selected Reference value (f_{ROSC} = 1 MHz)
				–	807	–		ϕ_{SUB} = 38.4 kHz
				–	945	–		ϕ_{SUB} = 32.8 kHz
				–	992	–		$\phi_{SUB} = R_{OSC}/32$ Reference value (f_{ROSC} = 1 MHz)

Notes: 1. Set $AV_{CC} = V_{CC}$ when the A/D converter is not used.

2. AI_{STOP1} is the current at ladder resistance operation while the A/D converter is idle.

3. AI_{STOP2} is the current at reset, in standby mode or watch mode, while the A/D converter is idle.

4. Conversion time is 29.5 µs.

5. Conversion time is 31/ϕ_W.

21.2.5 Comparator Characteristics

Table 21.8 shows the comparator characteristics.

Table 21.8 Comparator Characteristics

V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, unless otherwise specified.

Item	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Accuracy	1LSB = V_{CC}/30	–	1/2	–	LSB	When comparing internal resistance
Conversion time		–	–	15	µs	
External input reference voltage	VCref pin	0.9	–	0.9×V_{CC}	V	
Internal resistance compare voltage		0.9	–	26/30×V_{CC}	V	
Comparator input voltage	COMP0 and COMP1	–0.3	–	AV_{CC} + 0.3	V	
Ladder resistance		–	3	–	MΩ	Reference value

21.2.6 Watchdog Timer Characteristics

Table 21.9 shows the watchdog timer characteristics.

Table 21.9 Watchdog Timer Characteristics

V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
On-chip oscillator overflow time	t_{OVF}			0.2	0.4	–	s	*

Note: * Indicates the time starting from counting from 0 with the on-chip oscillator selected and until 255 is reached and an internal reset occurs.

21.2.7 Power-On Reset Circuit Characteristics

Table 21.10 lists the power-on reset circuit characteristics.

Table 21.10 Power-On Reset Circuit Characteristics

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, Ta = –20 to + 75 °C (regular specifications), Ta = –40 to + 85 °C (wide-range specifications), unless otherwise specified.

Item	Symbol	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Reset voltage	V_rst		0.7V_{CC}	0.8V_{CC}	0.9V_{CC}	V	
Power supply rise time	t_vtr		The V_{CC} rise time should be at least twice as fast as the $\overline{RES}$ rise time.				
Reset count time	t_out		0.8	–	4.0	µs	
			3.2	–	26.7		On-chip oscillator Is selected (reference value)
Count start time	t_cr		Adjustable by the value of the external capacitor of the $\overline{RES}$ pin.				
Pull-up resistance	Rp		60	100	–	kΩ	

21.2.8 Flash Memory Characteristics

Notes: 11. Applies to an operating voltage range when reading data of 2.7 V to 3.6 V.

21.4 Electrical Characteristics for Masked ROM Version

21.4.1 Power Supply Voltage and Operating Range

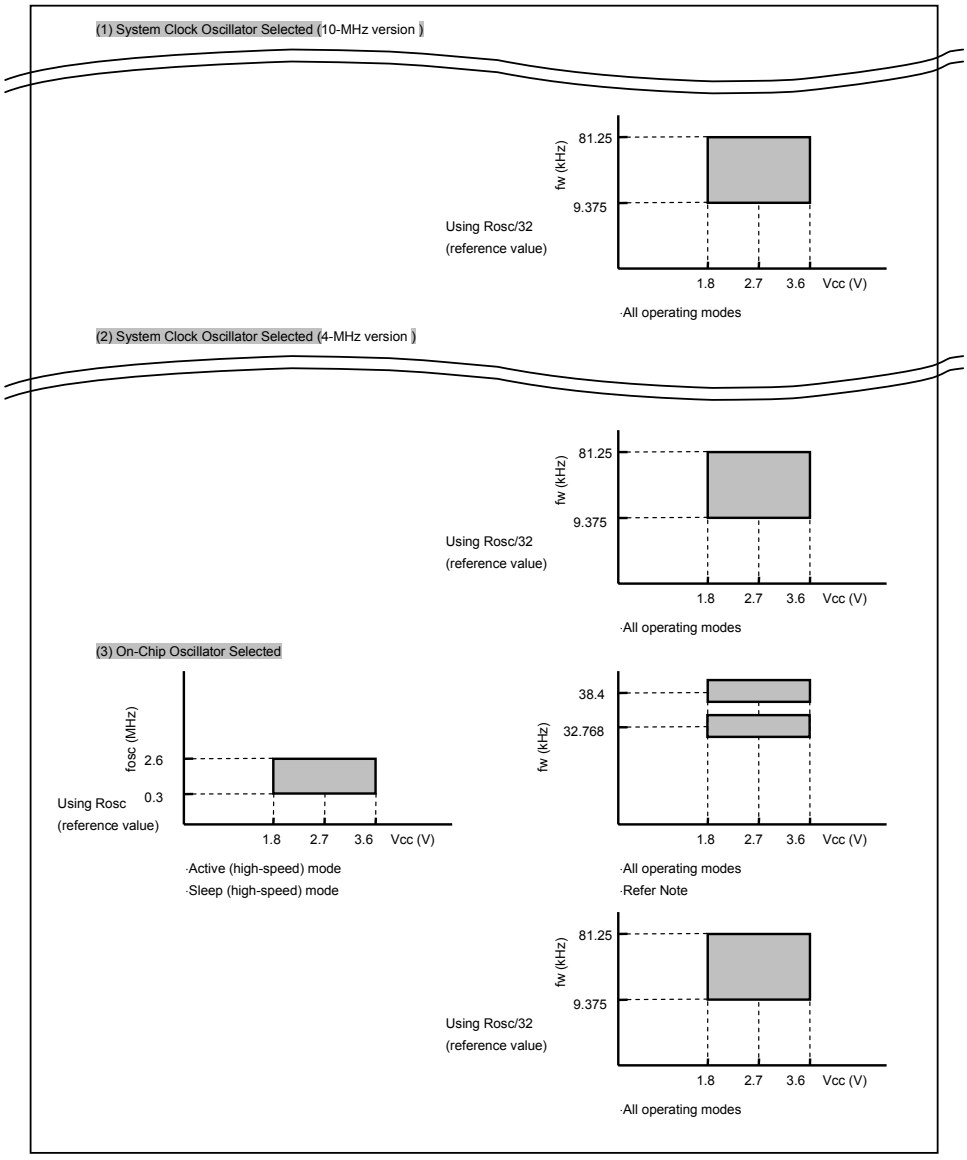


Figure 21.5 Power Supply Voltage and Oscillation Frequency Range

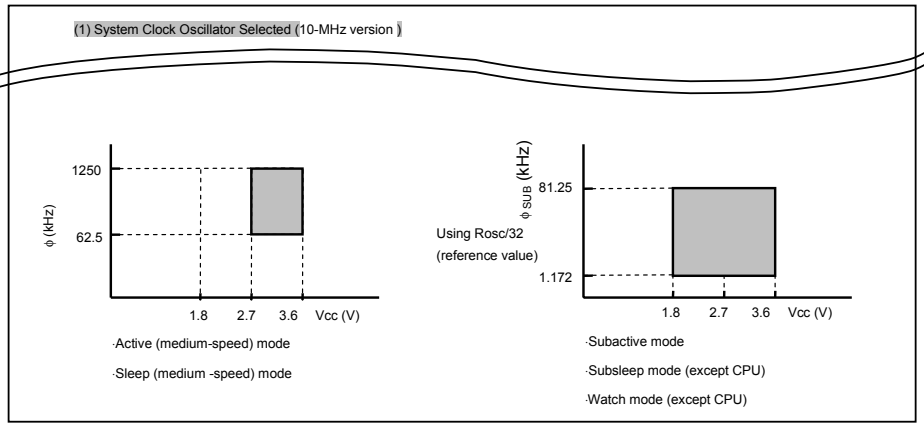


Figure 21.6 Power Supply Voltage and Operating Frequency Range (1)

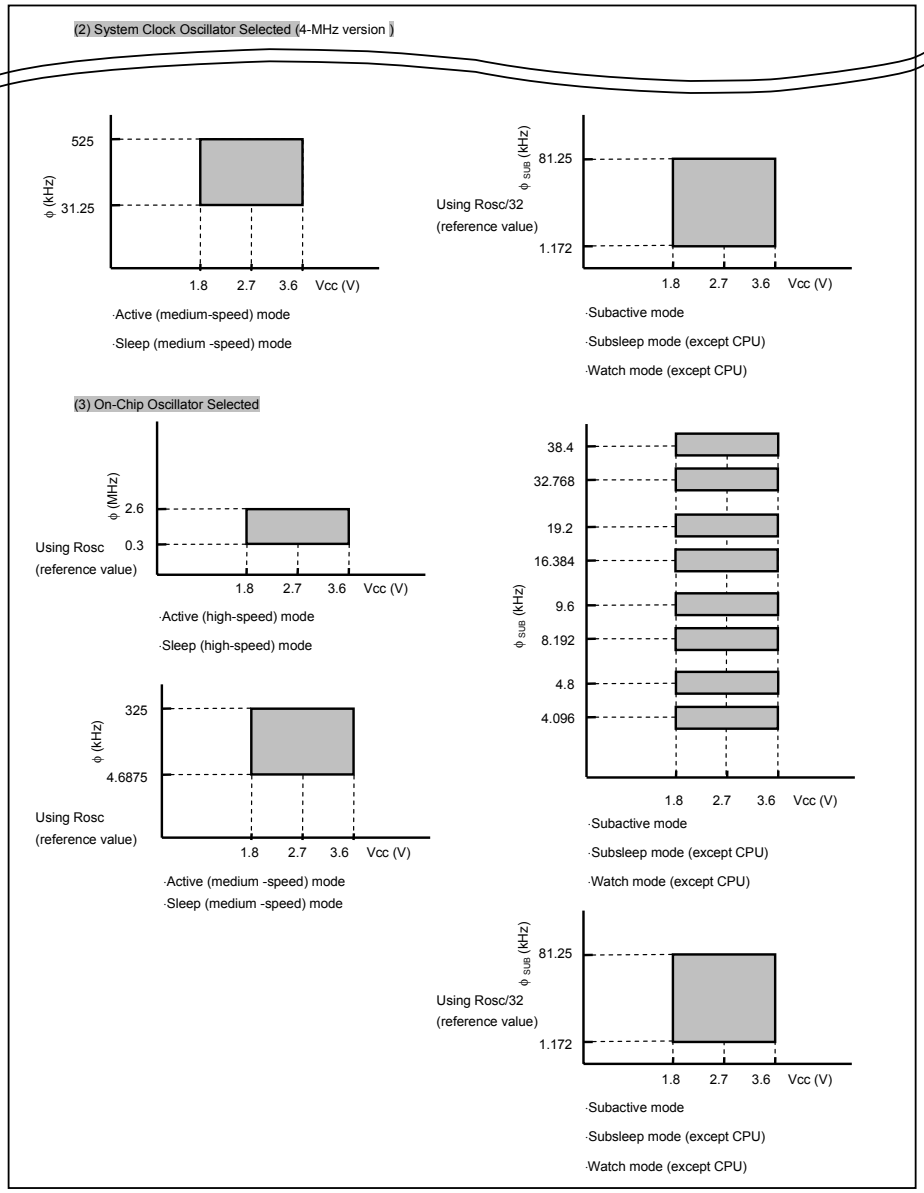


Figure 21.7 Power Supply Voltage and Operating Frequency Range (2)

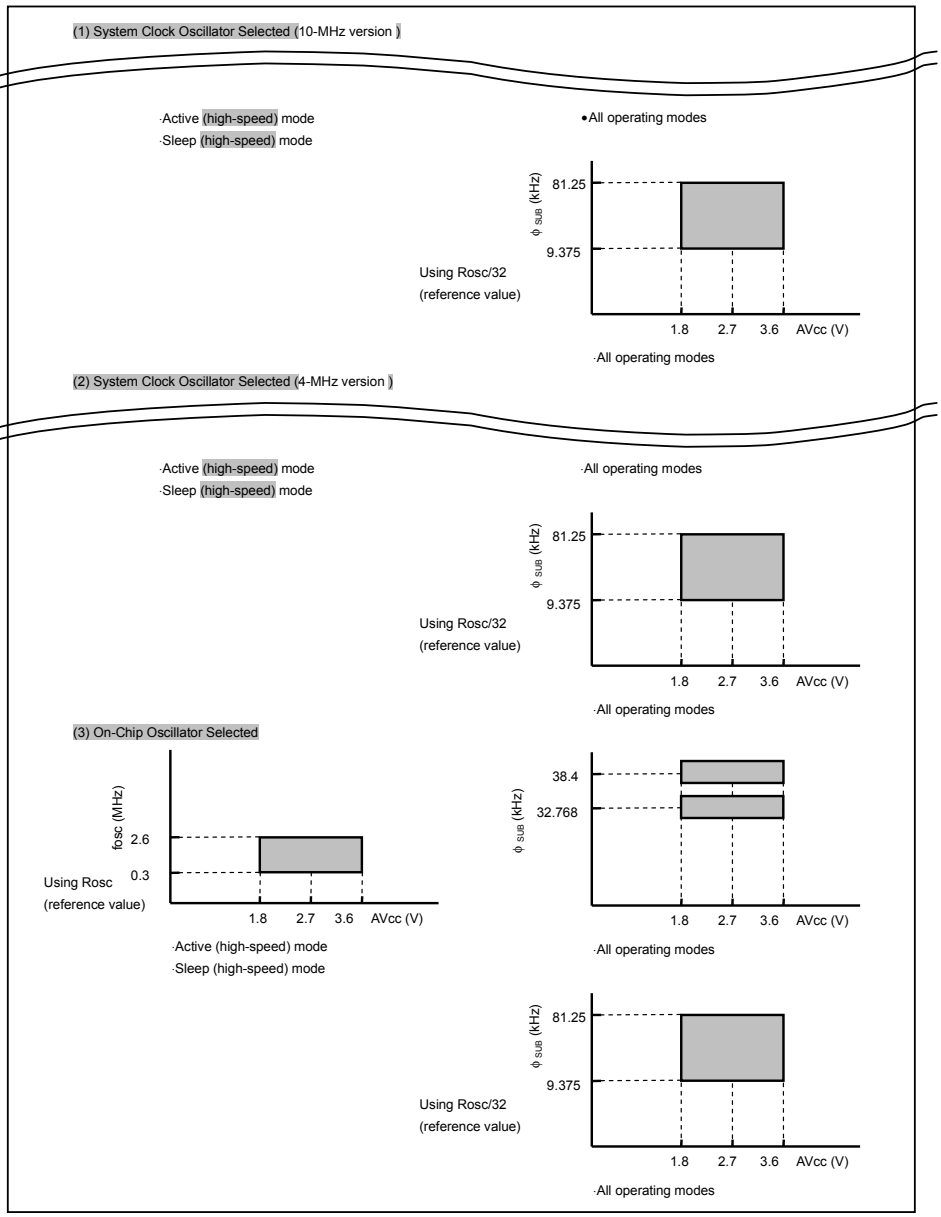


Figure 21.8 Analog Power Supply Voltage and Oscillation Frequency Range of A/D Converter

21.4.2 DC Characteristics

Table 21.13 lists the DC characteristics.

Table 21.13 DC Characteristics

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Input capacitance	C_{IN}	All input pins except power supply pin	f = 1 MHz, V_{IN} = 0 V, Ta = 25°C	–	–	15.0	pF	
Active mode current consumption	I_{OPE1}	V_{CC}	Active (high -speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz	–	TBD	–	mA	Max. guideline = 1.1 × typ.*1*2
			Active (high-speed) mode, V_{CC} = 3 V, f_{OSC} = R_{OSC}	–	TBD	–		Max. guideline = 1.1 × typ.*1*2 Reference value
			Active (high-speed) mode, V_{CC} = 3 V, f_{OSC} = 4.2 MHz	–	TBD	TBD		*1*2 4 MHz version
			Active (high-speed) mode, V_{CC} = 3 V, f_{OSC} = 10 MHz	–	TBD	TBD		*1*2 10 MHz version
	I_{OPE2}	V_{CC}	Active (medium -speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz, ϕ_{OSC}/64	–	TBD	–	mA	Max. guideline = 1.1 × typ.*1*2
			Active (medium -speed) mode, V_{CC} = 3 V, f_{OSC} = 4.2 MHz, ϕ_{OSC}/64	–	TBD	TBD		*1*2 4 MHz version
			Active (medium -speed) mode, V_{CC} = 3 V, f_{OSC} = 10 MHz, ϕ_{OSC}/64	–	TBD	TBD		*1*2 10 MHz version
Sleep mode current consumption	I_{SLEEP}	V_{CC}	V_{CC} = 1.8 V, f_{OSC} = 2 MHz	–	TBD	–	mA	Max. guideline = 1.1 × typ.*1*2
			V_{CC} = 3 V, f_{OSC} = 4.2 MHz	–	TBD	TBD		*1*2 4 MHz version
			V_{CC} = 3 V, f_{OSC} = 10 MHz	–	TBD	TBD		*1*2 10 MHz version
Subactive mode current consumption	I_{SUB}	V_{CC}	V_{CC} = 1.8 V, 32-kHz crystal resonator (ϕ_{SUB} = ϕ_W/2)	–	TBD	–	µA	*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator (ϕ_{SUB} = ϕ_W/8)	–	TBD	–		*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator (ϕ_{SUB} = ϕ_W/2)	–	TBD	–		*1*2 Reference value
			V_{CC} = 2.7 V, on-chip oscliiator/32 (ϕ_{SUB} = ϕ_W =R_{OSC}/32)	–	TBD	–		*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator (ϕ_{SUB} = ϕ_W)	–	TBD	TBD		*1*2
Subsleep mode current consumption	I_{SUBSP}	V_{CC}	V_{CC} = 2.7 V, 32-kHz crystal resonator (ϕ_{SUB} = ϕ_W/2)	–	TBD	–	µA	*1*2 Reference value
			V_{CC} = 2.7 V, on-chip oscliiator/32 (ϕ_{SUB} = ϕ_W =R_{OSC}/32)	–	TBD	–		*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator (ϕ_{SUB} = ϕ_W)	–	TBD	TBD		*1*2
Watch mode current consumption	I_{WATCH}	V_{CC}	V_{CC} = 1.8 V, Ta = 25°C, 32-kHz crystal resonator	–	TBD	–	µA	*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator	–	TBD	TBD		*1*2
Standby mode current consumption	I_{STBY}	V_{CC}	V_{CC} = 1.8 V, Ta = 25°C, 32-kHz crystal resonator not used	–	0.1	–	µA	*1*2 Reference value
			V_{CC} = 3.0 V, Ta = 25°C, 32-kHz crystal resonator not used	–	0.3	–		*1*2 Reference value
			32-kHz crystal resonator not used	–	1.0	5.0		*1*2
RAM data retaining voltage	V_{RAM}	V_{CC}		1.5	–	–	V	
Allowable output low current (per pin)	I_{OL}	Output pins except port 8		–	–	0.5	mA	
		Port 8		–	–	15.0		

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Allowable output low current (total)	ΣI_{OL}	Output pins except port 8		–	–	20.0	mA	
		Port 8		–	–	TBD		
Allowable output high current (per pin)	$-I_{OH}$	All output pins	V_{CC} = 2.7 V to 3.6 V	–	–	2.0	mA	
			Other than above	–	–	0.2		
Allowable output high current (total)	$\Sigma-I_{OH}$	All output pins		–	–	10.0	mA	

Notes: 1. Pin states during current measurement.

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	Oscillator Pins
Active (high-speed) mode (I_{OPE1})	V_{CC}	Only CPU operates	V_{CC}	System clock oscillator: Crystal resonator Subclock oscillator: Pin X1 = GND
Active (medium-speed) mode (I_{OPE2})				
Sleep mode	V_{CC}	Only on-chip timers operate	V_{CC}	
Subactive mode	V_{CC}	Only CPU operates	V_{CC}	System clock oscillator: Crystal resonator Subclock oscillator: Crystal resonator
Subsleep mode	V_{CC}	Only on-chip timers operate, CPU stops	V_{CC}	
Watch mode	V_{CC}	Only timer base operates, CPU stops	V_{CC}	
Standby mode	V_{CC}	CPU and timers both stop, SUBSTP = 1	V_{CC}	System clock oscillator: Crystal resonator Subclock oscillator: Crystal resonator

2. Excludes current in pull-up MOS transistors and output buffers.

3. When bits IRQ0S1 and IRQ0S0 are set to B'01 or B'10, and bits IRQ1S1 and IRQ1S0 are set to B'01 or B'10, the Max. value become V_{CC} + 0.3 (V).

21.4.3 AC Characteristics

Table 2.4.14 lists the control signal timing, table 21.15 lists the serial interface timing, table 21.16 lists the synchronous serial communization unit timing, and table 21.17 lists the I^2C bus interface timing.

Table 2.4.14 Control Signal Timing

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Reference Figure
System clock oscillation frequency	f_{OSC}	OSC1, OSC2	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	4.0	–	10.0	MHz	
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	2.0	–	4.2		
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC1, OSC2	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	100	–	250	ns	Figure 21.9
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	238	–	500		
System clock (ϕ) cycle time	t_{cyc}			1	–	64	t_{OSC}	
				–	–	32	µs	
On-chip oscillator frequency	f_{ROSC}			0.3	–	2.6	MHz	Reference value
On-chip oscillator clock cycle time	t_{ROSC}			0.38	–	3.3	µs	Reference value
Subclock oscillation frequency	f_w	X1, X2		–	32.768 or 38.4	–	kHz	
Watch clock (ϕ_W) cycle time	t_w	X1, X2		–	30.5 or 26.0	–	µs	Figure 21.9
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}			1	–	8	t_w	*1
Instruction cycle time				2	–	–	t_{cyc} t_{subcyc}	
Oscillation stabilization time	t_{rc}	OSC1, OSC2	Ceramic resonator (V_{CC} = 2.2 V to 3.6 V)	–	20	45	µs	Figure 21.22
			Ceramic resonator Other than above	–	80	–		
			Crystal resonator (V_{CC} = 2.7 V to 3.6 V)	–	TBD	TBD		
			Crystal resonator (V_{CC} = 2.2 V to 3.6 V)	–	TBD	TBD		
			Other than above	–	–	50	ms	
			On-chip oscillator (at power-on)	–	TBD	TBD	µs	
		X1, X2	V_{CC} = 2.2 V to 3.6 V	–	–	2	s	Figure 4.6 Figure 4.7
			Other than above	–	4	–		

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Reference Figure
External clock high width	t_{CPH}	OSC1	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	40	–	–	ns	Figure 21.9
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	95	–	–		
		X1		–	15.26 or 13.02	–	µs	
External clock low width	t_{CPL}	OSC1	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	40	–	–	ns	Figure 21.9
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	95	–	–		
		X1		–	15.26 or 13.02	–	µs	
External clock rise time	t_{CPr}	OSC1	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	–	–	10	ns	Figure 21.9
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	–	–	24		
		X1		–	–	55.0	µs	
External clock fall time	t_{CPf}	OSC1	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	–	–	10	ns	Figure 21.9
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	–	–	24		
		X1		–	–	55.0	µs	
$\overline{RES}$ pin low width	t_{REL}	$\overline{RES}$	At power-on or other than below	t_{rc} + 20 × t_{cyc}	–	–	µs	Figure 21.10*2
			Active mode or sleep mode	20	–	–	t_{cyc}	
Input pin high width	t_{IH}	$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{NMI}$, IRQAEC, $\overline{ADTRG}$, FTCI, FTIOA, FTIOB, FTIOC, FTIOD		2	–	–	t_{cyc} t_{subcyc}	Figure 21.11
		AEVL, AEVH	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	50	–	–	ns	
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	110				
Input pin low width	t_{IL}	$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{NMI}$, IRQAEC, $\overline{ADTRG}$, FTCI, FTIOA, FTIOB, FTIOC, FTIOD		2	–	–	t_{cyc} t_{subcyc}	Figure 21.11
		AEVL, AEVH	V_{CC} = 2.7 V to 3.6 V (10 MHz version)	50	–	–	ns	
			V_{CC} = 1.8 V to 3.6 V (4 MHz version)	110				

Notes: 1. Selected with the SA1 and SA0 bits in the system control register 2 (SYSCR2).

2. For details on the power-on reset characteristics, refer to table 21.10 and figure 21.20.

21.4.4 A/D Converter Characteristics

Table 21.18 lists the A/D converter characteristics.

Table 21.18 A/D Converter Characteristics

V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Analog power supply voltage	AV_{CC}	AV_{CC}		1.8	–	3.6	V	*1
Analog input voltage	AV_{IN}	AN0 to AN5		–0.3	–	AV_{CC} + 0.3	V	
Analog power supply current	AI_{OPE}	AV_{CC}	AV_{CC} = 3.0 V	–	–	1.0	mA	
	AI_{STOP1}	AV_{CC}		–	600	–	µA	*1 Reference value
	AI_{STOP2}	AV_{CC}		–	–	5	µA	*3
Analog input capacitance	C_{AIN}	AN0 to AN5		–	–	15.0	pF	
Allowable signal source impedance	R_{AIN}			–	–	10.0	kΩ	
Resolution (data length)				–	–	10	Bits	
Nonlinearity error			AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	–	–	±3.5	LSB	
			AV_{CC} = 2.0 V to 3.6 V V_{CC} = 2.0 V to 3.6 V	–	–	±5.5		
			Subclock operating	–	–	TBD		Subactive mode Subsleep mode *5
			Other than above	–	–	±7.5		*4
Quantization error				–	–	±0.5	LSB	

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Absolute accuracy			AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	–	–	±4.0	LSB	
			AV_{CC} = 2.0 V to 3.6 V V_{CC} = 2.0 V to 3.6 V	–	–	±6.0		
			Subclock operating	–	–	TBD		Subactive mode Subsleep mode *5
			Other than above	–	–	±8.0		*4
Conversion time			AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	12.4	–	124	µA	System clock oscillator Is selected
				31	62	124		On-chip oscillator Is selected Reference value (f_{ROSC} = 1 MHz)
				–	807	–		ϕ_{SUB} = 38.4 kHz
				–	945	–		ϕ_{SUB} = 32.8 kHz
				–	992	–		ϕ_{SUB} = R_{OSC}/32 Reference value (f_{ROSC} = 1 MHz)
			Other than AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	29.5	–	124	µA	System clock oscillator Is selected
				31	62	124		On-chip oscillator Is selected Reference value (f_{ROSC} = 1 MHz)
				–	807	–		ϕ_{SUB} = 38.4 kHz
				–	945	–		ϕ_{SUB} = 32.8 kHz
				–	992	–		ϕ_{SUB} = R_{OSC}/32 Reference value (f_{ROSC} = 1 MHz)

Notes: 1. Set AV_{CC} = V_{CC} when the A/D converter is not used.

2. AI_{STOP1} is the current at ladder resistance operation while the A/D converter is idle.

3. AI_{STOP2} is the current at reset, in standby mode or watch mode, while the A/D converter is idle.

4. Conversion time is 29.5 µs.

5. Conversion time is 31/ϕ_{W}.

21.4.7 Power-On Reset Circuit Characteristics

Table 21.21 lists the power-on reset circuit characteristics.

Table 21.21 Power-On Reset Circuit Characteristics

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, Ta = –20 to + 75 °C (regular specifications), Ta = –40 to + 85 °C (wide-range specifications), unless otherwise specified.

Item	Symbol	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Reset voltage	V_rst		0.7V_{CC}	0.8V_{CC}	0.9V_{CC}	V	
Power supply rise time	t_vtr		The V_{CC} rise time should be at least twice as fast as the $\overline{RES}$ rise time.				
Reset count time	t_out		0.8	–	4.0	µs	
			4.0	–	26.7		On-chip oscillator Is selected (reference value)
Count start time	t_cr		Adjustable by the value of the external capacitor of the $\overline{RES}$ pin.				
Pull-up resistance	Rp		TBD	100	–	kΩ	

21.7 Resonator Equivalent Circuit

Crystal Resonator Parameters

(Manufacture's Publicly Released Values)

Frequency (MHz)	4.19	10	Manufacturer
Rs(max.)	100Ω	30Ω	NIHON DENPA KOGYO CO., LTD.
Co(max.)	16pF	16pF	

Figure 21.22 Resonator Equivalent Circuit