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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0148A/E	Rev.	1.00
Title	I3C Note on rewriting PRTS.PRTMD bit		Information Category	Technical Notification		
Applicable Product	RA4E2 Group、RA4T1 Group、RA6E2 Group、RA6T3 Group、RA8M1 Group、RA8D1 Group、RA8T1 Group	Lot No. All	Reference Document	User's Manual for each product (see the table at the bottom)		

This document is a note on rewriting PRTS.PRTMD bit, which sets the communication protocol in the applicable products.

1. Note

When the PRTS.PRTMD bit is rewritten, the SCL terminal (and SDA terminal) may output low. In this case, the bus line is unintentionally put into a busy state, and communication cannot be started even if the communication start setting is made after that.

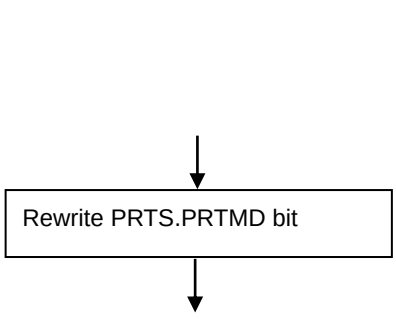
2. Cause

When the PRTS.PRTMD bit is rewritten, a hazard signal is generated in the subsequent combinational circuit, and the F/F of TCLK, which is asynchronous to the bus clock PCLK, latches this hazard, which may cause the SCL pin (and SDA pin) to unintentionally output low level.

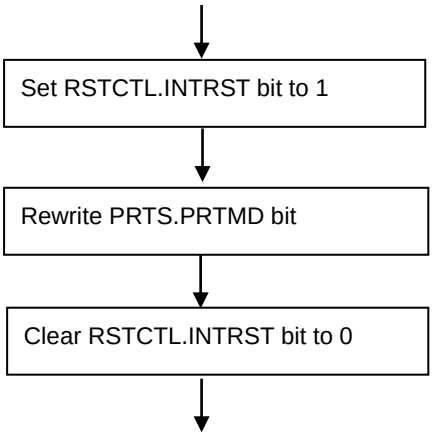
This phenomenon does not occur when TCLK and PCLK are the same clock source.

3. Workaround

To prevent hazard propagation, set the RSTCTL.INTRST bit to 1 and issue an internal software reset before rewriting the PRTMD bit. After rewriting, set the RSTCTL.INTRST bit to 0 to release the internal software reset.



Before



After

However, no countermeasure is necessary if the following conditions are applicable.

1. When the PRTS.PRTMD bit is not changed from its initial value of 1 (I2C protocol mode) to 0 (I3C protocol mode).
2. When the clock source selected by SCKSCR.CKSEL[2:0] and I3CCKCR.I3CCKSEL[3:0] are the same.
3. In master mode, when the timeout error detection function is enabled under the following conditions and a software reset is set in the I3C error interruption routine to release unintended low output.
    1. Set the BSTE.TODE bit to 1 to enable the timeout error detection function.
    2. Select TMOCTL.TOMDS[1:0] = b'00 or b'01 as the timeout operation mode and set the TMOCTL.TOLCTL bit = 1 and TMOCTL.TOHCTL bit = 1 to treat the SCL line fixed at low and fixed at high as errors.
    3. In the I3C error interruption routine, set the RSTCTL.RI3CRST bit to 1 to perform an I3C software reset, or set the RSTCTL.INTLRST bit to 1 to perform an internal software reset.
4. In slave mode, when the timeout error detection function is enabled under the following conditions and a software reset is set in the I3C error interruption routine to release unintended low output.
    1. Set the BSTE.TODE bit to 1 to enable the timeout error detection function.
    2. Select TMOCTL.TOMDS[1:0] = b'01 as the timeout operation mode and set TMOCTL.TOLCTL=1 and TMOCTL.TOHCTL = 1 to treat the SCL line fixed at low and fixed at high as errors.
    3. In the I3C error interruption routine, set the RSTCTL.RI3CRST bit to 1 to perform an I3C software reset, or set the RSTCTL.INTLRST bit to 1 to perform an internal software reset.

【Reference Documents】

Applicable Products	Related Document (Document Number)	Related Chapter Number
RA4E2 Group	RA4E2 Group User's Manual: Hardware Rev.1.30 (R01UH0996JJ0130)	27.2.1 PRTS : Protocol Selection Register 27.3.3.1.1 I2C Initial Setting Flow (Single Buffer Transfer) 27.3.3.1.2 I3C Initial Setting Flow
RA4T1 Group	RA4E2 Group User's Manual: Hardware Rev.1.20 (R01UH0999JJ0120)	25.2.1 PRTS : Protocol Selection Register 25.3.3.1.1 I2C Initial Setting Flow (Single Buffer Transfer) 25.3.3.1.2 I3C Initial Setting Flow
RA6E2 Group	RA6E2 Group User's Manual: Hardware Rev 1.30 (R01UH0988JJ0130)	27.2.1 PRTS : Protocol Selection Register 27.3.3.1.1 I2C Initial Setting Flow (Single Buffer Transfer) 27.3.3.1.2 I3C Initial Setting Flow
RA6T3 Group	RA6T3 Group User's Manual: Hardware Rev.1.20 (R01UH0998JJ0120)	26.2.1 PRTS : Protocol Selection Register 26.3.3.1.1 I2C Initial Setting Flow (Single Buffer Transfer) 26.3.3.1.2 I3C Initial Setting Flow
RA8M1 Group	RA8M1 Group User's Manual: Hardware Rev.1.20 (R01UH0994JJ0120)	33.2.1 PRTS : Protocol Selection Register 33.3.3.1.1 I2C Initial Setting Flow (Single Buffer Transfer) 33.3.3.1.2 I3C Initial Setting Flow
RA8D1 Group	RA8D1 Group User's Manual: Hardware Rev.1.20 (R01UH0995JJ0120)	33.2.1 PRTS : Protocol Selection Register 33.3.3.1.1 I2C Initial Setting Flow (Single Buffer Transfer) 33.3.3.1.2 I3C Initial Setting Flow
RA8T1 Group	RA8T1 Group User's Manual: Hardware Rev.1.20 (R01UH1016JJ0120)	30.2.1 PRTS : Protocol Selection Register 30.3.3.1.1 I2C Initial Setting Flow (Single Buffer Transfer) 30.3.3.1.2 I3C Initial Setting Flow