Date: Jun. 19, 2025

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0145A/E	Rev.	1.00
Title	Issue and adding notifications related to the ΔΣ interface (DSMIF)		Information Category	Technical Notification		
Applicable Product	RZ/T1 Group	Lot No. All lots	Reference Document	RZ/T1 User's Manual Hardware Rev.1.90 (R01UH0483EJ0190)		

This document describes an issue with the ΔΣ interface (DSMIF) of RZ/T1 Group and an addition to the Usage Notes section of the DSMIF chapter in the User's Manual.

[1-1] Issue details

When the DSMIF is configured in slave mode (DSCR.DSCK0=0, DSCR.DSCK1=0) and an MCLK frequency exceeding 15MHz is input, the following register value(s) may become invalid. Furthermore, if the error mask in ECM Error Mask Register 0 is disabled, these invalid register values may lead to false detection of UVW overcurrent abnormality detection error, UVW total current abnormality detection error, and X overcurrent abnormality detection error.

This issue does not occur when the DSMIF is configured in master mode.

- UVW status register (UVWSTA) b8, b2, b1, b0
  - Channel U current value register 1 (U1DATA) b15-b0
  - Channel U Current Value Mountain Trigger Capture Register 1 (U1CDATA) b15-b0
  - Channel U Current Value Valley Trigger Capture Register 1 (U1VDATA) b15-b0
  - Channel U current value register 2 (U2DATA) b15-b0
  - Channel V current value register 1 (V1DATA) b15-b0
  - Channel V Current Value Mountain Trigger Capture Register 1 (V1CDATA) b15-b0
  - Channel V Current Value Valley Trigger Capture Register 1 (V1VDATA) b15-b0
  - Channel V current value register 2 (V2DATA) b15-b0
  - Channel W current value register 1 (W1DATA) b15-b0
  - Channel W Current Value Mountain Trigger Capture Register 1 (W1CDATA) b15-b0
  - Channel W Current Value Valley Trigger Capture Register 1 (W1VDATA) b15-b0
  - Channel W current value register 2 (W2DATA) b15-b0
  - XYZ status register XYZSTA) b8
  - Channel X current value register 1 (X1DATA) b15-b0
  - Channel X Current Value Mountain Trigger Capture Register 1 (X1CDATA) b15-b0
  - Channel X Current Value Valley Trigger Capture Register 1 (X1VDATA) b15-b0
  - Channel X current value register 2 (X2DATA) b15-b0

DSMIF errors that can be falsely detected by ECM:

- UVW overcurrent abnormality detection error
- UVW total current abnormality detection error
- X overcurrent abnormality detection error

【1-2】Workaround

When using DSMIF in slave mode (unit0: DSCR.DSCK0=0, unit1: DSCR.DSCK1=0), please ensure that the input MCLK frequency does not exceed 15MHz. The changes to the electrical characteristics are shown below in red.

・R01UH0483EJ0190 Rev.1.90 Page 2593

Table 47.34 ΔΣ Interface Timing

Conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item			Symbol	min	max	Unit	Test Conditions
DSMIF	Clock cycle	Master	t_{DScyc}	1	1	t_{DCcyc}	Figure 47.79
		Slave		~~40~~ 66.67	200	ns	
	Clock high level	Master	t_{DSCKWH}	16	—	ns	
		Slave		~~16~~ 26.67	—	ns	
	Clock low level	Master	t_{DSCKWL}	16	—	ns	
		Slave		~~16~~ 26.67	—	ns	
	Setup time	Master	t_{SU}	15	—	ns	Figure 47.80, Figure 47.81
		Slave		10	—	ns	
	Hold time	Master	t_H	0	—	ns	
		Slave		10	—	ns	

Note: t_{DCcyc}: One cycle time of the ΔΣ interface clock (DSCLK0, DSCLK1)

[2-1] Notes when there is an unused channel in DSMIF unit 0

A short-circuit abnormality may be falsely detected when there are unused channels in DSMIF Unit 0 Channel 0-2, a non-zero value is set in the UVW short-circuit abnormality detection 0 data input threshold setting register (UVWSCUNCMP.CMPUVWSCUNDER) and only MCLK0 is used (DSCR.DSCHSEL=1) in either master mode (DSCR.DSCK1=1) or slave mode (DSCR.DSCK0=1). As a result, the following status bits may be set, or incorrect UVW short-circuit abnormality detection errors may occur.

- Short-Circuit Abnormality Detection Status bits (ERxSC) of unused channels in the UVW Status Register (UVWSTA) b6-b4
- UVW short-circuit abnormality detection error

Therefore, please take the following measures and use DSMIF.

[2-2] Measures for an unused channel in DSMIF unit 0

- Ignore the short-circuit abnormality detection status of the UVW Status Register (UVWSTA) unused channel.

  b6 : Ignore if channel 2 (W) is not used
  b5 : Ignore if channel 1 (V) is not in use
  b4 : Ignore if channel 0 (U) is not in use

- Set all of the following bits to 0 (disable interrupt and reset caused by error detection).
  (Initial values are all 0)
  ECM Maskable Interrupt Configuration Register 0 (ECMMICFG0) b27
  ECM Non-maskable Interrupt Configuration Register 0 (ECMNMICFG0) b27
  ECM Internal Reset Configuration Register 0(ECMIRCFG0) b27

- Set the following bits to 1 (mask the output to the error pin when an error occurs). (The default value is 0)
  ECM Error Mask Register 0 (ECMEMK0) b27

[3] Revisions to the User's Manual : Hardware

The User’s Manual: Hardware will be revised to reflect and add the contents of this document.