To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A612A/E	Rev.	1.00
Title	Notes of address error exception handling related to instruction fetch		Information Category	Technical Notification		
Applicable Product	R5S72060W200FPV R5E72060W200FPV	Lot No. ALL	Reference Document	SH7206 Group Hardware Manual Rev.2.00 (REJ09B0191-0200)		

In the above-mentioned product of SH2A, We would like to announce the notes about the address error exception handling related to instruction fetch. The following Note description is an additional description.

4.3.2 Address Error Exception Handling

When an address error occurs, the bus cycle in which the address error occurred ends.***** When the executing instruction then finishes, address error exception handling starts. The CPU operates as follows:

1. the exception service routine start address which corresponds to the address error that occurred in fetched from the exception handling vector table.
2. The status register(SR) is saved to the stack.
3. The program counter(PC) is saved to the stack. The PC value saved is the start address of the instruction to be executed after the last executed instruction

After jumping to the exception service routine start address fetched from the exception handling vector table, program execution saterts. The jump that occurs is not a delayed branch.

Note: In the case of address error related to data read/write. In the case of address error related to instruction fetch, If the bus cycle in which the address error occurred doesn't end until the entire three above-mentioned operations end, the CPU will start address error exception handling again until the bus cycle in which the address error occurred ends.